LinCMOS™ Data Book

TEXAS INSTRUMENTS

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Specifications contained in this data book supersede all data for these products published by TI before September 1987.

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First Edition

Compiled by Geoffrey Arnold

INTRODUCTION

Low power, low voltage, single supply circuits with their reduced operating temperature and enhanced reliability, allow for smaller equipment sizes and reduce the total cost of system ownership. Applying this fact to the world of digital electronics has been relatively simple with the introduction of digital CMOS technology. The same cannot be said for the analog world where upto now the designer has been faced with some uncomfortable compromises when looking for low power, low voltage operation, high performance analog components. With the introduction of Texas Instruments' LinCMOS technology, a technology specifically for Linear ICs, compromises are no longer necessary. LinCMOS has allowed the development of a complete family of analog components. Devices which are designed to operate from low voltage single supplies at minimal power dissipation with optimum performance.

LinCMOS is a true Linear technology, one that combines several innovations to overcome the problems associated with conventional metal gate technology. By utilizing phosphorous doped polysilicon gates, the transistor threshold drift associated with metal gate CMOS has virtually been eliminated. Op-amps were the first devices to be introduced in this technology offering the designer excellent stability with time, temperature and voltage. However LinCMOS is not only suitable for the fabrication of op-amps, the complete analog system is now available in LinCMOS including Analog to digital and Digital to analog converters. With the introduction of Advanced LinCMOS, LSI densities are possible for devices which contain both analog and digital circuits.

This data book is a compilation of all the current LinCMOS data sheets, the majority of the devices featured are readily available however please contact your local TI office or nearest distributor for up-to-date availability.

Information on the following types of LinCMOS products is included in this data book:

- Operational Amplifiers
- Voltage Comparators
- Timers
- Analog to Digital Converters
- Digital to Analog Converters
- Analog Switches
- Switched Capacitor Filters

At the front of each section is a selection guide to help you in defining the device which exactly meets your design criteria. The data book also contains packaging information both on conventional dual-in-line packaging and the new surface mount packages. Package options by device are included in the respective data sheet.

Ordering information and an alpha numeric listing are detailed in the general information section at the front of the data book.

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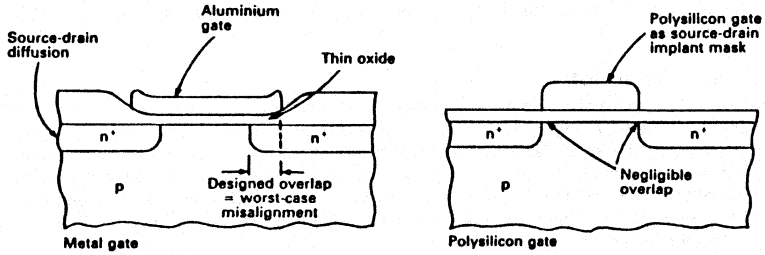
LinCMOS OVERVIEW

WHAT IS LinCMOS?

Texas Instruments' LinCMOS is a linear polysilicon-gate complementary-MOS process with p and n MOS transistors optimised to give bipolar type offsets and voltage swings. This process improves on the metal gate CMOS process in stability, speed and flexibility for linear building blocks such as operational amplifiers and comparators. The prime disadvantage of linear CMOS using the metal gate process has been the input transistors' threshold shift with time, temperature and applied gate voltage. This is caused by the migration of residual sodium ions in the gate oxide to the gate-oxide or silicon-oxide interface dependent on the polarity of the voltages stress. The resulting redistribution of charge causes threshold-voltage shifts that can be as great as hundreds of millivolts.

The LinCMOS process uses phosphorous doped polysilicon gates to counteract sodium drifts by trapping the sodium ions in the crystal structure. [Poly(crystalline) silicon is a layer of silicon with dislocations in the crystal structure. It is deposited by chemical vapour deposition in a similar manner to an epitaxial layer but at a lower temperature.] Op-amps may be built with voltage offset values of 2–5 mV with negligible drift and obtain these values without trimming.

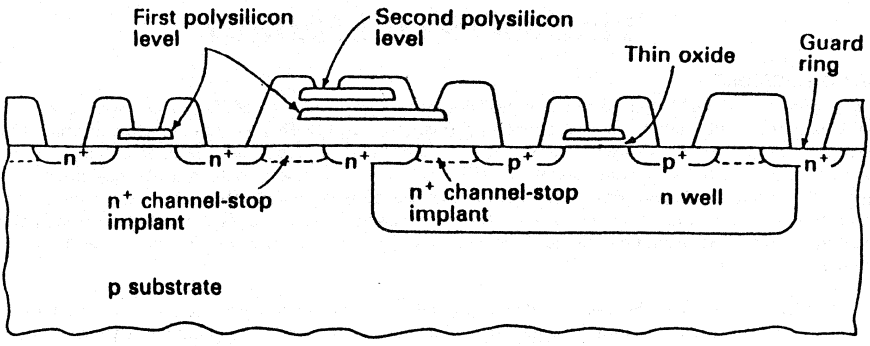
FIG. 1.1 METAL & POLYSILICON GATE ALIGNMENT COMPARISON



Polysilicon gate CMOS devices also have a two or three times greater band with than their metal gate counterparts because of a seven times reduction in gate capacitance. In a polysilicon gate process the polysilicon is laid down first and provides a self aligned mask for the source/drain diffusion (see Figure 1.1). In the metal gate process the diffusions are formed first so the metal gate must overlap the drain and source regions to ensure channel coverage.

The LinCMOS structure (Fig. 1.2) uses n-MOS devices in a p-type substrate and p-MOS devices in n-wells, unlike most CMOS digital circuits in which the structure is reversed. This optimises the inherently faster n-MOS devices at the expense of the p-types. Speed is proportional to carrier mobility, which is inversely dependent on channel doping level. The more heavily doped 'well' devices will be slower than those in the substrate. Putting the n-MOS devices in the substrate gives their carriers a 3–4 times greater mobility than those of the p-MOS transistors. In a p-well process the mobility is only 1.5 times greater.

FIG. 1.2



LinCMOS. An n-well structure is used so that the n-MOS devices of this process sit in the substrate and run faster. Linear circuits also benefit from the stable offset voltages afforded by silicon gates. A second polysilicon layer adds wiring channels and capacitors.

Digital designers have had to find ways to speed up p-MOS devices because they cannot be eliminated from the signal paths. However bipolar analogue designers are accustomed to using faster vertical npn transistors in signal paths and living with slower lateral pnp devices. This strategy has been adopted for LinCMOS with n-MOS and p-MOS devices.

LinCMOS CIRCUIT DESCRIPTION

An operational amplifier's input circuit is its most critical section as from here the stability, offsets and noise are largely determined. As shown in Figure 1.3 the input stage comprises p-MOS inputs (P_1 and P_2) and a n-MOS current mirror (N_1 and N_2). These are large transistors made up of many small circular, cross coupled geometries which counteract process variations and take up about half the chip's area. The complex interconnection gives precise matching of the P_1P_2 and N_1N_2 pairs and minimises the effects of thermal and mechanical stresses on the stability of the input offset voltage. For critical applications where less than 2mV of offset is required null pins are provided on the singles for offset zeroing.

Large p-MOS transistors are used because noise voltage generated by MOS transistors is inversely proportional to area. Noise from the n-MOS pair is converted into noise current in the p-MOS drain circuit so the n-MOS transistors have very long channels to keep their transconductance ($g_m \propto W/L$) small. The ratio of g_{mp} to g_{mn} is maximised within the constraints of geometric and electrical trade offs to generate as little noise as possible.

Use of a p-MOS differential input pair allows the common mode range to include the most negative supply rail, 0 V, in single rail applications. This is made possible by the body effect, the modulation of the gate source voltage from the bulk side of the transistor (see Figure 1.1) which increases the p-MOS transistors threshold voltage. This keeps the p-MOS input pair and n-MOS mirror in current saturation when the gates are at 0V.

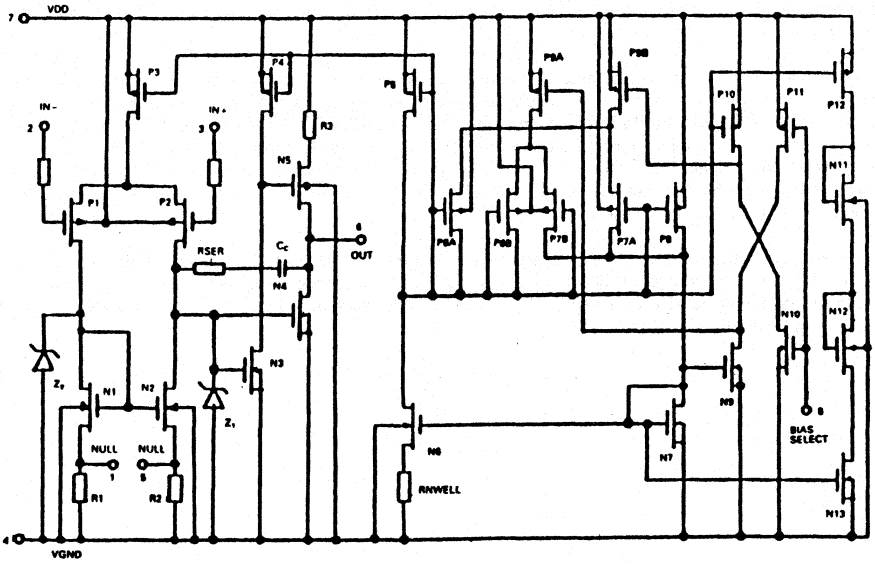
Transistor P_3 is the constant current source for the pair P_1P_2 and P_4 acts as a constant current load for the voltage amplifier N_3. Approximately half the voltage gain comes from the differential input stage comprising P_1P_2 with N_1N_2 as a current mirror active load. The other half comes from the N_3N_4 combination, N_3 for the positive output swing and N_4 for the negative output swing.

Transistors N_4 and N_5 provide small signal output drive current in class A. N_5 is connected as a source follower with drain resistor R_3 and the large N_4 as a bias current source. Transistor N_4 sinks large signal output currents. Zener diode Z_1 clamps N_4's gate to about 6V to limit the output current and give protection from shorts to V_{DD}. Zener diode Z_2 matches Z_1's leakage curents and prevents the input stage shifting in response to temperature. Large output source current is provided by N_5 and limited by R_3 to give short circuit protection.

The internal frequency compensation capacitor C_c of 12pF is connected from the gate of N_3 to the drain of N_4 and controls the circuits high frequency roll-off to ensure stability in voltage follower configurations (see op-amps compared and stability sections).

The chip's supply current setting circuit allows quiescent current adjustment over three decades, 10 to 1000 µA. Switching between currents is performed by transistor switches P_{9A} and P_{9B}. Connecting pin 8 to ground opens both P_{9A} and P_{9B} resulting in the high supply current mode. Connecting pin 8 to V_{DD} closes both P_{9A} and P_{9B} for low supply current operation. When pin 8 is connected to a voltage at least 0.8V above ground or below V_{DD} P_{9A} is closed and P_{9B} is open resulting in the medium current mode of operation.

FIG. 1.3 TLC271 SCHEMATIC DIAGRAM



Switches P_{9A} and P_{9B} select the current mode in the following manner: P_{9A} switches P_{6A} and P_{7A} into or out of the p-MOS mirror formed by P_5 and P_8, thus changing the width to length ratio of P_5 and P_8 with respect to P_3 and P_4. Since the P_5 diode is operating at a constant current, this alters the gate to source voltage of P_3 and P_4, to change the current by a factor of ten. Similarly, P_{9B} switches P_{6B} and P_{7B} into or out of the p-MOS mirror to change the current by an additional decade.

ADVANCED LinCMOS

Advanced LinCMOS features a scaled down version of the first generation process: in addition to 5 µm, Advanced LinCMOS has 3 µm capability. This is more important in integrated circuits which contain digital circuits and analog circuits. Advanced LinCMOS achieves the density levels needed for complex data-acquisition and telecommunication chips in addition to other high-performance integrated circuits requiring the use of combined analog and digital circuitry.

Besides the reduced geometry sizes, the use of a low resistance substrate removes the need for bulky guard rings between n- and p-channel devices, again increasing packing density. Capacitor and resistor structures, important for analog components, have been re-worked so they occupy typically one fourth the area compared with the old technology.

Like LinCMOS, Advanced LinCMOS is a double level poly-silicon process. However where the n-well of LinCMOS is fabricated in a p-substrate the n-well of the twin-well Advanced LinCMOS is fabricated in a p– epitaxial layer grown on top of a p+ substrate. This reduces the critical spacing of n+ to n– and p+ to n– regions.

The use of the low-resistance substrate reduces latchup susceptability and eliminates the need for guard rings between n– and p-channel devices. Because an LSI part contains many more individual transistors than a small- or medium scale IC, single or multiple guard rings for each transistor would occupy a considerable portion of the total chip area.

Switched capacitor structures are common to many A/D converters but are expensive in terms of chip area. For an increase of a single bit in resolution an A/D converter requires twice the capacitor area when the process technology uses binary-weighted switched capacitors, as does LinCMOS. To overcome this limitation Advanced LinCMOS uses a new capacitor structure consisting of an oxide-nitride sandwich. The oxide-nitride sandwich allows much thinner dielectrics and hence larger capacitors to be fabricated per unit area. The result is an effective oxide thickness which is just one fourth that of the straight-oxide capacitors in LinCMOS and a fourfold increase in capacitance per unit area.

The net result of all the reductions in chip real estate is demonstrated in the TLC7524 Digital to Analog converter. This DAC is 25% smaller in silicon area than competitor equivalents while having a 40% faster settling time. Digital interfacing is also enhanced, the new DAC is capable of 40% to 50% faster access times than competitive equivalents.

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TLC272	2-95
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TLC277	2-95
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TLC27L7	2-155
TLC27L9	2-245
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TLC27M4	2-215
TLC27M7	2-125
TLC27M9	2-215
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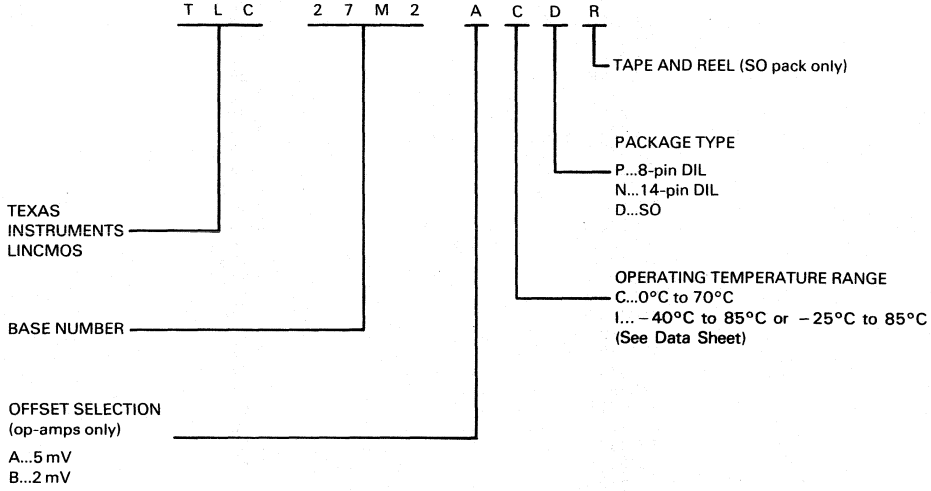
ORDERING INSTRUCTIONS

ORDERING INSTRUCTIONS

Electrical characteristics presented in this data book, unless otherwise noted, apply for the circuit type(s) listed in the page heading regardless of package. The availability of a circuit function in a particular package is denoted by an alphabetical reference above the pin-connection diagram(s). These alphabetical references refer to mechanical outline drawings shown in this section.



Circuits are shipped in one of the carriers below. Unless a specific method of shipment is specified by the customer (with possible additional costs), circuits will be shipped on the most practical carrier.

(D,DW,J,JD,JG,N,P)
–Slide Magazines
–A-Channel Plastic Tubing
–Barnes Carrier
–Sectioned Cardboard Box
–Individual Cardboard Box

Chip Carriers (FD,FH,FJ,FK,FN)
–Anti-Static Plastic Tubing
Flat (U,W)
–Barnes Carrier
–Milton Ross Carrier

Power Tab (KC,KH,KV)
–Sleeves

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OPERATIONAL AMPLIFIERS

	SUPPLY VOLTAGE (V)		SUPPLY CURRENT PER AMP (mA)	SLEW RATE (V/μS)	BAND-WIDTH MHZ	VOLTAGE GAIN V/mV	INPUT OFFSET VOLTAGE (mV)			INPUT BIAS CURRENT AT 25°C (pA)	PAGE No.
	Min	Max					STD	A	B		
Single											
TLC271	3(4)†	16	0.02/2.0*	0.04/4.5*	0.1/2.3*	50/10	10	5	2	0.7	2-33
TLC251	1.4	16	0.02/2.0*	0.04/4.5*	0.1/2.3*	50/10	10	–	–	0.7	2-7
Dual											
TLC272	3(4)†	16	2.0	4.5	2.3	10	10	5	2	0.7	2-95
TLC27M2	3(4)†	16	0.3	0.6	0.7	25	10	5	2	0.7	2-125
TLC27L2	3(4)†	16	0.02	0.04	0.1	50	10	5	2	0.7	2-155
TLC252	1.4	16	2.0	4.5	2.3	10	10	–	–	0.7	2-17
TLC25M2	1.4	16	0.3	0.6	0.7	25	10	–	–	0.7	2-125
TLC25L2	1.4	16	0.02	0.04	0.1	50	10	–	–	0.7	2-155
TLC277	3(4)†	16	2.0	4.5	2.3	10	0.5	–	–	0.7	2-95
TLC27M7	3(4)†	16	0.3	0.6	0.7	25	0.5	–	–	0.7	2-125
TLC27L7	3(4)†	16	0.02	0.04	0.1	50	0.5	–	–	0.7	2-155
Quad											
TLC274	3(4)†	16	2.0	4.5	2.3	10	10	5	2	0.7	2-185
TLC27M4	3(4)†	16	0.3	0.6	0.7	25	10	5	2	0.7	2-215
TLC27L4	3(4)†	16	0.02	0.04	0.1	50	10	5	2	0.7	2-245
TLC254	1.4	16	2.0	4.5	2.3	10	10	–	–	0.7	2-25
TLC25M4	1.4	16	0.3	0.6	0.7	25	10	–	–	0.7	2-215
TLC25L4	1.4	16	0.02	0.04	0.1	50	10	–	–	0.7	2-245
TLC279	3(4)†	16	2.0	4.5	2.3	10	0.9	–	–	0.7	2-185
TLC27M9	3(4)†	16	0.3	0.6	0.7	25	0.9	–	–	0.7	2-215
TLC27L9	3(4)†	16	0.02	0.04	0.1	50	0.9	–	–	0.7	2-245

**Signifies the value is dependent on the bias mode of the op-amp as set in the application.*

†Indicates Industrial Temp Range.

GLOSSARY
OPERATIONAL AMPLIFIER TERMS AND DEFINITIONS

Input Offset Voltage (V_{IO})

The d-c voltage that must be applied between the input terminals to force the quiescent d-c output voltage to zero or other level, if specified.

Average Temperature Coefficient of Input Offset Voltage (α_{VIO})

The ratio of the change in input offset voltage to the change in free-air temperature. This is an average value for the specified temperature range.

$$\alpha_{VIO} = \left[\frac{(V_{IO} \text{ @ } T_{A(1)}) - (V_{IO} \text{ @ } T_{A(2)})}{T_{A(1)} - T_{A(2)}}\right]$$ where $T_{A(1)}$ and $T_{A(2)}$ are the specified temperature extremes.

Input Offset Current (I_{IO})

The difference between the currents into the two input terminals with the output at zero volts.

Average Temperature Coefficient of Input Offset Current (α_{IIO})

The ratio of the change in input offset current to the change in free-air temperature. This is an average value for the specified temperature range.

$$\alpha_{IIO} = \left[\frac{(I_{IO} \text{ @ } T_{A(1)}) - (I_{IO} \text{ @ } T_{A(2)})}{T_{A(1)} - T_{A(2)}}\right]$$ where $T_{A(1)}$ and $T_{A(2)}$ are the specified temperature extremes.

Input Bias Current (I_{IB})

The average of the currents into the two input terminals with the output at zero volts.

Common-Mode Input Voltage (V_{IC})

The average of the two input voltages.

Common-Mode Input Voltage Range (V_{ICR})

The range of common-mode input voltage that if exceeded will cause the amplifier to cease functioning properly.

Differential Input Voltage (V_{ID})

The voltage at the noninverting input with respect to the inverting input.

Maximum Peak Output Voltage Swing (V_{OM})

The maximum positive or negative peak output voltage that can be obtained without waveform clipping when the quiescent d-c output voltage is zero.

Maximum Peak-to-Peak Output Voltage Swing (V_{OPP})

The maximum peak-to-peak output voltage that can be obtained without waveform clipping when the quiescent dc output voltage is zero.

Large-Signal Voltage Amplification (A_V)

The ratio of the peak-to-peak output voltage swing to the change in input voltage required to drive the output.

Differential Voltage Amplification (A_{VD})

The ratio of the change in output voltage to the change in differential input voltage producing it.

Equivalent Input Noise Voltage (V_n)

The voltage of an ideal voltage source (having an internal impedance equal to zero) in series with the input terminals of the device that represents the part of the internally generated noise that can properly be represented by a voltage source.

Equivalent Input Noise Current (I_n)

The current of an ideal current source (having an internal impedance equal to infinity) in parallel with the input terminals of the device that represents the part of the internally generated noise that can properly be represented by a current source.

Average Noise Figure (F)

The ratio of (1) the total output noise power within a designated output frequency band when the noise temperature of the input termination(s) is at the reference noise temperature, T_O, at all frequencies to (2) that part of (1) caused by the noise temperature of the designated signal-input termination within a designated signal-input frequency band.

Short-Circuit Output Current (I_{OS})

The maximum output current available from the amplifier with the output shorted to ground, to either supply, or to a specified point.

Supply Current (I_{CC})

The current into the V_{CC} or V_{CC+} terminal of an integrated circuit.

Total Power Dissipation (P_D)

The total d-c power supplied to the device less any power delivered from the device to a load.
NOTE: At no load: $P_D = V_{CC+} \bullet I_{CC+} + V_{CC-} \bullet I_{CC-}$.

Crosstalk Attenuation (V_{o1}/V_{o2})

The ratio of the change in output voltage of a driven channel to the resulting change in output voltage of another channel.

Rise Time (t_r)

The time required for an output voltage step to change from 10% to 90% of its final value.

Total Response Time (Settling Time) (t_{tot})

The time between a step-function change of the input signal level and the instant at which the magnitude of the output signal reaches for the last time a specified level range ($\pm \varepsilon$) containing the final output signal level.

Overshoot Factor

The ratio of (1) the largest deviation of the output signal value from its final steady-state value after a step-function change of the input signal, to (2) the absolute value of the difference between the steady-state output signal values before and after the step-function change of the input signal.

Slew Rate (SR)

The average time rate of change of the closed-loop amplifier output voltage for a step-signal input.

Maximum-Output-Swing Bandwidth (B_{OM})

The range of frequencies within which the maximum output voltage swing is above a specified value.

Unity-Gain Bandwidth (B_1)

The range of frequencies within which the open-loop voltage amplification is greater than unity.

Phase Margin (ϕ_m)

The absolute value of the open-loop phase shift between the output and the inverting input at the frequency at which the modulus of the open-loop amplification is unity.

Gain Margin (A_m)

The reciprocal of the open-loop voltage amplification at the lowest frequency at which the open-loop phase shift is such that the output is in phase with the inverting input.

Input Resistance (r_i)

The resistance between the input terminals with either input grounded.

Differential Input Resistance (r_{id})

The small-signal resistance between the two ungrounded input terminals.

Output Resistance (r_o)

The resistance between the output terminal and ground.

Input Capacitance (C_i)

The capacitance between the input terminals with either input grounded.

Common-Mode Input Impedance (z_{ic})

The parallel sum of the small-signal impedance between each input terminal and ground.

Output Impedance (z_o)

The small-signal impedance between the output terminal and ground.

Common-Mode Rejection Ratio (k_{CMR}, CMRR)

The ratio of differential voltage amplification to common-mode voltage amplification.
NOTE: This is measured by determining the ratio of a change in input common-mode voltage to the resulting change in input offset voltage.

Supply Voltage Sensitivity (k_{SVS}, $\Delta V_{IO}/\Delta V_{CC}$)

The absolute value of the ratio of the change in input offset voltage to the change in supply voltages producing it.
NOTES: 1. Unless otherwise noted, both supply voltages are varied symmetrically.
2. This is the reciprocal of supply voltage rejection ratio.

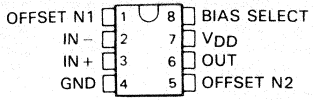
Supply Voltage Rejection Ratio (k_{SVR}, $\Delta V_{CC}/\Delta V_{IO}$)

The absolute value of the ratio of the change in supply voltages to the change in input offset voltage.
NOTES: 1. Unless otherwise noted, both supply voltages are varied symmetrically.
2. This is the reciprocal of supply voltage sensitivity.

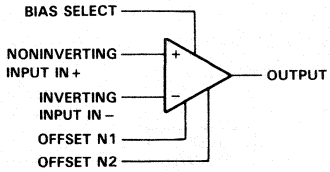
D2751, JULY 1983–REVISED OCTOBER 1987

- **Wide Range of Supply Voltages 1.4 V to 16 V**
- **True Single-Supply Operation**
- **Common-Mode Input Voltage Range Includes the Negative Rail**
- **Low Noise . . . 30 nV $\sqrt{Hz}$ Typ at 1 kHz (High Bias)**

D, JG, OR P PACKAGE
(TOP VIEW)



symbol



description

The TLC251C, TLC251AC, and TLC251BC are low-cost, low-power programmable operational amplifiers designed to operate with single or dual supplies. Unlike traditional metal-gate CMOS op amps, these devices utilize Texas Instruments silicon-gate LinCMOS™ process, giving them stable input offset voltages without sacrificing the advantages of metal-gate CMOS. This series of parts is available in selected grades of input offset voltage and can be nulled with one external potentiometer. Because the input common-mode range extends to the negative rail and the power consumption is extremely low, this family is ideally suited for battery-powered or energy-conserving applications. A bias-select pin can be used to program one of three ac performance and power-dissipation levels to suit the application. The series features guaranteed operation down to a 1.4 V supply and is stable at unity gain.

The TLC251C series is characterized for operation from 0°C to 70°C.

These devices have internal electrostatic discharge (ESD) protection circuits that will prevent catastrophic failures at voltages up to 2000 volts as tested under MIL-STD-883B, Method 3015.1. However, care should be exercised in handling these devices as exposure to ESD may result in a degradation of the device parametric performance.

Because of the extremely high input impedance and low input bias and offset currents, applications for the TLC251C series include many areas that have previously been limited to BIFET and NFET product types. Any circuit using high-impedance elements and requiring small offset errors is a good candidate for cost-effective use of these devices. Many features associated with bipolar technology are available with LinCMOS™ operational amplifiers without the power penalties of traditional bipolar devices. Remote and

DEVICE FEATURES

PARAMETER	LOW BIAS	MEDIUM BIAS	HIGH BIAS
Supply current (Typ)	10 μA	150 μA	1000 μA
Slew rate (Typ)	0.04 V/μs	0.6 V/μs	4.5 V/μs
Input offset voltage (Max)			
TLC251C	10 mV	10 mV	10 mV
TLC251AC	5 mV	5 mV	5 mV
TLC251BC	2 mV	2 mV	2 mV
Offset voltage drift (Typ)	0.1 μV/month†	0.1 μV/month†	0.1 μV/month†
Offset voltage temperature coefficient (Typ)	0.7 μV/°C	2 μV/°C	5 μV/°C
Input bias current (Typ)	1 pA	1 pA	1 pA
Input offset current (Typ)	1 pA	1 pA	1 pA

† The long-term drift value applies after the first month.

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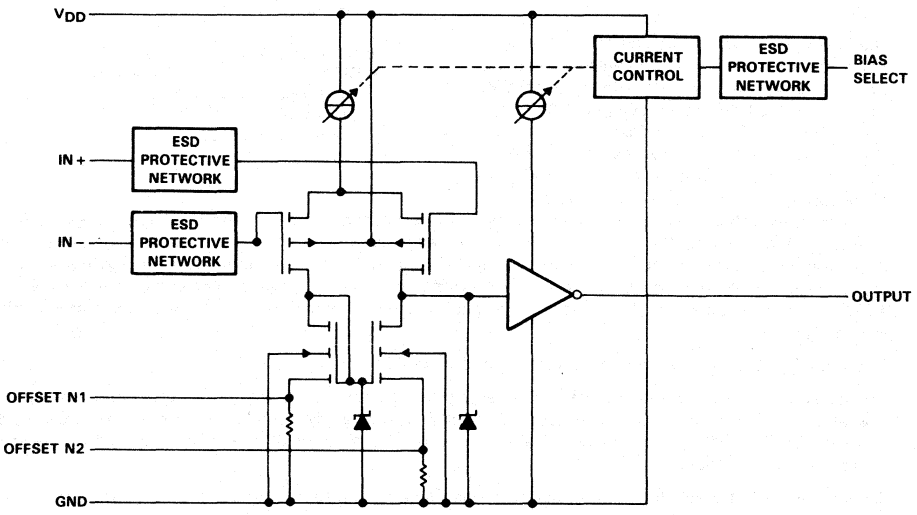
description (continued)

inaccessible equipment applications are possible using the low-voltage and low-power capabilities of the TLC251C series. In addition, by driving the bias-select input with a logic signal from a microprocessor, these operational amplifiers can have software-controlled performance and power consumption. The TLC251C series is well suited to solve the difficult problems associated with single battery and solar cell-powered applications.

schematic



absolute maximum ratings over operating free-air temperature (unless otherwise noted)

Supply voltage, V_{DD} (see Note 1) . . . . . 18 V
Differential input voltage (see Note 2) . . . . . ±18 V
Input voltage range (any input) . . . . . −0.3 V to 18 V
Duration of short-circuit at (or below) 25°C free-air temperature (see Note 3) . . . . . unlimited
Continuous total dissipation . . . . . See Dissipation Rating Table
Operating free-air temperature range . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C
Lead temperature 1,6 mm (1/16) inch from the case for 60 seconds: JG package . . . . . 300°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: D or P package . . . . . 260°C

NOTES: 1. All voltage values, except differential voltages, are with respect to network ground terminal.
2. Differential voltages are at the noninverting input terminal, with respect to the inverting input terminal.
3. The output may be shorted to either supply. Temperature and/or supply voltages must be limited to ensure the maximum dissipation rating is not exceeded.

DISSIPATION RATING TABLE

PACKAGE	POWER RATING	DERATING FACTOR	ABOVE T_A
D	725 mW	5.8 mW/°C	25°C
JG (glass mounted)	825 mW	6.6 mW/°C	25°C
P	1000 mW	8.0 mW/°C	25°C

recommended operating conditions

		MIN	NOM	MAX	UNIT
Supply voltage, V_{DD}		1.4		16	V
Common-mode input voltage, V_{IC}	V_{DD} = 1 V	0		0.2	V
	V_{DD} = 3 V	0		3	
	V_{DD} = 10 V	−0.2		9	
	V_{DD} = 16 V	−0.2		14	
Operating free-air temperature, T_A		0		70	°C
Bias Select pin voltage		See application notes			

electrical characteristics at specified free-air temperature, V_{DD} = 10 V (unless otherwise noted)

PARAMETER			TEST CONDITIONS†		BIAS	MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage	TLC251C	V_O = 1.4 V, R_S = 50 Ω	25°C	Any			10	mV
				0°C to 70°C				12	
		TLC251AC		25°C	Any			5	
				0°C to 70°C				6.5	
		TLC251BC		25°C	Any			2	
				0°C to 70°C				3	
α_{VIO}	Average temperature coefficient of input offset voltage			0°C to 70°C	Low		0.7		μV/°C
					Medium		2		
					High		5		
I_{IO}	Input offset current		V_{IC} = 5 V, V_O = 5 V	25°C	Any		1		pA
				0°C to 70°C				300	
I_{IB}	Input bias current		V_{IC} = 5 V, V_O = 5 V	25°C	Any		1		pA
				0°C to 70°C				600	
V_{ICR}	Common-mode input voltage range			25°C	Any	−0.2 to 9			V
V_{OM}	Peak output voltage range‡		V_{ID} = 100 mV	25°C	Any	8	8.6		V
				0°C to 70°C		7.8			
A_{VD}	Large-signal differential voltage amplification		V_O = 1 to 6 V, R_S = 50 Ω	25°C	Low	30	500		V/mV
					Medium	20	280		
					High	10	40		
				0°C to 70°C	Low	25			
					Medium	15			
					High	7.5			
CMRR	Common-mode rejection ratio		V_O = 1.4 V, V_{IC} = V_{ICR} min	25°C	Any	70	88		dB
k_{SVR}	Supply voltage rejection ratio ($\Delta V_{CC}/\Delta V_{IO}$)		V_{DD} = 5 to 10 V, V_O = 1.4 V	25°C	Low	70	88		dB
					Medium	70	88		
					High	65	82		
I_{OS}	Short-circuit output current		V_O = 0, V_{ID} = 100 mV	25°C	Any		−55		mA
			V_O = V_{DD}, V_{ID} = −100 mV				15		
$I_{IH(SEL)}$	High-level input current to bias select		$V_{I(SEL)}$ = 0 V	25°C	High		10.5		μA
$I_{IL(SEL)}$	Low-level input current to bias select		$V_{I(SEL)}$ = 10 V	25°C	Low		1.3		μA
I_{DD}	Supply current		No load, V_O = 5 V, V_{IC} = 5 V	25°C	Low		10	20	μA
					Medium		150	300	
					High		1000	2000	
				0°C to 70°C	Low			30	
					Medium			400	
					High			2200	

† All characteristics are measured under open-loop conditions with zero common-mode input voltage unless otherwise specified. Unless otherwise noted, an output load resistor is connected from the output to ground and has the following values: for low bias R_L = 1 MΩ, for medium bias R_L = 100 kΩ, and for high bias R_L = 10 kΩ.

‡ The output will swing to the potential of the ground pin.

electrical characteristics at specified free-air temperature, V_{DD} = 1.4 V

PARAMETER			TEST CONDITIONS†		BIAS	MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage	TLC251C	V_O = 0.2 V, R_S = 50 Ω	25°C	Any			10	mV
				0°C to 70°C				12	
		TLC251AC		25°C	Any			5	
				0°C to 70°C				6.5	
		TLC251BC		25°C	Any			2	
				0°C to 70°C				3	
α_{VIO}	Average temperature coefficient of input offset voltage			0°C to 70°C	Any		1		μV/°C
I_{IO}	Input offset current		V_O = 0.2 V	25°C	Any		1		pA
				0°C to 70°C				300	
I_{IB}	Input bias current		V_O = 0.2 V	25°C	Any		1		pA
				0°C to 70°C				600	
V_{ICR}	Common-mode input voltage range			25°C	Any	0 to 0.2			V
V_{OM}	Peak output voltage swing‡		V_{ID} = 100 mV	25°C	Any		450		mV
A_{VD}	Large-signal differential voltage amplification		V_O = 100 to 300 mV, R_S = 50 Ω	25°C	Low		20		V/mV
					High		10		
CMRR	Common-mode rejection ratio		R_S = 50 Ω, V_O = 0.2 V, V_{IC} = V_{IC} min	25°C	Any		77		dB
I_{DD}	Supply current		V_O = 0.2 V, No load	25°C	Low		2		μA
					High		12		

† All characteristics are measured under open-loop conditions with zero common-mode input voltage unless otherwise specified. Unless otherwise noted, an output load resistor is connected from the output to ground and has the following values: for low bias R_L = 1 MΩ, for medium bias R_L = 100 kΩ, and for high bias R_L = 10 kΩ.
‡ The output will swing to the potential of the ground pin.

operating characteristics, V_{DD} = 1.4 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	BIAS	MIN	TYP	MAX	UNIT
B_1	Unity-gain bandwidth	C_L = 10 pF	Low		12		kHz
			High		75		
SR	Slew rate at unity gain	See Figure 1	Low		0.001		V/μs
			High		0.01		
	Overshoot factor	See Figure 1	Low		35%		
			High		30%		

operating characteristics, V_{DD} = 10 V, T_A = 25°C

PARAMETER	TEST CONDITIONS	BIAS	MIN	TYP	MAX	UNIT
B_1 Unity-gain bandwidth	A_V = 40 dB, C_L = 10 pF, R_S = 50Ω	Low		0.1		MHz
		Medium		0.7		
		High		2.3		
SR Slew rate at unity gain	See Figure 1	Low		0.04		V/μs
		Medium		0.6		
		High		4.5		
Overshoot factor	See Figure 1	Low		30%		
		Medium		35%		
		High		35%		
ϕ_m Phase margin at unity gain	A_V = 40 dB, R_S = 100 Ω, C_L = pF	Low		43°		
		Medium		43°		
		High		50°		
V_n Equivalent input noise voltage	f = 1 kHz, R_S = 100 Ω	Low		70		nV/√Hz
		Medium		38		
		High		30		

PARAMETER MEASUREMENT INFORMATION

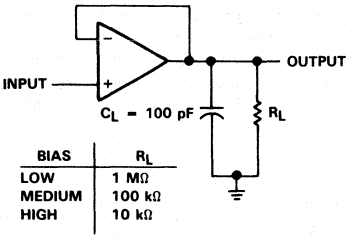


FIGURE 1. UNITY-GAIN AMPLIFIER

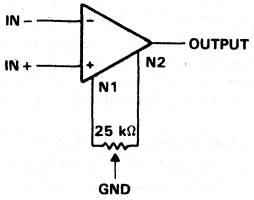


FIGURE 2. INPUT OFFSET VOLTAGE NULL CIRCUIT

TYPICAL CHARACTERISTICS

SUPPLY CURRENT
vs
BIAS SELECT PIN VOLTAGE

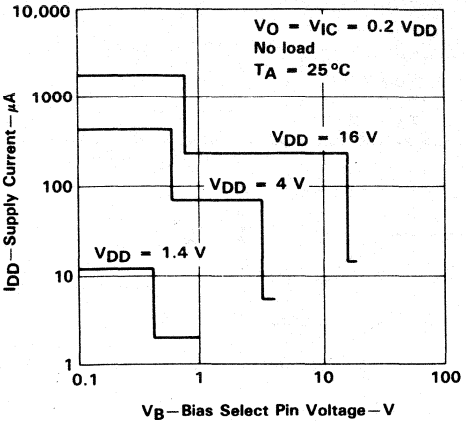


FIGURE 3

SUPPLY CURRENT
vs
SUPPLY VOLTAGE

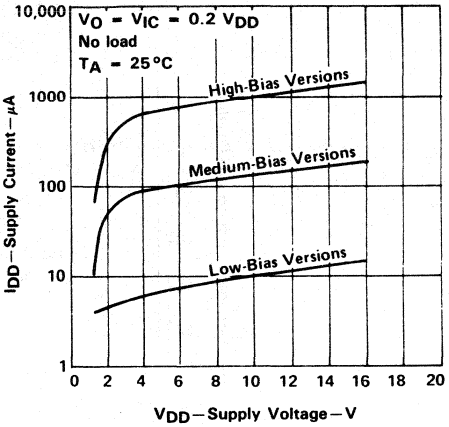


FIGURE 4

SUPPLY CURRENT
vs
FREE-AIR TEMPERATURE

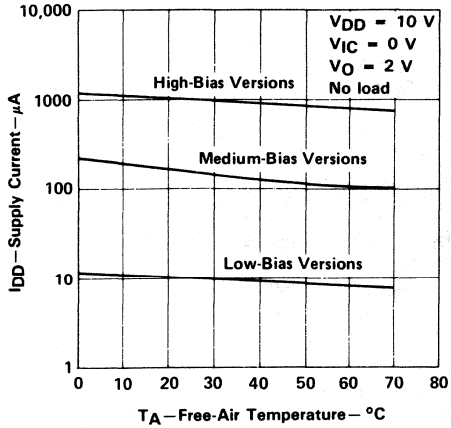


FIGURE 5

LOW BIAS
LARGE-SIGNAL
DIFFERENTIAL VOLTAGE AMPLIFICATION
and PHASE SHIFT
vs
FREQUENCY

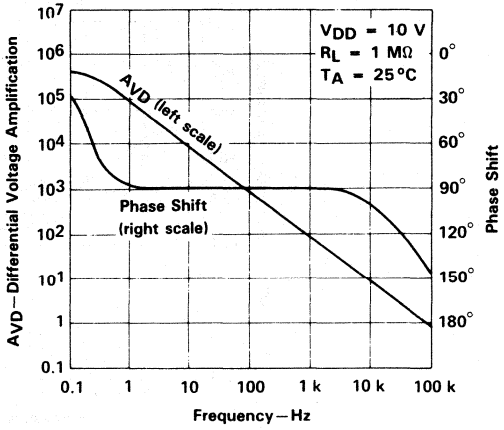


FIGURE 6

TYPICAL CHARACTERISTICS

MEDIUM BIAS
LARGE-SIGNAL
DIFFERENTIAL VOLTAGE AMPLIFICATION
and PHASE SHIFT
vs
FREQUENCY

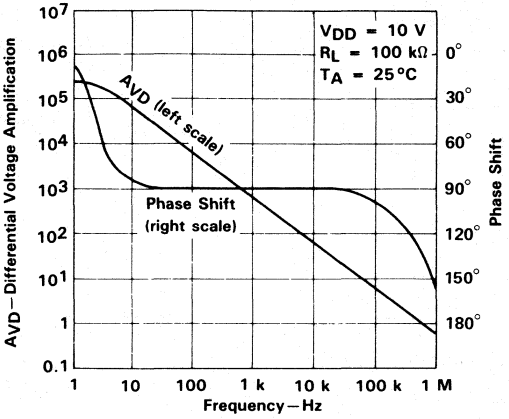


FIGURE 7

HIGH BIAS
LARGE-SIGNAL
DIFFERENTIAL VOLTAGE AMPLIFICATION
and PHASE SHIFT
vs
FREQUENCY

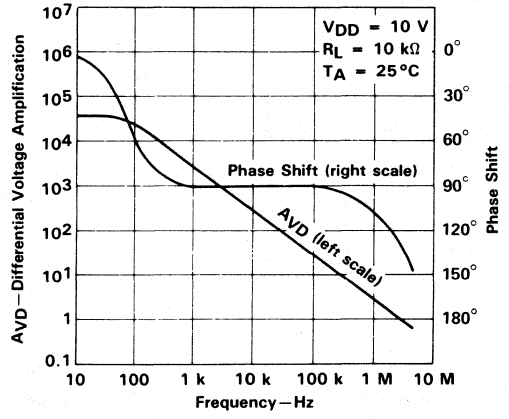


FIGURE 8

TYPICAL APPLICATION INFORMATION

latchup avoidance

Junction-isolated CMOS circuits have an inherent parasitic PNPN structure that can function as an SCR. Under certain conditions, this SCR may be triggered into a low-impedance state, resulting in excessive supply current. To avoid such conditions, no voltage greater than 0.3 V beyond the supply rails should be applied to any pin. In general, the op amp supplies should be applied simultaneously with, or before, application of any input signals.

using the bias select pin

The TLC251C series has a bias select pin that allows the selection of one of three I_{DD} conditions (10, 150, and 1000 μA typical). This allows the user to trade-off power and ac performance. As shown in the typical supply current (I_{DD}) versus supply voltage (V_{DD}) curves (Figure 4), the I_{DD} varies only slightly from 4 to 16 V. Below 4 V, the I_{DD} varies more significantly. Note that the I_{DD} values in the medium and low-bias modes at V_{DD} = 1.4 V are typically 2 μA, and in the high mode are typically 12 μA. The following table shows the recommended bias select pin connections at V_{DD} = 10 V:

BIAS MODE	AC PERFORMANCE	BIAS SELECT CONNECTION†	TYPICAL I_{DD}‡
Low	Low	V_{DD}	10 μA
Medium	Medium	0.8 V to 9.2 V	150 μA
High	High	Ground pin	1000 μA

†The Bias Select pin may also be controlled by external circuitry to conserve power, etc. For information regarding the bias select pin, see Figure 3 in the typical characteristics curves.
‡For I_{DD} characteristics at voltages other than 10 V, see Figure 4 in the typical characteristics curves.

output stage considerations

The amplifier's output stage consists of a source-follower-connected pullup transistor and an open-drain pulldown transistor. The high-level output voltage (V_{OH}) is virtually independent of the I_{DD} selection, and increases with higher values of V_{DD} and reduced output loading. The low-level output voltage (V_{OL}) decreases with reduced output current and higher input common-mode voltage. With no load, V_{OL} is essentially equal to the GND pin potential.

input offset nulling

The TLC251C series offers external offset null control. Nulling may be achieved by adjusting a 25-kΩ potentiometer connected between the offset null terminals with the wiper connected to the device GND pin as shown in Figure 2. The amount of nulling range varies with the bias selection. At I_{DD} settings of 150 and 1000 μA (medium and high bias), the nulling range will allow the maximum offset specified to be trimmed to zero. In low bias or when the amplifier is used below 4 V, total nulling may not be possible on all units.

supply configurations

Even though the TLC251C series is characterized for single-supply operation, it can be used effectively in a split-supply configuration when the input common-mode voltage (V_{ICR}), output swing (V_{OL} and V_{OH}), and supply voltage limits are not exceeded.

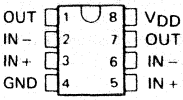
circuit layout precautions

The user is cautioned that when ever extremely high circuit impedances are used, care must be exercised in layout, construction, board cleanliness, and supply filtering to avoid hum and noise pickup, as well as excessive dc leakages.

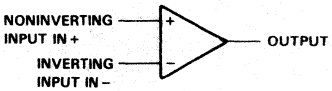
D2752, JUNE 1983 - REVISED OCTOBER 1987

- A Suffix Versions Offer 5-mV V_{IO}
- B Suffix Versions Offer 2-mV V_{IO}
- Wide Range of Supply Voltages 1.4 V to 16 V
- True Single-Supply Operation
- Common-Mode Input Voltage Includes the Negative Rail
- Low Noise . . . 30 $nV/\sqrt{Hz}$ Typ at f = 1 kHz (High-Bias Versions)

D, JG, OR P PACKAGE
(TOP VIEW)



symbol (each amplifier)



description

The TLC252C, TLC25L2C, and TLC25M2C are low-cost, low-power dual operational amplifiers designed to operate with single or dual supplies. These devices utilize the Texas Instruments silicon gate LinCMOS™ process, giving them stable input offset voltages that are available in selected grades of 2, 5 or 10 mV maximum, very high input impedances, and extremely low input offset and bias currents. Because the input common-mode range extends to the negative rail and the power consumption is extremely low, this series is ideally suited for battery-powered or energy-conserving applications. The series offers guaranteed operation down to a 1.4-V supply, is stable at unity gain, and has excellent noise characteristics.

The TLC252C series is characterized for operation from 0°C to 70°C

These devices have internal electrostatic discharge (ESD) protection circuits that will prevent catastrophic failures at voltages up to 2000 volts as tested under MIL-STD-883B, Method 3015.1. However, care should be exercised in handling these devices as exposure to ESD may result in a degradation of the device parametric performance.

Because of the extremely high input impedance and low input bias and offset currents, applications for the TLC252C series include many areas that have previously been limited to BIFET and NFET product types. Any circuit using high-impedance elements and requiring small offset errors is a good candidate for cost-effective use of these devices. Many features associated with bipolar technology are available with LinCMOS™ operational amplifiers without the power penalties of traditional bipolar devices. General applications such as transducer interfacing, analog calculations, amplifier blocks, active filters, and signal buffering are all easily designed with the TLC252C series devices. Remote and inaccessible equipment

DEVICE FEATURES

PARAMETER	TLC25L2C (LOW BIAS)	TLC25M2C (MEDIUM BIAS)	TLC252C (HIGH BIAS)
Supply current (Typ)	20 μA	300 μA	2000 μA
Slew rate (Typ)	0.04 V/μs	0.6 V/μs	4.5 V/μs
Input offset voltage (Max)			
TLC252C, TLC25L2C, TLC25M2C	10 mV	10 mV	10 mV
TLC252AC, TLC25L2AC, TLC25M2AC	5 mV	5 mV	5 mV
TLC252BC, TLC25L2BC, TLC25M2BC	2 mV	2 mV	2 mV
Offset voltage drift (Typ)	0.1 μV/month†	0.1 μV/month†	0.1 μV/month†
Offset voltage temperature coefficient (Typ)	0.7 μV/°C	2 μV/°C	5 μV/°C
Input bias current (Typ)	1 pA	1 pA	1 pA
Input offset current (Typ)	1 pA	1 pA	1 pA

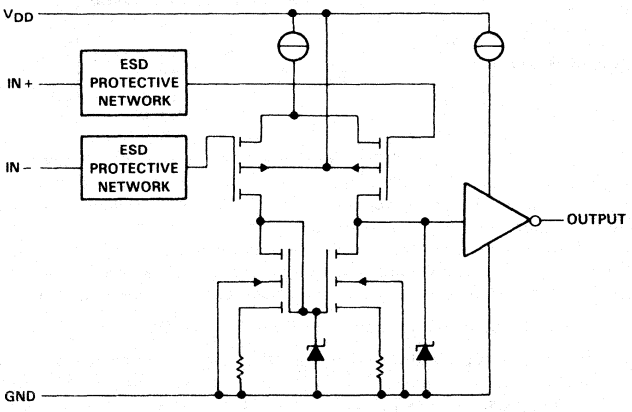
† The long-term drift value applies after the first month.

LinCMOS is a trademark of Texas Instruments Incorporated

description (continued)

applications are possible using their low-voltage and low-power capabilities. The TLC252C series is well suited to solve the difficult problems associated with single-battery and solar-cell-powered applications. This series includes devices that are characterized for the commercial temperature range and are available in 8-pin plastic and ceramic dual-in-line (DIP) packages and the small outline (D) package.

schematic (each amplifier)



absolute maximum ratings over operating free-air temperature (unless otherwise noted)

Supply voltage, V_{DD} (see Note 1) . . . . . 18 V
Differential input voltage (see Note 2) . . . . . ±18 V
Input voltage range (any input) . . . . . −0.3 V to 18 V
Duration of short-circuit at (or below) 25°C free-air temperature (see Note 3) . . . . . unlimited
Continuous total dissipation . . . . . See Dissipation Rating Table
Operating free-air temperture range . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C
Lead temperature 1,6 mm (1/16) inch from the case for 60 seconds: JG package . . . . . 300°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: D or P package . . . . . 260°C

NOTES: 1. All voltage values, except differential voltages, are with respect to network ground terminal.
2. Differential voltages are at the noninverting input terminal, with respect to the inverting input terminal.
3. The output may be shorted to either supply. Temperature and/or supply voltages must be limited to ensure the maximum dissipation rating is not exceeded.

DISSIPATION RATING TABLE

PACKAGE	POWER RATING	DERATING FACTOR	ABOVE T_A
D	725 mW	5.8 mW/°C	25°C
JG (glass mounted)	825 mW	6.6 mW/°C	25°C
P	1000 mW	8.0 mW/°C	25°C

recommended operating conditions

		MIN	NOM	MAX	UNIT
Supply voltage, V_{DD}		1.4		16	V
Common-mode input voltage, V_{IC}	V_{DD} = 1 V	0		0.2	V
	V_{DD} = 3 V	0		3	
	V_{DD} = 10 V	−0.2		9	
	V_{DD} = 16 V	−0.2		14	
Operating free-air temperature, T_A		0		70	°C

electrical characteristics at specified free-air temperature, V_{DD} = 10 V (unless otherwise noted)

PARAMETER			TEST CONDITIONS†		TLC252_C			TLC25L2_C			TLC25M2_C			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
V_O	Input offset voltage	TLC25_2C	V_O = 1.4 V, R_S = 50 Ω	25°C			10			10			10	mV
				0°C to 70°C			12			12			12	
		TLC25_2AC		25°C			5			5			5	
				0°C to 70°C			6.5			6.5			6.5	
		TLC25_2BC		25°C			2			2			2	
				0°C to 70°C			3			3			3	
αV_{IO}	Average temperature coefficient of input offset voltage			0°C to 70°C		5			0.7			2		μV/°C
I_{IO}	Input offset current		V_{IC} = 5 V, V_O = 5 V	25°C		1			1			1		pA
				0°C to 70°C			300			300			300	
I_{IB}	Input bias current		V_{IC} = 5 V, V_O = 5 V	25°C		1			1			1		pA
				0°C to 70°C			600			600			600	
V_{ICR}	Common-mode input voltage range			25°C	−0.2 to 9			−0.2 to 9			−0.2 to 9			V
V_{OM}	Peak output voltage swing‡		V_{ID} = 100 mV	25°C	8	8.6		8	8.6		8	8.6		V
				0°C to 70°C	7.8			7.8			7.8			
A_{VD}	Large-signal differential voltage amplification		V_O = 1 to 6 V, R_S = 50 Ω	25°C	10	40		30	500		20	280		V/mV
				0°C to 70°C	7.5			25			15			
CMRR	Common-mode rejection ratio		V_O = 1.4 V, V_{IC} = V_{ICR} min	25°C	70	88		70	88		70	88		dB
k_{SVR}	Supply voltage rejection ratio ($\Delta V_{CC}/\Delta V_{IO}$)		V_{DD} = 5 to 10 V, V_O = 1.4 V	25°C	65	82		70	88		70	88		dB
I_{OS}	Short-circuit output current		V_O = 0, V_{ID} = 100 mV	25°C		−55			−55			−55		mA
			V_O = V_{DD}, V_{ID} = −100 mV			15			15			15		
I_{DD}	Supply current (each amplifier)		No load, V_O = 5 V, V_{IC} = 5 V	25°C		1000	2000		10	20		150	300	μA
				0°C to 70°C			2200			30			400	

† All characteristics are measured under open-loop conditions with zero common-mode input voltage unless otherwise specified. Unless otherwise noted, an output load resistor is connected from the output to the ground pin and has the following values: For low bias R_L = 1 MΩ; for medium bias R_L = 100 kΩ; and for high bias R_L = 10 kΩ.

‡ The output will swing to the potential of the ground pin.

electrical characteristics at specified free-air temperature, V_{DD} = 1.4 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		TLC252_C			TLC25L2_C			TLC25M2_C			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage, TLC25_2C	V_O = 0.2 V, R_S = 50 Ω	25°C		10			10			10		mV
			0°C to 70°C		12			12			12		
	Input offset voltage, TLC25_2AC		25°C		5			5			5		
			0°C to 70°C		6.5			6.5			6.5		
	Input offset voltage, TLC25_2BC		25°C		2			2			2		
			0°C to 70°C		3			3			3		
α_{VIO}	Average temperature coefficient of input offset voltage		0°C to 70°C		1			1			1		μV/°C
I_{IO}	Input offset current	V_O = 0.2 V	25°C		1			1			1		pA
			0°C to 70°C		300			300			300		
I_{IB}	Input bias current	V_O = 0.2 V	25°C		1			1			1		pA
			0°C to 70°C		600			600			600		
V_{ICR}	Common mode input voltage range		25°C	0 to 0.2			0 to 0.2			0 to 0.2			V
V_{OM}	Peak output voltage swing‡	V_{ID} = 100 mV	25°C		450			450			450		mV
A_{VD}	Large signal differential voltage amplification	V_O = 100 to 300 mV, R_S = 50 Ω	25°C		10			20			20		V/mV
CMRR	Common mode rejection ratio	V_O = 0.2 V, V_{IC} = V_{ICR} min	25°C		77			77			77		dB
I_{DD}	Supply current (each amplifier)	No load, V_O = 0.2 V	25°C		12			2			2		μA

† All characteristics are measured under open loop conditions with zero common-mode input voltage unless otherwise specified. Unless otherwise noted, an output load resistor is connected from the output to the ground pin and has the following values: For low bias R_L = 1 MΩ; for medium bias R_L = 100 kΩ; and for high bias R_L = 10 kΩ.
‡ The output will swing to the potential of the ground pin.

operating characteristics, V_{DD} = 1.4 V, T_A = 25°C

TEST CONDITIONS		TEST CONDITIONS	TLC252_C			TLC25L2_C			TLC25M2_C			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
B_1	Unity-gain bandwidth	A_V = 40 dB, C_L = 10 pF, R_S = 50 Ω		75			12			12		kHz
SR	Slew rate at unity gain	See Figure 1		0.01			0.001			0.001		V/μs
	Overshoot factor	See Figure 1		30%			35%			35%		

operating characteristics, V_{DD} = 10 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	TLC252_C			TLC25L2_C			TLC25M2_C			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
B_1	Unity-gain bandwidth	A_V = 40 dB, C_L = 10 pF, R_S = 50 Ω		2.3			0.1			0.7		MHz
SR	Slew rate at unity gain	See Figure 1		4.5			0.04			0.6		V/μs
	Overshoot factor	See Figure 1		35%			30%			35%		
ϕ_m	Phase margin at unity gain	A_V = 40 dB, R_S = 100 Ω, C_L = 10 pF		50°			43°			43°		
V_n	Equivalent input noise voltage	f = 1 kHz, R_S = 100 Ω		30			70			38		$nV/\sqrt{Hz}$
V_{o1}/V_{o2}	Cross talk attenuation	A_V = 100		120			120			120		dB

PARAMETER MEASUREMENT INFORMATION

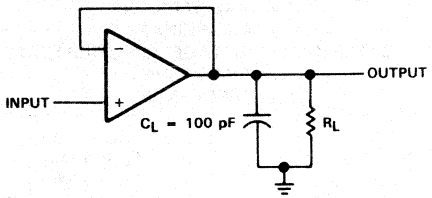


FIGURE 1. UNITY-GAIN AMPLIFIER

TYPICAL CHARACTERISTICS

SUPPLY CURRENT
vs
SUPPLY VOLTAGE

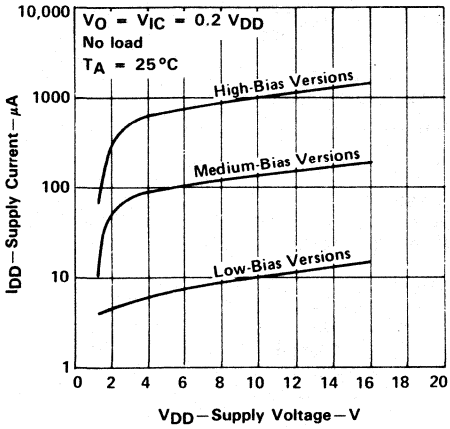


FIGURE 2

SUPPLY CURRENT
vs
FREE-AIR TEMPERATURE

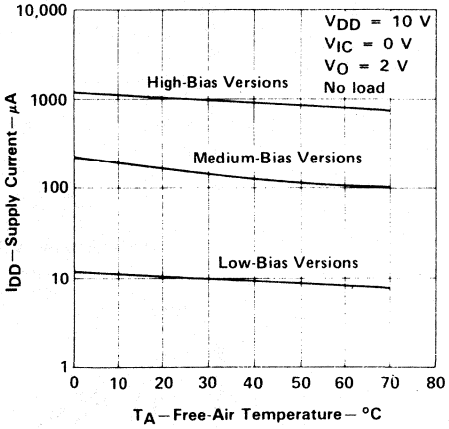


FIGURE 3

TYPICAL CHARACTERISTICS

LOW-BIAS VERSIONS
LARGE-SIGNAL
DIFFERENTIAL VOLTAGE AMPLIFICATION
and PHASE SHIFT
vs FREQUENCY

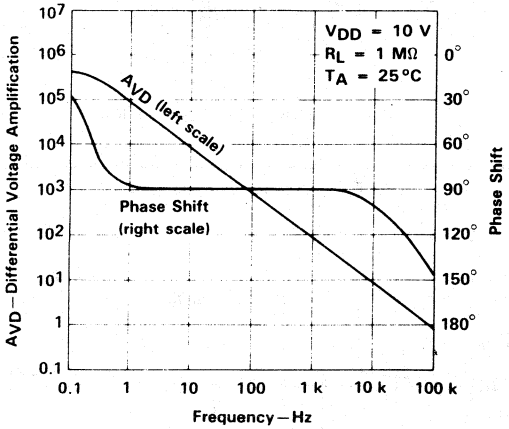


FIGURE 4

MEDIUM-BIAS VERSIONS
LARGE-SIGNAL
DIFFERENTIAL VOLTAGE AMPLIFICATION
and PHASE SHIFT
vs FREQUENCY

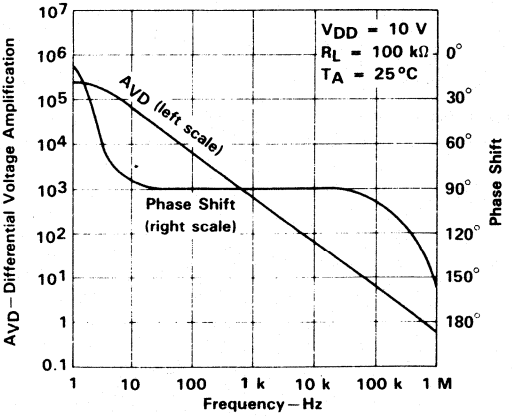


FIGURE 5

TYPICAL CHARACTERISTICS

HIGH-BIAS VERSIONS
LARGE-SIGNAL
DIFFERENTIAL VOLTAGE AMPLIFICATION
and PHASE SHIFT
vs FREQUENCY

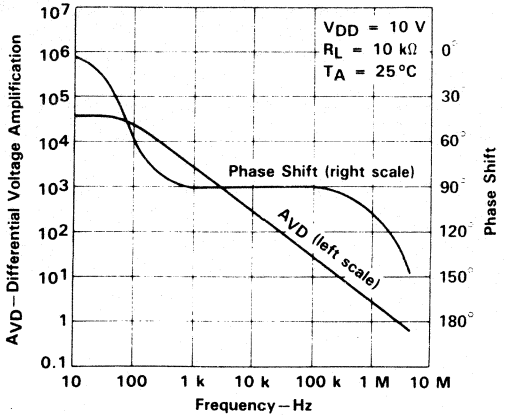


FIGURE 6

TYPICAL APPLICATION INFORMATION

latchup avoidance

Junction-isolated CMOS circuits have an inherent parasitic PNPN structure that can function as an SCR. Under certain conditions, this SCR may be triggered into a low-impedance state, resulting in excessive supply current. To avoid such conditions, no voltage greater than 0.3 V beyond the supply rails should be applied to any pin. In general, the op amp supplies should be established simultaneously with, or before, application of any input signals.

output stage considerations

The amplifier's output stage consists of a source follower connected pullup transistor and an open drain pulldown transistor. The high-level output voltage (V_{OH}) is virtually independent of the I_{DD} selection, and increases with higher values of V_{DD} and reduced output loading. The low-level output voltage (V_{OL}) decreases with reduced output current and higher input common-mode voltage. With no load, V_{OL} is essentially equal to the GND pin potential.

supply configurations

Even though the TLC252C series is characterized for single-supply operation, it can be used effectively in a split supply configuration if the input common-mode voltage (V_{ICR}), output swing (V_{OL} and V_{OH}), and supply voltage limits are not exceeded.

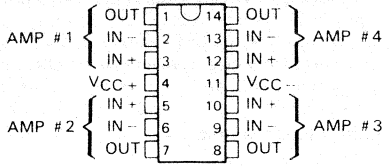
circuit layout precautions

The user is cautioned that whenever extremely high circuit impedances are used, care must be exercised in layout, construction, board cleanliness, and supply filtering to avoid hum and noise pickup, as well as excessive DC leakages.

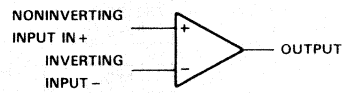
D2753, JUNE 1983 – REVISED OCTOBER 1987

- **A Suffix Versions Offer 5-mV V_{IO}**
- **B Suffix Versions Offer 2-mV V_{IO}**
- **Wide Range of Supply Voltages 1.4 V to 16 V**
- **True Single-Supply Operation**
- **Common-Mode Input Voltage Includes the Negative Rail**
- **Low Noise . . . 30 nV$\sqrt{Hz}$ Typ at f = 1 kHz (High-Bias Versions)**

D, J, OR N PACKAGE
(TOP VIEW)



symbol (each amplifier)



description

The TLC254C, TLC25L4C, and TLC25M4C are low-cost, low-power quad operational amplifiers designed to operate with single or dual supplies. These devices utilize the Texas Instruments silicon gate LinCMOS™ process, giving them stable input offset voltages that are available in selected grades of 2, 5, or 10 mV maximum, very high input impedances, and extremely low input offset and bias currents. Because the input common-mode range extends to the negative rail and the power consumption is extremely low, this series is ideally suited for battery-powered or energy-conserving applications. The series offers guaranteed operation down to a 1.4-V supply, is stable at unity gain, and has excellent noise characteristics.

The TLC254C series is characterized for operation from 0°C to 70°C

These devices have internal electrostatic discharge (ESD) protection circuits that will prevent catastrophic failures at voltages up to 2000 volts as tested under MIL-STD-883B, Method 3015.1. However, care should be exercised in handling these devices as exposure to ESD may result in a degradation of the device parametric performance.

Because of the extremely high input impedance and low input bias and offset currents, applications for the TLC254C series include many areas that have previously been limited to BIFET and NFET product types. Any circuit using high-impedance elements and requiring small offset errors is a good candidate for cost-effective use of these devices. Many features associated with bipolar technology are available with LinCMOS™ operational amplifiers without the power penalties of traditional bipolar devices. General applications such as transducer interfacing, analog calculations, amplifier blocks, active filters, and signal

DEVICE FEATURES

PARAMETER	TLC25L4C (LOW BIAS)	TLC25M4C (MEDIUM BIAS)	TLC254C (HIGH BIAS)
Supply current (Typ)	40 μA	600 μA	4000 μA
Slew rate (Typ)	0.04 V/μs	0.6 V/μs	4.5 V/μs
Input offset voltage (Max)			
TLC254C, TLC25L4C, TLC25M4C	10 mV	10 mV	10 mV
TLC254AC, TLC25L4AC, TLC25M4AC	5 mV	5 mV	5 mV
TLC254BC, TLC25L4BC, TLC25M4BC	2 mV	2 mV	2 mV
Offset voltage drift (Typ)	0.1 μV/month†	0.1 μV/month†	0.1 μV/month†
Offset voltage temperature coefficient (Typ)	0.7 μV/°C	2 μV/°C	5 μV/°C
Input bias current (Typ)	1 pA	1 pA	1 pA
Input offset current (Typ)	1 pA	1 pA	1 pA

† The long-term drift value applies after the first month.

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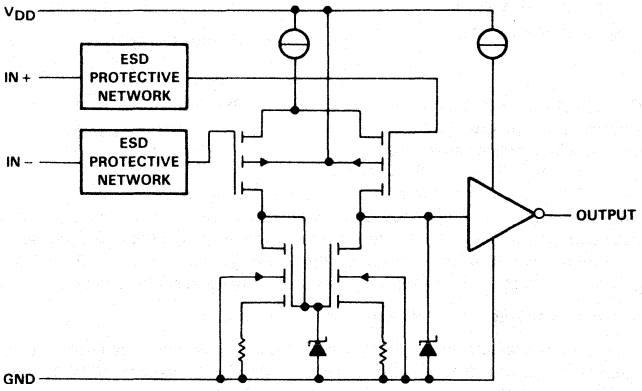
description (continued)

buffering are all easily designed with the TLC254C series devices. Remote and inaccessible equipment applications are possible using their low-voltage and low-power capabilities. The TLC254C series is well suited to solve the difficult problems associated with single-battery and solar-cell-powered applications. This series includes devices that are characterized for the commercial temperature range and are available in 14-pin plastic and ceramic dual-in-line (DIP) packages and the small outline (D) package.

schematic (each amplifier)



absolute maximum ratings over operating free-air temperature (unless otherwise noted)

Supply voltage, V_{DD} (see Note 1) . . . . . 18 V
Differential input voltage (see Note 2) . . . . . ±18 V
Input voltage range (any input) . . . . . −0.3 V to 18 V
Duration of short-circuit at (or below) 25°C free-air temperature (see Note 3) . . . . . unlimited
Continuous total dissipation . . . . . See Dissipation Rating Table
Operating free-air temperature range . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C
Lead temperature 1,6 mm (1/16) inch from the case for 60 seconds: J package . . . . . 300°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: D or N package . . . . . 260°C

NOTES: 1. All voltage values, except differential voltages, are with respect to network ground terminal.
2. Differential voltages are at the noninverting input terminal, with respect to the inverting input terminal.
3. The output may be shorted to either supply. Temperature and/or supply voltages must be limited to ensure the maximum dissipation rating is not exceeded.

DISSIPATION RATING TABLE

PACKAGE	POWER RATING	DERATING FACTOR	ABOVE T_A
D	950 mW	7.6 mW/°C	25°C
J (glass mounted)	1025 mW	8.2 mW/°C	25°C
N	1150 mW	9.2 mW/°C	25°C

recommended operating conditions

		MIN	NOM	MAX	UNIT
Supply voltage, V_{DD}		1.4		16	V
Common-mode input voltage, V_{IC}	V_{DD} = 1 V	0		0.2	V
	V_{DD} = 3 V	0		3	
	V_{DD} = 10 V	0		9	
	V_{DD} = 16 V	0		14	
Operating free-air temperature, T_A		0		70	°C

electrical characteristics at specified free-air temperature, V_{DD} = 10 V (unless otherwise noted)

PARAMETER			TEST CONDITIONS†		TLC254_C			TLC25L4_C			TLC25M4_C			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
V_O	Input offset voltage	TLC25_4C	V_O = 1.4 V, R_S = 50 Ω	25°C		10			10			10		mV
				0°C to 70°C		12			12			12		
		TLC25_4AC		25°C		5			5			5		
				0°C to 70°C		6.5			6.5			6.5		
		TLC25_4BC		25°C		2			2			2		
				0°C to 70°C		3			3			3		
αV_{IO}	Average temperature coefficient of input offset voltage			0°C to 70°C		5			0.7			2		μV/°C
I_{IO}	Input offset current		V_{IC} = 5 V, V_O = 5 V	25°C		1			1			1		pA
				0°C to 70°C			300			300			300	
I_{IB}	Input bias current		V_{IC} = 5 V, V_O = 5 V	25°C		1			1			1		pA
				0°C to 70°C			600			600			600	
V_{ICR}	Common-mode input voltage range			25°C	−0.2 to 9			−0.2 to 9			−0.2 to 9			V
V_{OM}	Peak output voltage swing‡		V_{ID} = 100 mV	25°C	8	8.6		8	8.6		8	8.6		V
				0°C to 70°C	7.8			7.8			7.8			
A_{VD}	Large-signal differential voltage amplification		V_O = 1 to 6 V, R_S = 50 Ω	25°C	10	40		30	500		20	280		V/mV
				0°C to 70°C	7.5			25			15			
CMRR	Common-mode rejection ratio		V_O = 1.4 V, V_{IC} = V_{ICR} min	25°C	70	88		70	88		70	88		dB
k_{SVR}	Supply voltage rejection ratio ($\Delta V_{CC}/\Delta V_{IO}$)		V_{DD} = 5 to 10 V, V_O = 1.4 V	25°C	65	82		70	88		70	88		dB
I_{OS}	Short-circuit output current		V_O = 0, V_{ID} = 100 mV	25°C		−55			−55			−55		mA
			V_O = V_{DD}, V_{ID} = −100 mV			15			15			15		
I_{DD}	Supply current (each amplifier)		No load, V_O = 5 V, V_{IC} = 5 V	25°C		1000	2000		10	20		150	300	μA
				0°C to 70°C			2200			30			400	

† All characteristics are measured under open-loop conditions with zero common-mode input voltage unless otherwise specified. Unless otherwise noted, an output load resistor is connected from the output to the ground pin and has the following values: For low bias R_L = 1 MΩ; for medium bias R_L = 100 kΩ; and for high bias R_L = 10 kΩ.

‡ The output will swing to the potential of the ground pin.

electrical characteristics at specified free-air temperature, V_{DD} = 1.4 V (unless otherwise noted)

PARAMETER			TEST CONDITIONS†		TLC254_C			TLC25L4_C			TLC25M4_C			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	TLC25_4C	V_O = 0.2 V, R_S = 50 Ω	25°C			10			10			10	mV
				0°C to 70°C			12			12			12	
		TLC25_4AC		25°C			5			5			5	
				0°C to 70°C			6.5			6.5			6.5	
		TLC25_4BC		25°C			2			2			2	
				0°C to 70°C			3			3			3	
α_{VIO}	Average temperature coefficient of input offset voltage			0°C to 70°C		1			1			1		μV/°C
I_{IO}	Input offset current		V_O = 0.2 V	25°C		1			1			1		pA
				0°C to 70°C			300			300			300	
I_{IB}	Input bias current		V_O = 0.2 V	25°C		1			1			1		pA
				0°C to 70°C			600			600			600	
V_{ICR}	Common-mode input voltage range			25°C	0 to 0.2			0 to 0.2			0 to 0.2			V
V_{OM}	Peak output voltage swing‡		V_{ID} = 100 mV	25°C		450			450			450		mV
A_{VD}	Large-signal differential voltage amplification		V_O = 100 to 300 mV, R_S = 50 Ω	25°C		10			20			20		V/mV
CMRR	Common-mode rejection ratio		V_O = 0.2 V, V_{IC} = V_{ICR} min	25°C		77			77			77		dB
I_{DD}	Supply current (each amplifier)		No load, V_O = 0.2 V	25°C		12			2			2		μA

† All characteristics are measured under open-loop conditions with zero common-mode input voltage unless otherwise specified. Unless otherwise noted, an output load resistor is connected from the output to the ground pin and has the following values: For low bias R_L = 1 MΩ; for medium bias R_L = 100 kΩ; and for high bias R_L = 10 kΩ.

‡ The output will swing to the potential of the ground pin.

operating characteristics, V_{DD} = 1.4 V, T_A = 25°C

TEST CONDITIONS		TEST CONDITIONS	TLC254_C			TLC25L4_C			TLC25M4_C			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
B_1	Unity-gain bandwidth	A_V = 40 dB, C_L = 10 pF, R_S = 50 Ω		75			12			12		kHz
SR	Slew rate at unity gain	See Figure 1		0.01			0.001			0.001		V/μs
	Overshoot factor	See Figure 1		30%			35%			35%		

operating characteristics, V_{DD} = 10 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	TLC254_C			TLC25L4_C			TLC25M4_C			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
B_1	Unity-gain bandwidth	A_V = 40 dB, C_L = 10 pF, R_S = 50 Ω		2.3			0.1			0.7		MHz
SR	Slew rate at unity gain	See Figure 1		4.5			0.04			0.6		V/μs
	Overshoot factor	See Figure 1		35%			30%			35%		
ϕ_m	Phase margin at unity gain	A_V = 40 dB, R_S = 100 Ω, C_L = 10 pF		50°			43°			43°		
V_n	Equivalent input noise voltage	f = 1 kHz, R_S = 100 Ω		30			70			38		$nV/\sqrt{Hz}$
V_{o1}/V_{o2}	Cross talk attenuation	A_V = 100		120			120			120		dB

PARAMETER MEASUREMENT INFORMATION

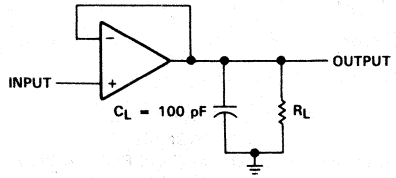


FIGURE 1. UNITY-GAIN AMPLIFIER

TYPICAL CHARACTERISTICS

SUPPLY CURRENT
vs
SUPPLY VOLTAGE

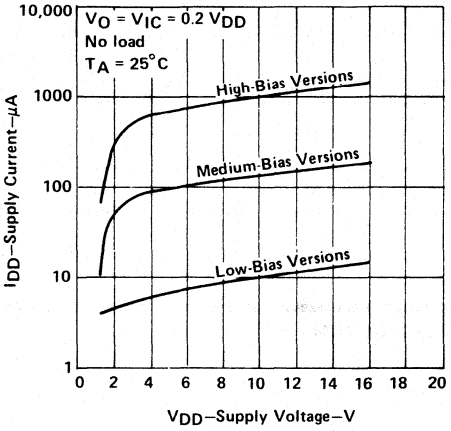


FIGURE 2

SUPPLY CURRENT
vs
FREE-AIR TEMPERATURE

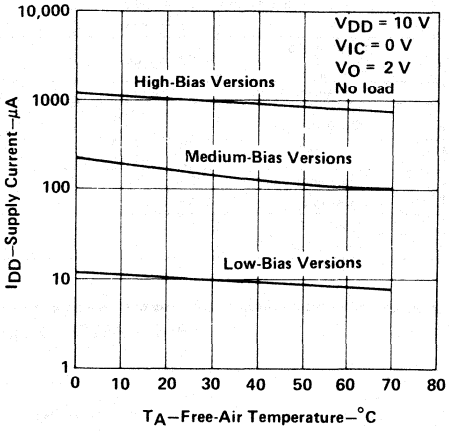


FIGURE 3

LOW-BIAS VERSIONS
LARGE-SIGNAL
DIFFERENTIAL VOLTAGE AMPLIFICATION
and PHASE SHIFT
vs
FREQUENCY

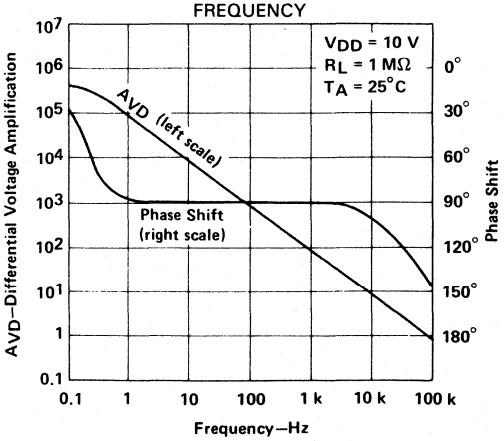


FIGURE 4

TYPICAL CHARACTERISTICS

MEDIUM-BIAS VERSIONS
LARGE-SIGNAL
DIFFERENTIAL VOLTAGE AMPLIFICATION
and PHASE SHIFT
vs
FREQUENCY

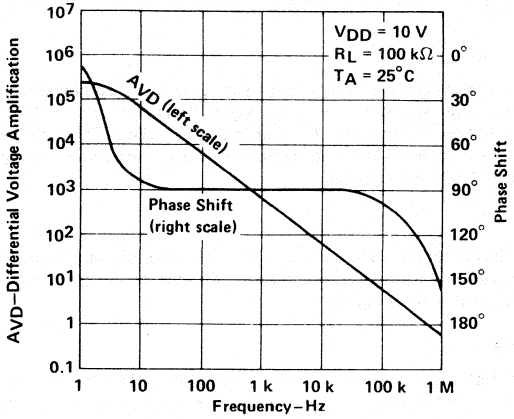


FIGURE 5

HIGH-BIAS VERSIONS
LARGE-SIGNAL
DIFFERENTIAL VOLTAGE AMPLIFICATION
and PHASE SHIFT
vs
FREQUENCY

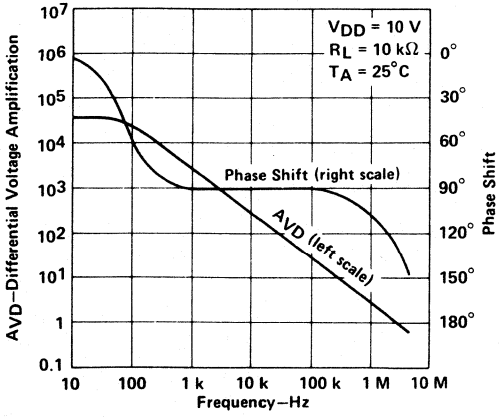


FIGURE 6

TYPICAL APPLICATION INFORMATION

latchup avoidance

Junction-isolated CMOS circuits have an inherent parasitic PNPN structure that can function as an SCR. Under certain conditions, this SCR may be triggered into a low-impedance state, resulting in excessive supply current. To avoid such conditions, no voltage greater than 0.3 V beyond the supply rails should be applied to any pin. In general, the op amp supplies should be established simultaneously with, or before, application of any input signals.

output stage considerations

The amplifier's output stage consists of a source follower connected pullup transistor and an open drain pulldown transistor. The high-level output voltage (V_{OH}) is virtually independent of the I_{DD} selection, and increases with higher values of V_{DD} and reduced output loading. The low-level output voltage (V_{OL}) decreases with reduced output current and higher input common-mode voltage. With no load, V_{OL} is essentially equal to the GND pin potential.

supply configurations

Even though the TLC254C series is characterized for single-supply operation, it can be used effectively in a split supply configuration if the input common-mode voltage (V_{ICR}), output swing (V_{OL} and V_{OH}), and supply voltage limits are not exceeded.

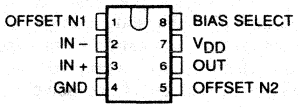
circuit layout precautions

The user is cautioned that whenever extremely high circuit impedances are used, care must be exercised in layout, construction, board cleanliness, and supply filtering to avoid hum and noise pickup, as well as excessive DC leakages.

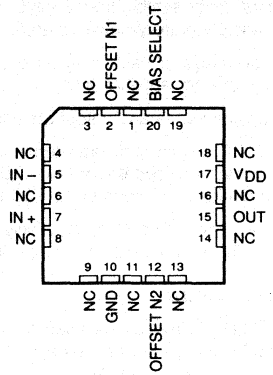
NOVEMBER 1987

- **Input Offset Voltage Drift Typically 0.1 μV / Month, Including the First 30 Days**
- **Wide Range of Supply Voltages over Specified Temperature Range:**
  – 55°C to125°C ... 4 V to 16 V
  – 40°C to 85°C ... 4 V to 16 V
  0°C to 70°C ... 3 V to 16 V
- **Single-Supply Operation**
- **Common-Mode Input Voltage Range Extends Below the Negative Rail (C- suffix, I- suffix types)**
- **Low Noise ... 25 nV $\sqrt{Hz}$ Typically at f = 1 kHz (High-Bias Mode)**
- **Output Voltage Range Includes Negative Rail**
- **High Input Impedance ... 10^{12} Ω Typical**
- **ESD Protection Circuitry**
- **Small-Outline Package Option Also Available in Tape-and-Reel**
- **Designed-in Latchup Immunity**

JG AND P DUAL-IN-LINE PACKAGE
D SMALL-OUTLINE PACKAGE
(TOP VIEW)



FK CHIP CARRIER PACKAGE
(TOP VIEW)



NC – No internal connection

description

The TLC271 operational amplifier combines a wide range of input offset voltage grades with low offset voltage drift and high input impedance. In addition, the TLC271 offers a bias select mode which allows the user to select the best combination of power dissipation and AC performance for a particular application. These devices use Texas Instruments silicon-gate LinCMOS technology, which provides offset voltage stability far exceeding the stability available with conventional metal-gate processes.

T_A	V_{IO}max at 25°C	PACKAGE			
		Small-Outline (D) See Note 1	Plastic DIP (P)	Ceramic DIP (JG)	Chip Carrier (FK)
0°C to 70°C	2 mV	TLC271BCD	TLC271BCP	TLC271BCJG	—
	5 mV	TLC271ACD	TLC271ACP	TLC271ACJG	—
	10 mV	TLC271CD	TLC271CP	TLC271CJG	—
– 40°C to 85°C	2 mV	TLC271BID	TLC271BIP	TLC271BIJG	—
	5 mV	TLC271AID	TLC271AIP	TLC271AIJG	—
	10 mV	TLC271ID	TLC271IP	TLC271IJG	—
– 55°C to 125°C	10 mV	—	—	TLC271MJG	TLC271MFK

NOTE 1: Available in tape-and-reel. Add "R" suffix to the device type when ordering (e.g., TLC271CDR).

DEVICE FEATURES Typical at V_{DD} = 5 V, T_A = 25°C				
	BIAS-SELECT MODE			UNIT
	HIGH	MEDIUM	LOW	
P_D	3375	525	50	μW
SR	3.6	0.4	0.03	V/μs
V_n	25	32	68	nV/$\sqrt{Hz}$
B_1	1.7	0.5	0.09	MHz
A_{VD}	23	170	480	V/mV

LinCMOS is a trademark of Texas Instruments Incorporated

description (continued)

Using the bias select option, these cost-effective devices can be "programmed" to span a wide range of applications which previously required BiFET, NFET or bipolar technology. Three offset voltage grades are available (C- suffix and I- suffix types), ranging from the low-cost TLC271 (10mV) to the TLC271B (2mV) low-offset version. The extremely high input impedance and low bias currents, in conjunction with good common-mode rejection and supply voltage rejection, make these devices a good choice for new state-of-the-art designs as well as for upgrading existing designs.

In general, many features associated with bipolar technology are available in LinCMOS operational amplifiers, without the power penalties of bipolar technology. General applications such as transducer interfacing, analog calculations, amplifier blocks, active filters, and signal buffering are all easily designed with the TLC271. The devices also exhibit low voltage single-supply operation, making them ideally suited for remote and inaccessible battery-powered applications. The common-mode input voltage range includes the negative rail.

A wide range of packaging options is available, including small-outline and chip carrier versions for high-density system applications.

The device inputs and output are designed to withstand – 100-mA surge currents without sustaining latchup.

The TLC271 incorporates internal ESD protection circuits that will prevent functional failures at voltages up to 2000 V as tested under MIL-STD-883C, Method 3015.2; however, care should be exercised in handling these devices as exposure to ESD may result in the degradation of the device parametric performance.

The M- suffix devices are characterized for operation over the full military temperature range of – 55°C to 125°C, the I- suffix devices from – 40°C to 85°C, and the C- suffix devices from 0°C to 70°C.

bias select feature

The TLC271 offers a bias select feature which allows the user to select any one of three bias levels, depending on the level of performance desired. The trade-offs between bias levels involve AC performance and power dissipation (see Figure 1).

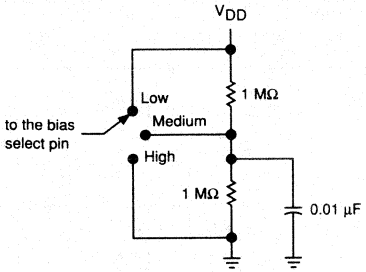
TYPICAL PARAMETER VALUES T_A = 25°C, V_{DD} = 5 V		MODE			UNITS
		HIGH-BIAS R_L = 10 kΩ	MEDIUM-BIAS R_L = 100 kΩ	LOW-BIAS R_L = 1 MΩ	
P_D	Power dissipation	3.4	0.5	0.05	mW
SR	Slew rate	3.6	0.4	0.03	V/μs
V_n	Equivalent input noise voltage at f = 1 kHz	25	32	68	nV/√Hz
B_1	Unity-gain bandwidth	1.7	0.5	0.09	MHz
ϕ_m	Phase margin	46°	40°	34°	
A_{VD}	Large-signal differential voltage amplification	23	170	480	V/mV

FIGURE 1. EFFECT OF BIAS SELECTION ON PERFORMANCE

bias selection

Bias selection is achieved by connecting the bias select pin to one of three voltage levels (see Figure 2). For medium-bias applications, it is recommended that the bias select pin be connected to the mid-point between the supply rails. This is a simple procedure in split-supply applications, since this point is ground. In single-supply applications, the medium-bias mode will necessitate using a voltage divider as indicated in Figure 2. The use of large-value resistors in the voltage divider will reduce the current drain of the divider from the supply line. However, large-value resistors used in conjunction with a large-value capacitor will require significant time to charge up to the supply midpoint after the supply is switched on. A voltage other than the mid-point may be used if it is within the voltages specified in the following table.

bias selection (continued)



BIAS MODE	BIAS SELECT VOLTAGE (Single Supply)
LOW	V_{DD}
MEDIUM	1 V to V_{DD} – 1 V
HIGH	GND

FIGURE 2. BIAS SELECTION FOR SINGLE-SUPPLY APPLICATIONS

high-bias mode

In the high-bias mode, the TLC271 series features low offset voltage drift, high input impedance, and low noise. Speed in this mode approaches that of BiFET devices, but at only a fraction of the power dissipation. Unity-gain bandwidth is typically greater than 1 MHz.

medium-bias mode

The TLC271 in the medium-bias mode features low offset voltage drift, high input impedance, and low noise. Speed in this mode is similar to general-purpose bipolar devices, but power dissipation is only a fraction of that consumed by bipolar devices.

low-bias mode

In the low-bias mode, the TLC271 features low offset voltage drift, high input impedance, extremely low power consumption, and high differential voltage gain.

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TOPIC	BIAS-MODE	PAGE
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	Low	40
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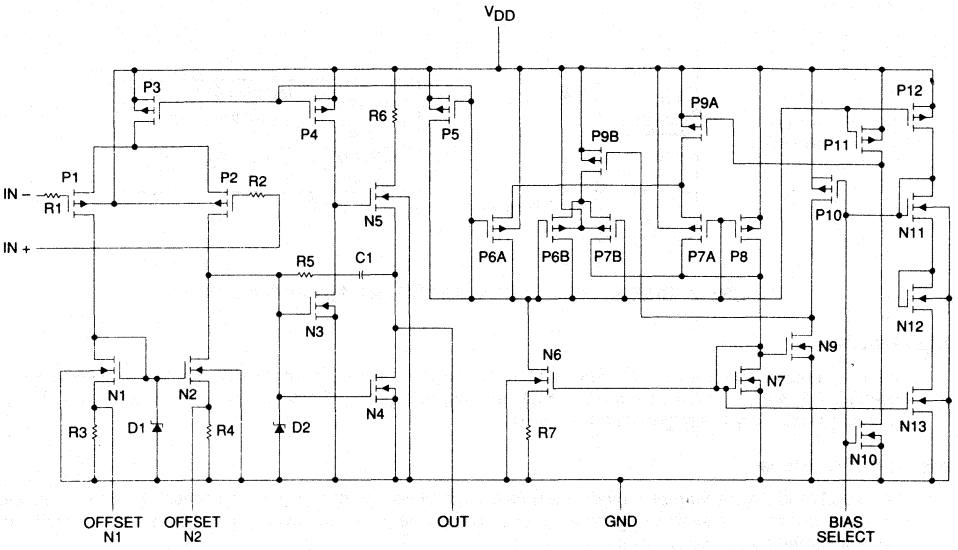
equivalent schematic



absolute maximum ratings over operating free-air temperature (unless otherwise noted)

Supply voltage, V_{DD} (see Note 2)	18 V
Differential input voltage (see Note 3)	± V_{DD}
Input voltage range, V_I (any input)	− 0.3 V to V_{DD}
Input current, I_I	± 5 mA
Output current, I_O	± 30 mA
Duration of short-circuit current at (or below) 25°C (see Note 4)	Unlimited
Continuous total dissipation	See Dissipation Rating Table
Operating free-air temperature, T_A: C-suffix types	0°C to 70°C
I-suffix types	− 40°C to 85°C
M-suffix types	− 55°C to 125°C
Storage temperature range	− 65°C to 150°C
Case temperature for 60 seconds: FK package	260°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds: JG package	300°C
Lead temperature 1,6mm (1/16 inch) from case for 10 seconds: D and P package	260°C

NOTES: 2. All voltage values, except differential voltages, are with respect to network ground.
3. Differential voltages are at the noninverting input with respect to the inverting input.
4. The output may be shorted to either supply. Temperature and/or supply voltages must be limited to ensure that the maximum dissipation rating is not exceeded (see application section).

DISSIPATION RATING TABLE

PACKAGE	$T_A \leq 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING	$T_A = 85°C$ POWER RATING	$T_A = 125°C$ POWER RATING
D	725 mW	5.8 mW/°C	464 mW	377 mW	
FK	1375 mW	11 mW/°C	880 mW	715 mW	275 mW
JG (C-, I- suffix)	825 mW	6.6 mW/°C	528 mW	429 mW	
JG (M- suffix)	1050 mW	8.4 mW/°C	672 mW	546 mW	210 mW
P	1000 mW	8.0 mW/°C	640 mW	520 mW	

recommended operating conditions

		M- SUFFIX TYPES			I- SUFFIX TYPES			C- SUFFIX TYPES			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{DD}		4		16	4		16	3		16	V
Common-mode input voltage, V_{IC}	$V_{DD} = 5$ V	0		3.5	−0.2		3.5	−0.2		3.5	V
	$V_{DD} = 10$ V	0		8.5	−0.2		8.5	−0.2		8.5	V
Input voltage, V_I	$V_{DD} = 5$ V	0		3.5	−0.2		3.5	−0.2		3.5	V
	$V_{DD} = 10$ V	0		8.5	−0.2		8.5	−0.2		8.5	V
Operating free-air temperature, T_A		−55		125	−40		85	0		70	°C

HIGH-BIAS MODE

electrical characteristics over recommended free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS		C- SUFFIX TYPES V_{DD} = 5 V MIN	TYP	MAX	C- SUFFIX TYPES V_{DD} = 10 V MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage	TLC271C	V_O = 1.4 V, V_{IC} = 0 V, R_S = 50 Ω, R_L = 10 kΩ	25°C		1.1	10		1.1	10	mV
				Full range			12			12	
		TLC271AC		25°C		0.9	5		0.9	5	
				Full range			6.5			6.5	
		TLC271BC		25°C		0.34	2		0.39	2	
				Full range			3			3	
α_{VIO}	Average temperature coefficient of input offset voltage			25°C to 70°C		1.8			2		μV/°C
I_{IO}	Input offset current (see Note 5)		$V_O = V_{DD}/2$, $V_{IC} = V_{DD}/2$	25°C		0.1			0.1		pA
				70°C		7	300		8	300	
I_{IB}	Input bias current (see Note 5)		$V_O = V_{DD}/2$, $V_{IC} = V_{DD}/2$	25°C		0.6			0.7		pA
				70°C		40	600		50	600	
V_{ICR}	Common-mode input voltage range (see Note 6)			25°C	−0.2 to 4	−0.3 to 4.2		−0.2 to 9	−0.3 to 9.2		V
				Full range	−0.2 to 3.5			−0.2 to 8.5			V
V_{OH}	High-level output voltage		V_{ID} = 100 mV, R_L = 10 kΩ	25°C	3.2	3.8		8	8.5		V
				70°C	3	3.8		7.8	8.4		
				0°C	3	3.8		7.8	8.5		
V_{OL}	Low-level output voltage		V_{ID} = −100 mV, I_{OL} = 0	25°C		0	50		0	50	mV
				70°C		0	50		0	50	
				0°C		0	50		0	50	
A_{VD}	Large-signal differential voltage amplification		R_L = 10 kΩ, See Note 7	25°C	5	23		10	36		V/mV
				70°C	4	20		7.5	32		
				0°C	4	27		7.5	42		
CMRR	Common-mode rejection ratio		$V_{IC} = V_{ICR}$min	25°C	65	80		65	85		dB
				70°C	60	85		60	88		
				0°C	60	84		60	88		
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{DD} / \Delta V_{IO}$)		V_{DD} = 5 V to 10 V, V_O = 1.4 V	25°C	65	95		65	95		dB
				70°C	60	96		60	96		
				0°C	60	94		60	94		
$I_{I(SEL)}$	Input current to bias select pin		$V_{I(SEL)}$ = 0	25°C		−1.4			−1.9		μA
I_{DD}	Supply current		No load, $V_O = V_{DD}/2$, $V_{IC} = V_{DD}/2$	25°C		675	1600		950	2000	μA
				70°C		575	1300		750	1700	
				0°C		775	1800		1125	2200	

NOTES: 5. The typical values of input bias current and input offset current below 5 pA were determined mathematically.
6. This range also applies to each input individually.
7. At V_{DD} = 5 V, V_O = 0.25 V to 2 V; at V_{DD} = 10 V, V_O = 1 V to 6 V.

HIGH-BIAS MODE

electrical characteristics over recommended free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS		I-SUFFIX TYPES V_{DD} = 5 V MIN	TYP	MAX	I-SUFFIX TYPES V_{DD} = 10 V MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage	TLC271I	V_O = 1.4 V, V_{IC} = 0 V, R_S = 50 Ω, R_L = 10 kΩ	25°C		1.1	10		1.1	10	mV
				Full range			13			13	
		TLC271AI		25°C		0.9	5		0.9	5	
				Full range			7			7	
		TLC271BI		25°C		0.34	2		0.39	2	
				Full range			3.5			3.5	
α_{VIO}	Average temperature coefficient of input offset voltage			25°C to 85°C		1.8			2		μV/°C
I_{IO}	Input offset current (see Note 5)		V_O = V_{DD} / 2, V_{IC} = V_{DD} / 2	25°C		0.1			0.1		pA
				85°C		24	1000		26	1000	
I_{IB}	Input bias current (see Note 5)		V_O = V_{DD} / 2, V_{IC} = V_{DD} / 2	25°C		0.6			0.7		pA
				85°C		200	2000		220	2000	
V_{ICR}	Common-mode input voltage range (see Note 6)			25°C	−0.2 to 4	−0.3 to 4.2		−0.2 to 9	−0.3 to 9.2		V
				Full range	−0.2 to 3.5			−0.2 to 8.5			V
V_{OH}	High-level output voltage		V_{ID} = 100 mV, R_L = 10 kΩ	25°C	3.2	3.8		8	8.5		V
				85°C	3	3.8		7.8	8.5		
				−40°C	3	3.8		7.8	8.5		
V_{OL}	Low-level output voltage		V_{ID} = −100 mV, I_{OL} = 0	25°C		0	50		0	50	mV
				85°C		0	50		0	50	
				−40°C		0	50		0	50	
A_{VD}	Large-signal differential voltage amplification		R_L = 10 kΩ, See Note 7	25°C	5	23		10	36		V/mV
				85°C	3.5	19		7	31		
				−40°C	3.5	32		7	46		
CMRR	Common-mode rejection ratio		V_{IC} = V_{ICR}min	25°C	65	80		65	85		dB
				85°C	60	86		60	88		
				−40°C	60	81		60	87		
k_{SVR}	Supply-voltage rejection ratio (ΔV_{DD} / ΔV_{IO})		V_{DD} = 5 V to 10 V, V_O = 1.4 V	25°C	65	95		65	95		dB
				85°C	60	96		60	96		
				−40°C	60	92		60	92		
$I_{I(SEL)}$	Input current to bias select pin		$V_{I(SEL)}$ = 0	25°C		−1.4			−1.9		μA
I_{DD}	Supply current		No load, V_O = V_{DD} / 2, V_{IC} = V_{DD} / 2	25°C		675	1600		950	2000	μA
				85°C		525	1200		725	1600	
				−40°C		950	2200		1375	2500	

NOTES: 5. The typical values of input bias current and input offset current below 5 pA were determined mathematically.
6. This range also applies to each input individually.
7. At V_{DD} = 5 V, V_O = 0.25 V to 2 V; at V_{DD} = 10 V, V_O = 1 V to 6 V.

HIGH-BIAS MODE

electrical characteristics over recommended free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		M- SUFFIX TYPES						UNIT
				V_{DD} = 5 V			V_{DD} = 10 V			
				MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	V_O = 1.4 V, V_{IC} = 0 V, R_S = 50 Ω, R_L = 10 kΩ	25°C		1.1	10		1.1	10	mV
			Full range			12			12	
α_{VIO}	Average temperature coefficient of input offset voltage		25°C to 125°C		2.1			2.2		μV/°C
I_{IO}	Input offset current (see Note 5)	V_O = V_{DD} / 2, V_{IC} = V_{DD} / 2	25°C		0.1			0.1		pA
			125°C		1.4	15		1.8	15	nA
I_{IB}	Input bias current (see Note 5)	V_O = V_{DD} / 2, V_{IC} = V_{DD} / 2	25°C		0.6			0.7		pA
			125°C		9	35		10	35	nA
V_{ICR}	Common-mode input voltage range (see Note 6)		25°C	0 to 4	−0.3 to 4.2		0 to 9	−0.3 to 9.2		V
			Full range	0 to 3.5			0 to 8.5			V
V_{OH}	High-level output voltage	V_{ID} = 100 mV, R_L = 10 kΩ	25°C	3.2	3.8		8	8.5		V
			125°C	3	3.8		7.8	8.4		
			−55°C	3	3.8		7.8	8.5		
V_{OL}	Low-level output voltage	V_{ID} = −100 mV, I_{OL} = 0	25°C		0	50		0	50	mV
			125°C		0	50		0	50	
			−55°C		0	50		0	50	
A_{VD}	Large-signal differential voltage amplification	R_L = 10 kΩ, See Note 7	25°C	5	23		10	36		V/mV
			125°C	3.5	16		7	27		
			−55°C	3.5	35		7	50		
CMRR	Common-mode rejection ratio	V_{IC} = V_{ICR}min	25°C	65	80		65	85		dB
			125°C	60	84		60	86		
			−55°C	60	81		60	87		
k_{SVR}	Supply-voltage rejection ratio (ΔV_{DD} / ΔV_{IO})	V_{DD} = 5 V to 10 V, V_O = 1.4 V	25°C	65	95		65	95		dB
			125°C	60	97		60	97		
			−55°C	60	90		60	90		
$I_{I(SEL)}$	Input current to bias select pin	$V_{I(SEL)}$ = 0	25°C		−1.4			−1.9		μA
I_{DD}	Supply current	No load, V_O = V_{DD} / 2, V_{IC} = V_{DD} / 2	25°C		675	1600		950	2000	μA
			125°C		475	1100		625	1400	
			−55°C		1000	2500		1475	3000	

NOTES: 5. The typical values of input bias current and input offset current below 5 pA were determined mathematically.
6. This range also applies to each input individually.
7. At V_{DD} = 5 V, V_O = 0.25 V to 2 V; at V_{DD} = 10 V, V_O = 1 V to 6 V.

HIGH-BIAS MODE

operating characteristics, V_{DD} = 5 V

PARAMETER		TEST CONDITIONS			C- SUFFIX TYPES MIN	TYP	MAX	UNIT
SR	Slew rate at unity gain	R_L = 10 kΩ, C_L = 20 pF, See Figure 99	V_{IPP} = 1 V	25°C		3.6		V/μs
				70°C		3		
				0°C		3.9		
			V_{IPP} = 2.5 V	25°C		2.9		
				70°C		2.5		
				0°C		3.1		
V_n	Equivalent input noise voltage	f = 1 kHz, R_S = 100 Ω, See Figure 100		25°C		25		nV/√Hz
B_{OM}	Maximum output swing bandwidth	V_O = V_{OH}, C_L = 20 pF, R_L = 10 kΩ, See Figure 99		25°C		320		kHz
				70°C		260		
				0°C		340		
B_1	Unity-gain bandwidth	V_i = 10 mV, C_L = 20 pF, See Figure 101		25°C		1.7		MHz
				70°C		1.3		
				0°C		2		
ϕ_m	Phase margin	f = B_1, V_i = 10 mV, C_L = 20 pF, See Figure 101		25°C		46°		
				70°C		43°		
				0°C		47°		

operating characteristics, V_{DD} = 10 V

PARAMETER		TEST CONDITIONS			C- SUFFIX TYPES MIN	TYP	MAX	UNIT
SR	Slew rate at unity gain	R_L = 10 kΩ, C_L = 20 pF, See Figure 99	V_{IPP} = 1 V	25°C		5.3		V/μs
				70°C		4.3		
				0°C		5.9		
			V_{IPP} = 5.5 V	25°C		4.6		
				70°C		3.8		
				0°C		5.1		
V_n	Equivalent input noise voltage	f = 1 kHz, R_S = 100 Ω, See Figure 100		25°C		25		nV/√Hz
B_{OM}	Maximum output swing bandwidth	V_O = V_{OH}, C_L = 20 pF, R_L = 10 kΩ, See Figure 99		25°C		200		kHz
				70°C		140		
				0°C		220		
B_1	Unity-gain bandwidth	V_i = 10 mV, C_L = 20 pF, See Figure 101		25°C		2.2		MHz
				70°C		1.8		
				0°C		2.5		
ϕ_m	Phase margin	f = B_1, V_i = 10 mV, C_L = 20 pF, See Figure 101		25°C		49°		
				70°C		46°		
				0°C		50°		

HIGH-BIAS MODE

operating characteristics, V_{DD} = 5 V

PARAMETER		TEST CONDITIONS			I-SUFFIX TYPES MIN	TYP	MAX	UNIT
SR	Slew rate at unity gain	R_L = 10 kΩ, C_L = 20 pF, See Figure 99	V_{IPP} = 1 V	25°C		3.6		V/μs
				85°C		2.8		
				−40°C		4.5		
			V_{IPP} = 2.5 V	25°C		2.9		
				85°C		2.3		
				−40°C		3.5		
V_n	Equivalent input noise voltage	f = 1 kHz, R_S = 100 Ω, See Figure 100		25°C		25		nV/√Hz
B_{OM}	Maximum output swing bandwidth	$V_O = V_{OH}$, C_L = 20 pF, R_L = 10 kΩ, See Figure 99		25°C		320		kHz
				85°C		250		
				−40°C		380		
B_1	Unity-gain bandwidth	V_i = 10 mV, C_L = 20 pF, See Figure 101		25°C		1.7		MHz
				85°C		1.2		
				−40°C		2.6		
ϕ_m	Phase margin	f = B_1, V_i = 10 mV, C_L = 20 pF, See Figure 101		25°C		46°		
				85°C		43°		
				−40°C		49°		

operating characteristics, V_{DD} = 10 V

PARAMETER		TEST CONDITIONS			I-SUFFIX TYPES MIN	TYP	MAX	UNIT
SR	Slew rate at unity gain	R_L = 10 kΩ, C_L = 20 pF, See Figure 99	V_{IPP} = 1 V	25°C		5.3		V/μs
				85°C		4		
				−40°C		6.7		
			V_{IPP} = 5.5 V	25°C		4.6		
				85°C		3.5		
				−40°C		5.8		
V_n	Equivalent input noise voltage	f = 1 kHz, R_S = 100 Ω, See Figure 100		25°C		25		nV/√Hz
B_{OM}	Maximum output swing bandwidth	$V_O = V_{OH}$, C_L = 20 pF, R_L = 10 kΩ, See Figure 99		25°C		200		kHz
				85°C		130		
				−40°C		260		
B_1	Unity-gain bandwidth	V_i = 10 mV, C_L = 20 pF, See Figure 101		25°C		2.2		MHz
				85°C		1.7		
				−40°C		3.1		
ϕ_m	Phase margin	f = B_1, V_i = 10 mV, C_L = 20 pF, See Figure 101		25°C		49°		
				85°C		46°		
				−40°C		52°		

HIGH-BIAS MODE

operating characteristics, V_{DD} = 5 V

PARAMETER		TEST CONDITIONS			M- SUFFIX TYPES MIN	TYP	MAX	UNIT
SR	Slew rate at unity gain	R_L = 10 kΩ, C_L = 20 pF, See Figure 99	V_{IPP} = 1 V	25°C		3.6		V/μs
				125°C		2.3		
				– 55°C		4.7		
			V_{IPP} = 2.5 V	25°C		2.9		
				125°C		2		
				– 55°C		3.7		
V_n	Equivalent input noise voltage	f = 1 kHz, R_S = 100 Ω, See Figure 100		25°C		25		nV/√Hz
B_{OM}	Maximum output swing bandwidth	$V_O = V_{OH}$, C_L = 20 pF, R_L = 10 kΩ, See Figure 99		25°C		320		kHz
				125°C		230		
				– 55°C		400		
B_1	Unity-gain bandwidth	V_i = 10 mV, C_L = 20 pF, See Figure 101		25°C		1.7		MHz
				125°C		1.1		
				– 55°C		2.9		
ϕ_m	Phase margin	f = B_1, V_i = 10 mV, C_L = 20 pF, See Figure 101		25°C		46°		
				125°C		41°		
				– 55°C		49°		

operating characteristics, V_{DD} = 10 V

PARAMETER		TEST CONDITIONS			M- SUFFIX TYPES MIN	TYP	MAX	UNIT
SR	Slew rate at unity gain	R_L = 10 kΩ, C_L = 20 pF, See Figure 99	V_{IPP} = 1 V	25°C		5.3		V/μs
				125°C		3.1		
				– 55°C		7.1		
			V_{IPP} = 5.5 V	25°C		4.6		
				125°C		2.7		
				– 55°C		6.1		
V_n	Equivalent input noise voltage	f = 1 kHz, R_S = 100 Ω, See Figure 100		25°C		25		nV/√Hz
B_{OM}	Maximum output swing bandwidth	$V_O = V_{OH}$, C_L = 20 pF, R_L = 10 kΩ, See Figure 99		25°C		200		kHz
				125°C		110		
				– 55°C		280		
B_1	Unity-gain bandwidth	V_i = 10 mV, C_L = 20 pF, See Figure 101		25°C		2.2		MHz
				125°C		1.6		
				– 55°C		3.4		
ϕ_m	Phase margin	f = B_1, V_i = 10 mV, C_L = 20 pF, See Figure 101		25°C		49°		
				125°C		44°		
				– 55°C		52°		

TYPICAL CHARACTERISTICS (HIGH-BIAS MODE)

DISTRIBUTION OF TLC271
INPUT OFFSET VOLTAGE

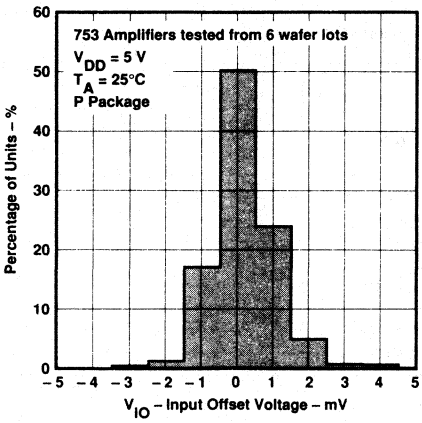


FIGURE 3

DISTRIBUTION OF TLC271
INPUT OFFSET VOLTAGE

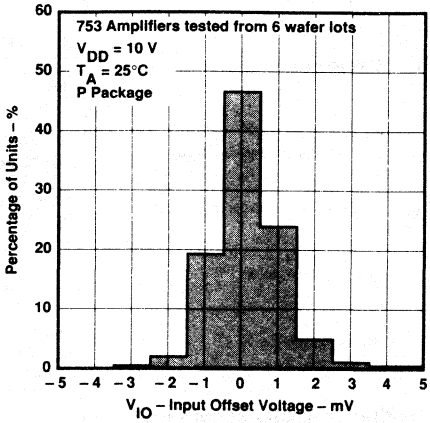


FIGURE 4

DISTRIBUTION OF TLC271
INPUT OFFSET VOLTAGE
TEMPERATURE COEFFICIENT

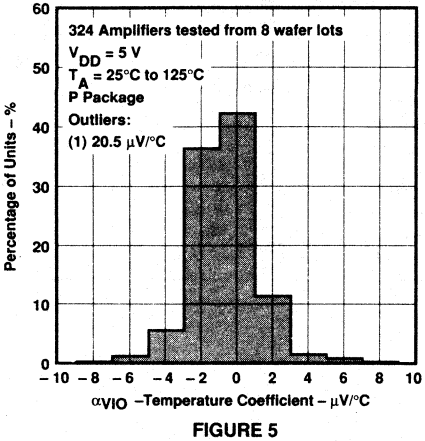


FIGURE 5

DISTRIBUTION OF TLC271
INPUT OFFSET VOLTAGE
TEMPERATURE COEFFICIENT

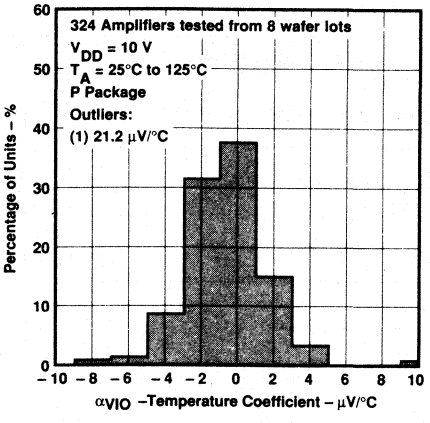


FIGURE 6

TYPICAL CHARACTERISTICS (HIGH-BIAS MODE)

HIGH-LEVEL OUTPUT VOLTAGE
vs
HIGH-LEVEL OUTPUT CURRENT

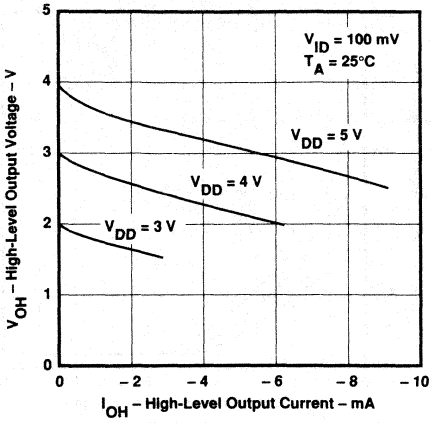


FIGURE 7

HIGH-LEVEL OUTPUT VOLTAGE
vs
HIGH-LEVEL OUTPUT CURRENT

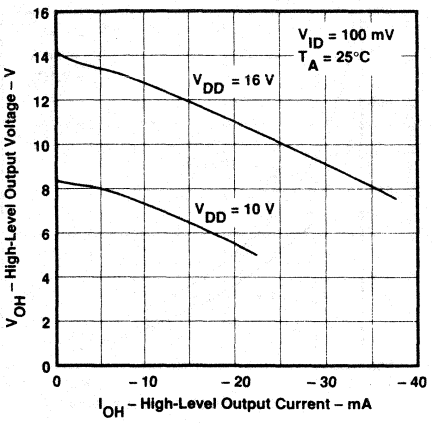


FIGURE 8

HIGH-LEVEL OUTPUT VOLTAGE
vs
SUPPLY VOLTAGE

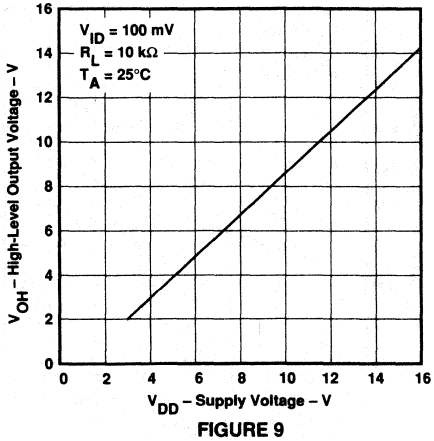


FIGURE 9

HIGH-LEVEL OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE

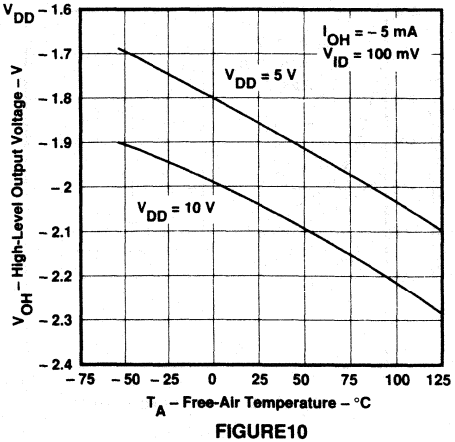


FIGURE10

TYPICAL CHARACTERISTICS (HIGH-BIAS MODE)

LOW-LEVEL OUTPUT VOLTAGE
vs
COMMON-MODE INPUT VOLTAGE

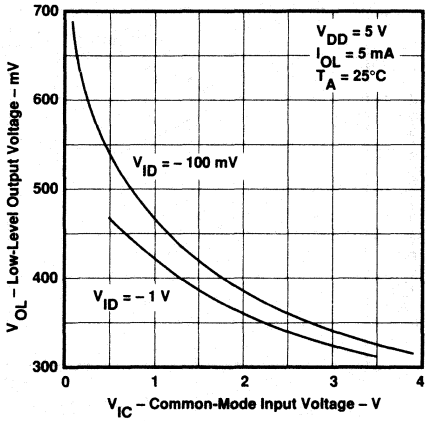


FIGURE 11

LOW-LEVEL OUTPUT VOLTAGE
vs
COMMON-MODE INPUT VOLTAGE

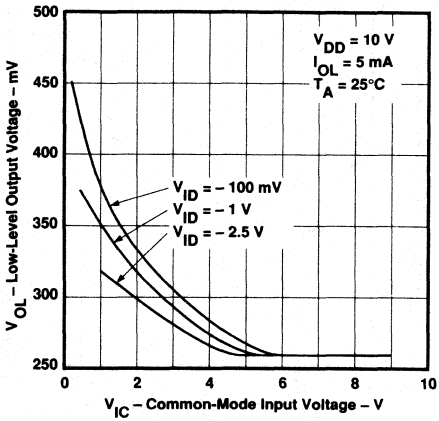


FIGURE 12

LOW-LEVEL OUTPUT VOLTAGE
vs
DIFFERENTIAL INPUT VOLTAGE

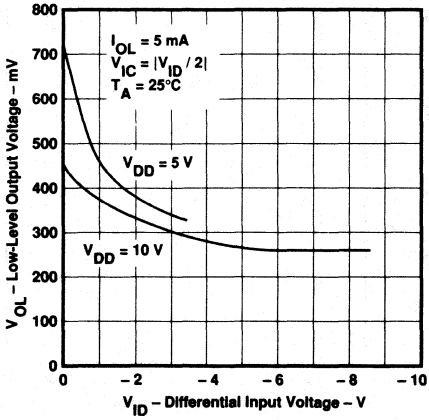


FIGURE 13

LOW-LEVEL OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE

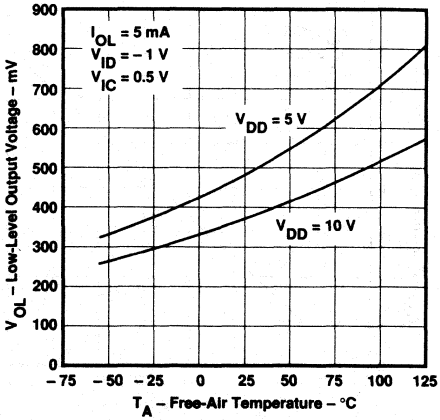


FIGURE 14

TYPICAL CHARACTERISTICS (HIGH-BIAS MODE)

LOW-LEVEL OUTPUT VOLTAGE
vs
LOW-LEVEL OUTPUT CURRENT

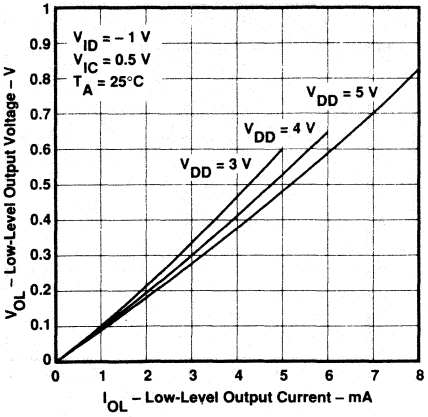


FIGURE 15

LOW-LEVEL OUTPUT VOLTAGE
vs
LOW-LEVEL OUTPUT CURRENT

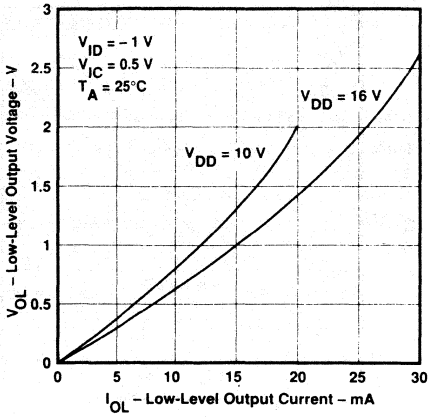


FIGURE 16

LARGE-SIGNAL
DIFFERENTIAL VOLTAGE AMPLIFICATION
vs
SUPPLY VOLTAGE

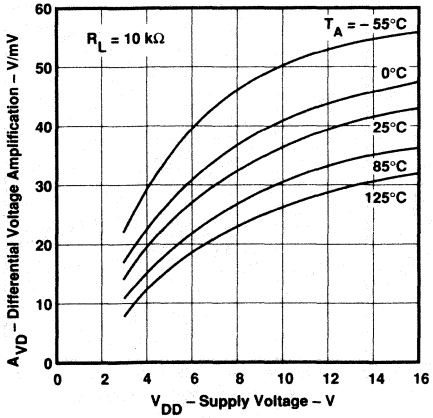


FIGURE 17

LARGE-SIGNAL
DIFFERENTIAL VOLTAGE AMPLIFICATION
vs
FREE-AIR TEMPERATURE

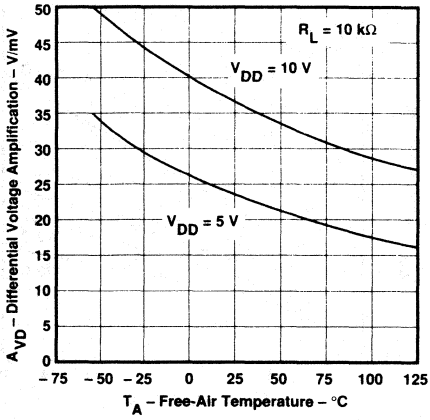


FIGURE 18

TYPICAL CHARACTERISTICS (HIGH-BIAS MODE)

INPUT BIAS CURRENT AND INPUT OFFSET CURRENT
vs
FREE-AIR TEMPERATURE

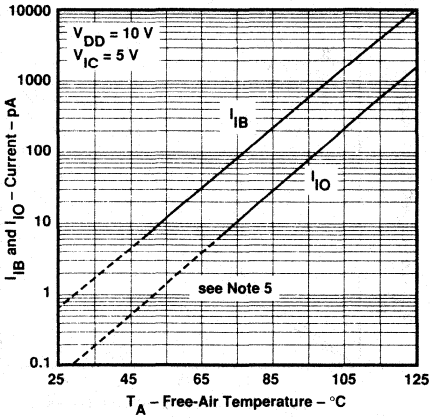


FIGURE 19

MAXIMUM INPUT VOLTAGE
vs
SUPPLY VOLTAGE

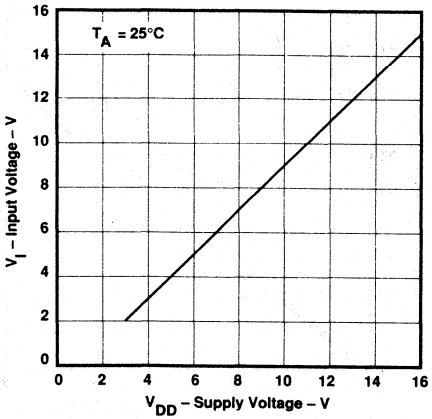


FIGURE 20

SUPPLY CURRENT
vs
SUPPLY VOLTAGE

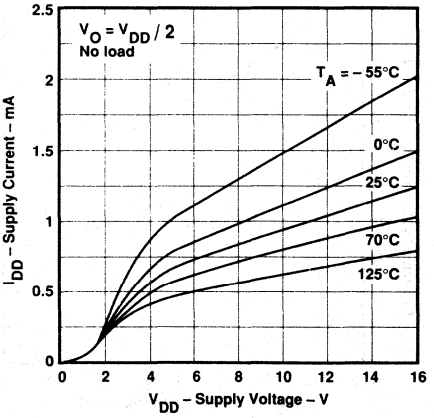


FIGURE 21

SUPPLY CURRENT
vs
FREE-AIR TEMPERATURE

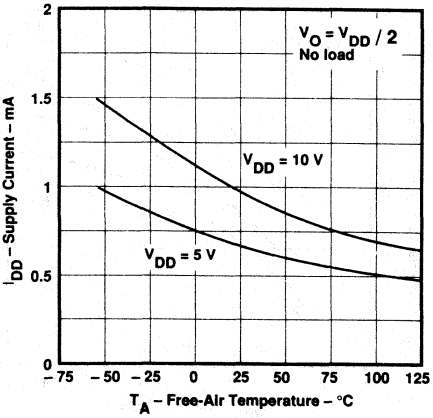


FIGURE 22

NOTE 5: The typical values of input bias current and input offset current below 5 pA were determined mathematically.

TYPICAL CHARACTERISTICS (HIGH-BIAS MODE)

SLEW RATE
vs
SUPPLY VOLTAGE

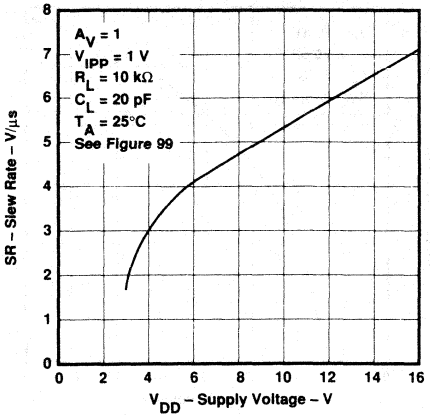


FIGURE 23

SLEW RATE
vs
FREE-AIR TEMPERATURE

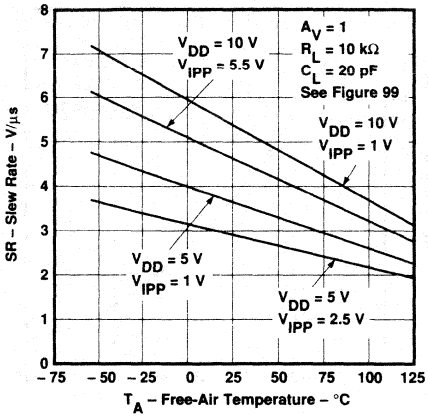


FIGURE 24

BIAS SELECT CURRENT
vs
SUPPLY VOLTAGE

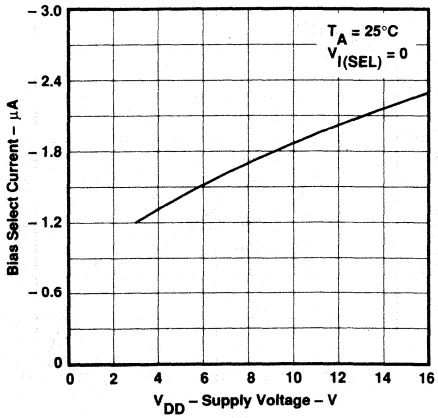


FIGURE 25

MAXIMUM PEAK-TO-PEAK OUTPUT VOLTAGE
vs
FREQUENCY

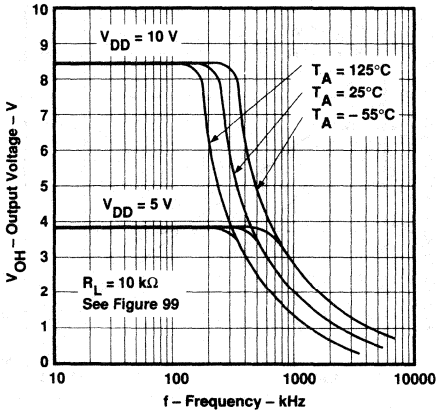


FIGURE 26

TYPICAL CHARACTERISTICS (HIGH-BIAS MODE)

UNITY-GAIN BANDWIDTH
vs
FREE-AIR TEMPERATURE

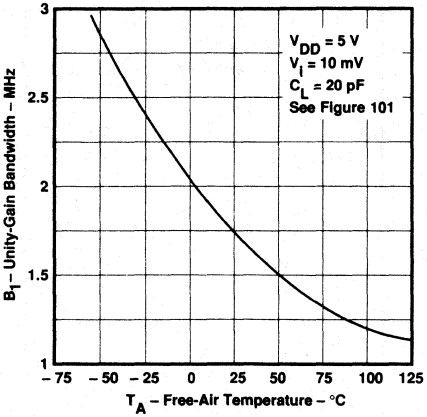


FIGURE 27

UNITY-GAIN BANDWIDTH
vs
SUPPLY VOLTAGE

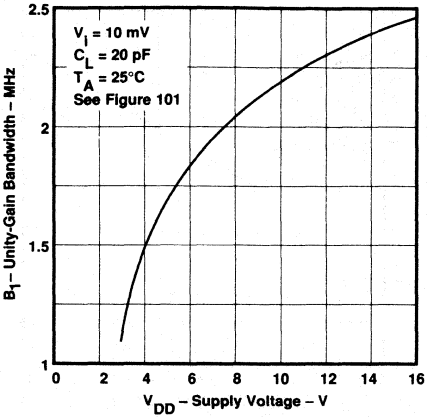


FIGURE 28

LARGE-SIGNAL DIFFERENTIAL VOLTAGE
AMPLIFICATION AND PHASE SHIFT
vs
FREQUENCY

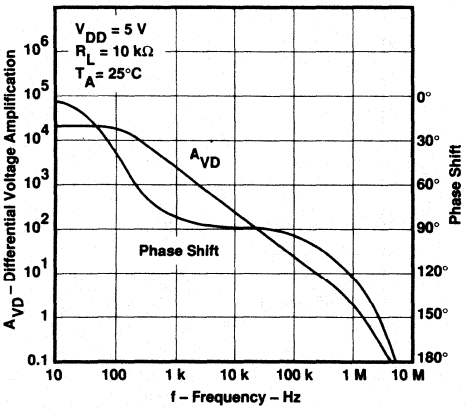


FIGURE 29

LARGE-SIGNAL DIFFERENTIAL VOLTAGE
AMPLIFICATION AND PHASE SHIFT
vs
FREQUENCY

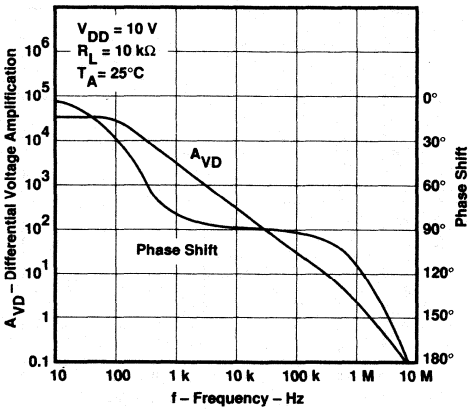


FIGURE 30

TYPICAL CHARACTERISTICS (HIGH-BIAS MODE)

PHASE MARGIN
vs
SUPPLY VOLTAGE

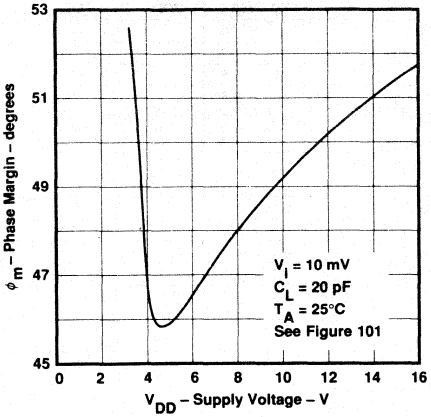


FIGURE 31

PHASE MARGIN
vs
FREE-AIR TEMPERATURE

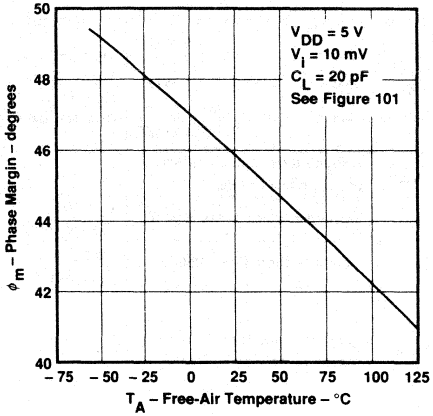


FIGURE 32

PHASE MARGIN
vs
CAPACITIVE LOAD

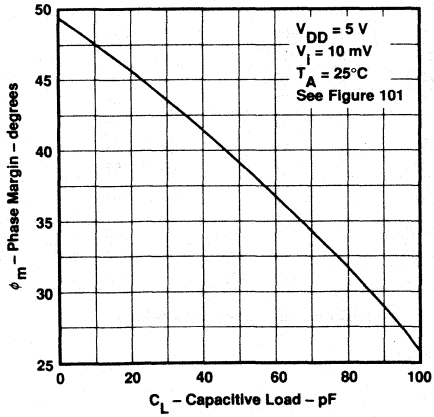


FIGURE 33

EQUIVALENT INPUT NOISE VOLTAGE
vs
FREQUENCY

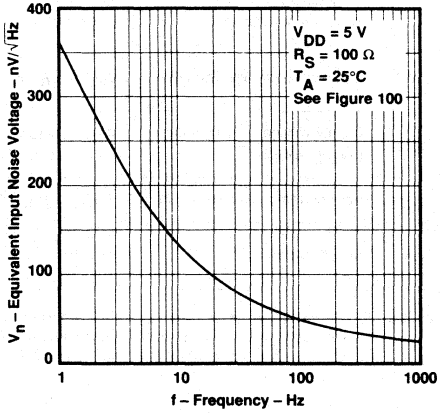


FIGURE 34

MEDIUM-BIAS MODE

electrical characteristics over recommended free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS		C- SUFFIX TYPES V_{DD} = 5 V MIN	TYP	MAX	C- SUFFIX TYPES V_{DD} = 10 V MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage	TLC271C	V_O = 1.4 V, V_{IC} = 0 V, R_S = 50 Ω, R_L = 100 kΩ	25°C		1.1	10		1.1	10	mV
				Full range			12			12	
		TLC271AC		25°C		0.9	5		0.9	5	
				Full range			6.5			6.5	
		TLC271BC		25°C		0.25	2		0.26	2	
				Full range			3			3	
α_{VIO}	Average temperature coefficient of input offset voltage			25°C to 70°C		1.7			2.1		µV/°C
I_{IO}	Input offset current (see Note 5)		V_O = V_{DD} / 2, V_{IC} = V_{DD} / 2	25°C		0.1			0.1		pA
				70°C		7	300		8	300	
I_{IB}	Input bias current (see Note 5)		V_O = V_{DD} / 2, V_{IC} = V_{DD} / 2	25°C		0.6			0.7		pA
				70°C		40	600		50	600	
V_{ICR}	Common-mode input voltage range (see Note 6)			25°C	−0.2 to 4	−0.3 to 4.2		−0.2 to 9	−0.3 to 9.2		V
				Full range	−0.2 to 3.5			−0.2 to 8.5			V
V_{OH}	High-level output voltage		V_{ID} = 100 mV, R_L = 100 kΩ	25°C	3.2	3.9		8	8.7		V
				70°C	3	4		7.8	8.7		
				0°C	3	3.9		7.8	8.7		
V_{OL}	Low-level output voltage		V_{ID} = −100 mV, I_{OL} = 0	25°C		0	50		0	50	mV
				70°C		0	50		0	50	
				0°C		0	50		0	50	
A_{VD}	Large-signal differential voltage amplification		R_L = 100 kΩ, See Note 7	25°C	25	170		25	275		V/mV
				70°C	15	140		15	230		
				0°C	15	200		15	320		
CMRR	Common-mode rejection ratio		V_{IC} = V_{ICR}min	25°C	65	91		65	94		dB
				70°C	60	92		60	94		
				0°C	60	91		60	94		
k_{SVR}	Supply-voltage rejection ratio (ΔV_{DD} / ΔV_{IO})		V_{DD} = 5 V to 10 V, V_O = 1.4 V	25°C	70	93		70	93		dB
				70°C	60	94		60	94		
				0°C	60	92		60	92		
$I_{I(SEL)}$	Input current to bias select pin		$V_{I(SEL)}$ = V_{DD} / 2	25°C		−130			−160		nA
I_{DD}	Supply current		No load, V_O = V_{DD} / 2, V_{IC} = V_{DD} / 2	25°C		105	280		143	300	µA
				70°C		85	220		110	280	
				0°C		125	320		173	400	

NOTES: 5. The typical values of input bias current and input offset current below 5 pA were determined mathematically.
6. This range also applies to each input individually.
7. At V_{DD} = 5 V, V_O = 0.25 V to 2 V; at V_{DD} = 10 V, V_O = 1 V to 6 V.

MEDIUM-BIAS MODE

electrical characteristics over recommended free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS		I-SUFFIX TYPES V_{DD} = 5 V MIN	TYP	MAX	I-SUFFIX TYPES V_{DD} = 10 V MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage	TLC271I	V_O = 1.4 V, V_{IC} = 0 V, R_S = 50 Ω, R_L = 100 kΩ	25°C		1.1	10		1.1	10	mV
				Full range			13			13	
		TLC271AI		25°C		0.9	5		0.9	5	
				Full range			7			7	
		TLC271BI		25°C		0.25	2		0.26	2	
				Full range			3.5			3.5	
α_{VIO}	Average temperature coefficient of input offset voltage			25°C to 85°C		1.7			2.1		μV/°C
I_{IO}	Input offset current (see Note 5)		$V_O = V_{DD}/2$, $V_{IC} = V_{DD}/2$	25°C		0.1			0.1		pA
				85°C		24	1000		26	1000	
I_{IB}	Input bias current (see Note 5)		$V_O = V_{DD}/2$, $V_{IC} = V_{DD}/2$	25°C		0.6			0.7		pA
				85°C		200	2000		220	2000	
V_{ICR}	Common-mode input voltage range (see Note 6)			25°C	−0.2 to 4	−0.3 to 4.2		−0.2 to 9	−0.3 to 9.2		V
				Full range	−0.2 to 3.5			−0.2 to 8.5			V
V_{OH}	High-level output voltage		V_{ID} = 100 mV, R_L = 100 kΩ	25°C	3.2	3.9		8	8.7		V
				85°C	3	4		7.8	8.7		
				−40°C	3	3.9		7.8	8.7		
V_{OL}	Low-level output voltage		V_{ID} = −100 mV, I_{OL} = 0	25°C		0	50		0	50	mV
				85°C		0	50		0	50	
				−40°C		0	50		0	50	
A_{VD}	Large-signal differential voltage amplification		R_L = 100 kΩ, See Note 7	25°C	25	170		25	275		V/mV
				85°C	15	130		15	220		
				−40°C	15	270		15	390		
CMRR	Common-mode rejection ratio		$V_{IC} = V_{ICR}$min	25°C	65	91		65	94		dB
				85°C	60	90		60	94		
				−40°C	60	90		60	93		
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{DD}/\Delta V_{IO}$)		V_{DD} = 5 V to 10 V, V_O = 1.4 V	25°C	70	93		70	93		dB
				85°C	60	94		60	94		
				−40°C	60	91		60	91		
$I_{I(SEL)}$	Input current to bias select pin		$V_{I(SEL)} = V_{DD}/2$	25°C		−130			−160		nA
I_{DD}	Supply current		No load, $V_O = V_{DD}/2$, $V_{IC} = V_{DD}/2$	25°C		105	280		143	300	μA
				85°C		80	200		103	260	
				−40°C		158	400		225	450	

NOTES: 5. The typical values of input bias current and input offset current below 5 pA were determined mathematically.
6. This range also applies to each input individually.
7. At V_{DD} = 5 V, V_O = 0.25 V to 2 V; at V_{DD} = 10 V, V_O = 1 V to 6 V.

MEDIUM-BIAS MODE

electrical characteristics over recommended free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		M- SUFFIX TYPES V_{DD} = 5 V MIN	TYP	MAX	V_{DD} = 10 V MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage	V_O = 1.4 V, V_{IC} = 0 V, R_S = 50 Ω, R_L = 100 kΩ	25°C		1.1	10		1.1	10	mV
			Full range			12			12	
α_{VIO}	Average temperature coefficient of input offset voltage		25°C to 125°C		1.7			2.1		µV/°C
I_{IO}	Input offset current (see Note 5)	V_O = V_{DD} / 2, V_{IC} = V_{DD} / 2	25°C		0.1			0.1		pA
			125°C		1.4	15		1.8	15	nA
I_{IB}	Input bias current (see Note 5)	V_O = V_{DD} / 2, V_{IC} = V_{DD} / 2	25°C		0.6			0.7		pA
			125°C		9	35		10	35	nA
V_{ICR}	Common-mode input voltage range (see Note 6)		25°C	0 to 4	−0.3 to 4.2		0 to 9	−0.3 to 9.2		V
			Full range	0 to 3.5			0 to 8.5			V
V_{OH}	High-level output voltage	V_{ID} = 100 mV, R_L = 100 kΩ	25°C	3.2	3.9		8	8.7		V
			125°C	3	4		7.8	3.8		
			−55°C	3	3.9		7.8	8.6		
V_{OL}	Low-level output voltage	V_{ID} = −100 mV, I_{OL} = 0	25°C		0	50		0	50	mV
			125°C		0	50		0	50	
			−55°C		0	50		0	50	
A_{VD}	Large-signal differential voltage amplification	R_L = 100 kΩ, See Note 7	25°C	25	170		25	275		V/mV
			125°C	15	120		15	190		
			−55°C	15	290		15	420		
CMRR	Common-mode rejection ratio	V_{IC} = V_{ICR}min	25°C	65	91		65	94		dB
			125°C	60	91		60	93		
			−55°C	60	89		60	93		
k_{SVR}	Supply-voltage rejection ratio (ΔV_{DD} / ΔV_{IO})	V_{DD} = 5 V to 10 V, V_O = 1.4 V	25°C	70	93		70	93		dB
			125°C	60	94		60	94		
			−55°C	60	91		60	91		
$I_{I(SEL)}$	Input current to bias select pin	$V_{I(SEL)}$ = V_{DD} / 2	25°C		−130			−160		nA
I_{DD}	Supply current	No load, V_O = V_{DD} / 2, V_{IC} = V_{DD} / 2	25°C		105	280		143	300	µA
			125°C		70	180		90	240	
			−55°C		170	440		245	500	

NOTES: 5. The typical values of input bias current and input offset current below 5 pA were determined mathematically.
6. This range also applies to each input individually.
7. At V_{DD} = 5 V, V_O = 0.25 V to 2 V; at V_{DD} = 10 V, V_O = 1 V to 6 V.

MEDIUM-BIAS MODE

operating characteristics, V_{DD} = 5 V

PARAMETER		TEST CONDITIONS			C- SUFFIX TYPES MIN	TYP	MAX	UNIT
SR	Slew rate at unity gain	R_L = 100 kΩ, C_L = 20 pF, See Figure 99	V_{IPP} = 1 V	25°C		0.43		V/μs
				70°C		0.36		
				0°C		0.46		
			V_{IPP} = 2.5 V	25°C		0.40		
				70°C		0.34		
				0°C		0.43		
V_n	Equivalent input noise voltage	f = 1 kHz, R_S = 100 Ω, See Figure 100		25°C		32		nV/√Hz
B_{OM}	Maximum output swing bandwidth	V_O = V_{OH}, C_L = 20 pF, R_L = 100 kΩ, See Figure 99		25°C		55		kHz
				70°C		50		
				0°C		60		
B_1	Unity-gain bandwidth	V_i = 10 mV, C_L = 20 pF, See Figure 101		25°C		525		kHz
				70°C		400		
				0°C		600		
ϕ_m	Phase margin	f = B_1, V_i = 10 mV, C_L = 20 pF, See Figure 101		25°C		40°		
				70°C		39°		
				0°C		41°		

operating characteristics, V_{DD} = 10 V

PARAMETER		TEST CONDITIONS			C- SUFFIX TYPES MIN	TYP	MAX	UNIT
SR	Slew rate at unity gain	R_L = 100 kΩ, C_L = 20 pF, See Figure 99	V_{IPP} = 1 V	25°C		0.62		V/μs
				70°C		0.51		
				0°C		0.67		
			V_{IPP} = 5.5 V	25°C		0.56		
				70°C		0.46		
				0°C		0.61		
V_n	Equivalent input noise voltage	f = 1 kHz, R_S = 100 Ω, See Figure 100		25°C		32		nV/√Hz
B_{OM}	Maximum output swing bandwidth	V_O = V_{OH}, C_L = 20 pF, R_L = 100 kΩ, See Figure 99		25°C		35		kHz
				70°C		30		
				0°C		40		
B_1	Unity-gain bandwidth	V_i = 10 mV, C_L = 20 pF, See Figure 101		25°C		635		kHz
				70°C		510		
				0°C		710		
ϕ_m	Phase margin	f = B_1, V_i = 10 mV, C_L = 20 pF, See Figure 101		25°C		43°		
				70°C		42°		
				0°C		44°		

MEDIUM-BIAS MODE

operating characteristics, V_{DD} = 5 V

PARAMETER		TEST CONDITIONS			I-SUFFIX TYPES MIN	TYP	MAX	UNIT
SR	Slew rate at unity gain	R_L = 100 kΩ, C_L = 20 pF, See Figure 99	V_{IPP} = 1 V	25°C		0.43		V/μs
				85°C		0.35		
				−40°C		0.51		
			V_{IPP} = 2.5 V	25°C		0.40		
				85°C		0.32		
				−40°C		0.48		
V_n	Equivalent input noise voltage	f = 1 kHz, R_S = 100 Ω, See Figure 100		25°C		32		nV/√Hz
B_{OM}	Maximum output swing bandwidth	$V_O = V_{OH}$, C_L = 20 pF, R_L = 100 kΩ, See Figure 99		25°C		55		kHz
				85°C		45		
				−40°C		75		
B_1	Unity-gain bandwidth	V_i = 10 mV, C_L = 20 pF, See Figure 101		25°C		525		kHz
				85°C		370		
				−40°C		770		
ϕ_m	Phase margin	f = B_1, V_i = 10 mV, C_L = 20 pF, See Figure 101		25°C		40°		
				85°C		38°		
				−40°C		43°		

operating characteristics, V_{DD} = 10 V

PARAMETER		TEST CONDITIONS			I-SUFFIX TYPES MIN	TYP	MAX	UNIT
SR	Slew rate at unity gain	R_L = 100 kΩ, C_L = 20 pF, See Figure 99	V_{IPP} = 1 V	25°C		0.62		V/μs
				85°C		0.47		
				−40°C		0.77		
			V_{IPP} = 5.5 V	25°C		0.56		
				85°C		0.44		
				−40°C		0.70		
V_n	Equivalent input noise voltage	f = 1 kHz, R_S = 100 Ω, See Figure 100		25°C		32		nV/√Hz
B_{OM}	Maximum output swing bandwidth	$V_O = V_{OH}$, C_L = 20 pF, R_L = 100 kΩ, See Figure 99		25°C		35		kHz
				85°C		25		
				−40°C		45		
B_1	Unity-gain bandwidth	V_i = 10 mV, C_L = 20 pF, See Figure 101		25°C		635		kHz
				85°C		480		
				−40°C		880		
ϕ_m	Phase margin	f = B_1, V_i = 10 mV, C_L = 20 pF, See Figure 101		25°C		43°		
				85°C		41°		
				−40°C		46°		

MEDIUM-BIAS MODE

operating characteristics, V_{DD} = 5 V

PARAMETER		TEST CONDITIONS			M- SUFFIX TYPES MIN	TYP	MAX	UNIT
SR	Slew rate at unity gain	R_L = 100 kΩ, C_L = 20 pF, See Figure 99	V_{IPP} = 1 V	25°C		0.43		V/μs
				125°C		0.29		
				−55°C		0.54		
			V_{IPP} = 2.5 V	25°C		0.40		
				125°C		0.28		
				−55°C		0.50		
V_n	Equivalent input noise voltage	f = 1 kHz, R_S = 100 Ω, See Figure 100		25°C		32		nV/√Hz
B_{OM}	Maximum output swing bandwidth	$V_O = V_{OH}$, C_L = 20 pF, R_L = 100 kΩ, See Figure 99		25°C		55		kHz
				125°C		40		
				−55°C		80		
B_1	Unity-gain bandwidth	V_i = 10 mV, C_L = 20 pF, See Figure 101		25°C		525		kHz
				125°C		330		
				−55°C		850		
ϕ_m	Phase margin	f = B_1, V_i = 10 mV, C_L = 20 pF, See Figure 101		25°C		40°		
				125°C		36°		
				−55°C		44°		

operating characteristics, V_{DD} = 10 V

PARAMETER		TEST CONDITIONS			M- SUFFIX TYPES MIN	TYP	MAX	UNIT
SR	Slew rate at unity gain	R_L = 100 kΩ, C_L = 20 pF, See Figure 99	V_{IPP} = 1 V	25°C		0.62		V/μs
				125°C		0.38		
				−55°C		0.81		
			V_{IPP} = 5.5 V	25°C		0.56		
				125°C		0.35		
				−55°C		0.73		
V_n	Equivalent input noise voltage	f = 1 kHz, R_S = 100 Ω, See Figure 100		25°C		32		nV/√Hz
B_{OM}	Maximum output swing bandwidth	$V_O = V_{OH}$, C_L = 20 pF, R_L = 100 kΩ, See Figure 99		25°C		35		kHz
				125°C		20		
				−55°C		50		
B_1	Unity-gain bandwidth	V_i = 10 mV, C_L = 20 pF, See Figure 101		25°C		635		kHz
				125°C		440		
				−55°C		960		
ϕ_m	Phase margin	f = B_1, V_i = 10 mV, C_L = 20 pF, See Figure 101		25°C		43°		
				125°C		39°		
				−55°C		47°		

TYPICAL CHARACTERISTICS (MEDIUM-BIAS MODE)

DISTRIBUTION OF TLC271
INPUT OFFSET VOLTAGE

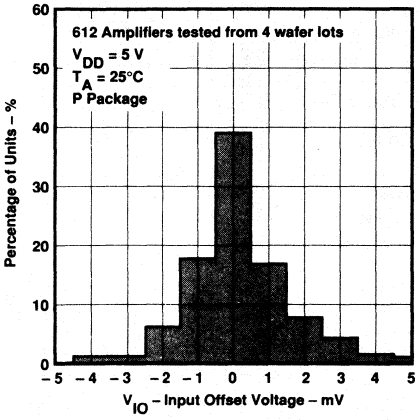


FIGURE 35

DISTRIBUTION OF TLC271
INPUT OFFSET VOLTAGE

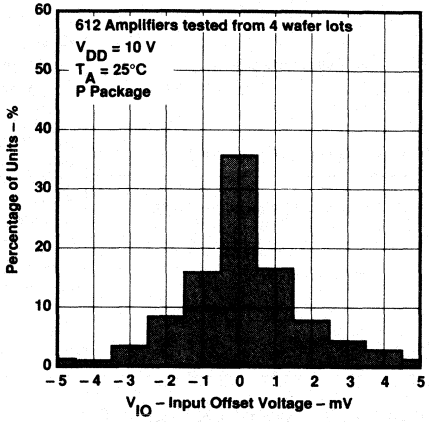


FIGURE 36

DISTRIBUTION OF TLC271
INPUT OFFSET VOLTAGE
TEMPERATURE COEFFICIENT

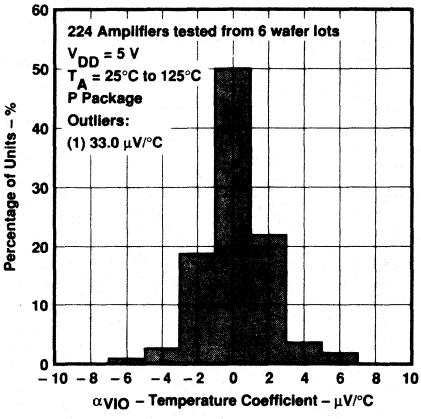


FIGURE37

DISTRIBUTION OF TLC271
INPUT OFFSET VOLTAGE
TEMPERATURE COEFFICIENT

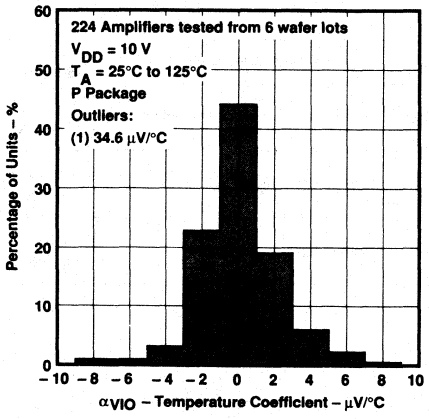


FIGURE 38

TYPICAL CHARACTERISTICS (MEDIUM-BIAS MODE)

HIGH-LEVEL OUTPUT VOLTAGE
vs
HIGH-LEVEL OUTPUT CURRENT

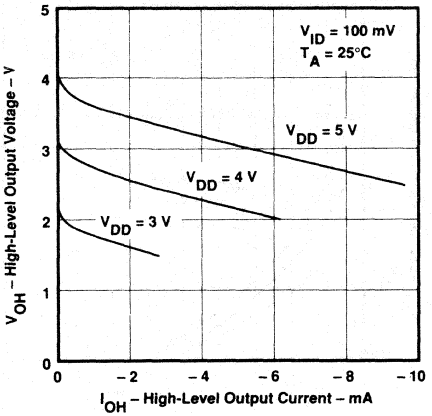


FIGURE 39

HIGH-LEVEL OUTPUT VOLTAGE
vs
HIGH-LEVEL OUTPUT CURRENT

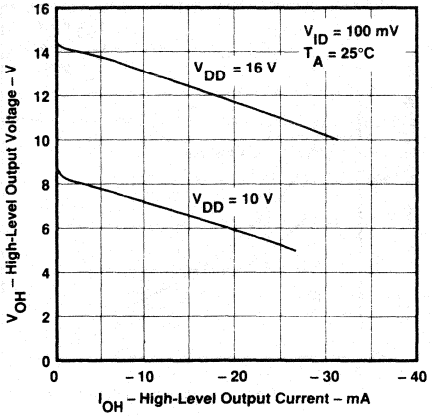


FIGURE 40

HIGH-LEVEL OUTPUT VOLTAGE
vs
SUPPLY VOLTAGE

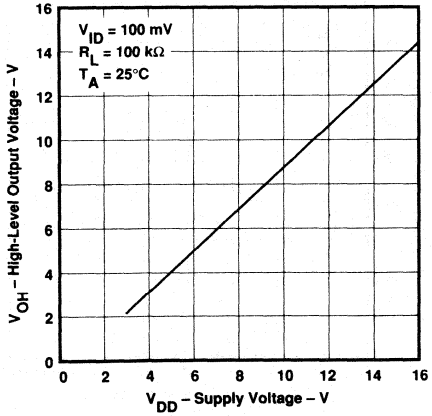


FIGURE 41

HIGH-LEVEL OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE

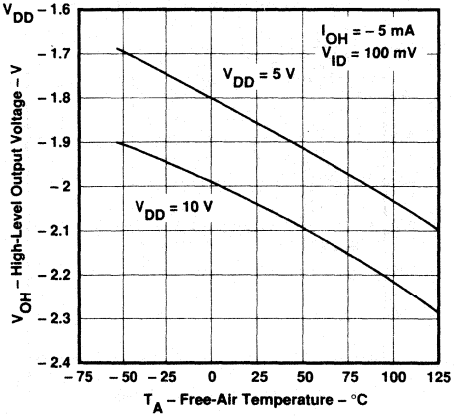


FIGURE 42

TYPICAL CHARACTERISTICS (MEDIUM-BIAS MODE)

LOW-LEVEL OUTPUT VOLTAGE
vs
COMMON-MODE INPUT VOLTAGE

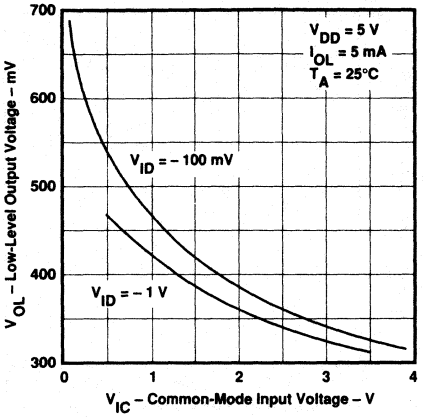


FIGURE 43

LOW-LEVEL OUTPUT VOLTAGE
vs
COMMON-MODE INPUT VOLTAGE

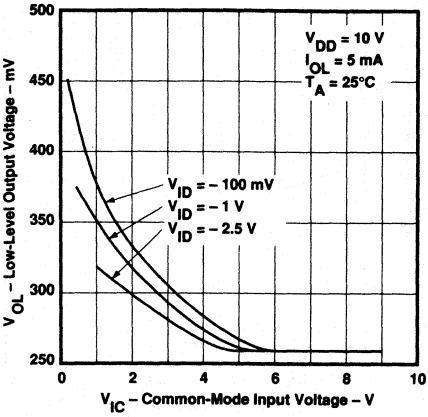


FIGURE 44

LOW-LEVEL OUTPUT VOLTAGE
vs
DIFFERENTIAL INPUT VOLTAGE

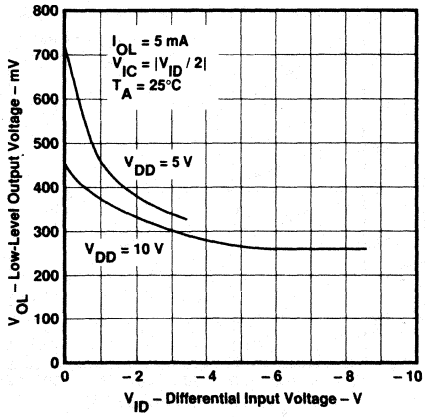


FIGURE 45

LOW-LEVEL OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE

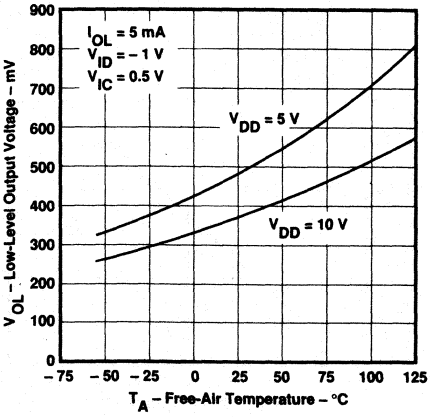


FIGURE 46

TYPICAL CHARACTERISTICS (MEDIUM-BIAS MODE)

LOW-LEVEL OUTPUT VOLTAGE
vs
LOW-LEVEL OUTPUT CURRENT

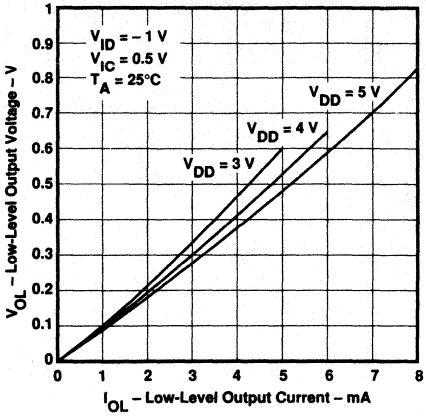


FIGURE 47

LOW-LEVEL OUTPUT VOLTAGE
vs
LOW-LEVEL OUTPUT CURRENT

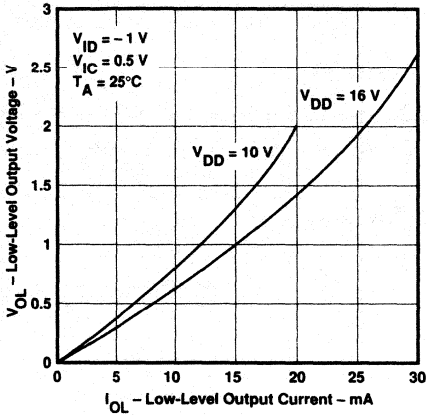


FIGURE 48

LARGE-SIGNAL
DIFFERENTIAL VOLTAGE AMPLIFICATION
vs
SUPPLY VOLTAGE

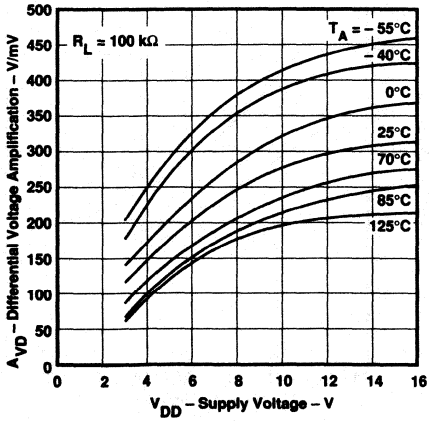


FIGURE 49

LARGE-SIGNAL
DIFFERENTIAL VOLTAGE AMPLIFICATION
vs
FREE-AIR TEMPERATURE

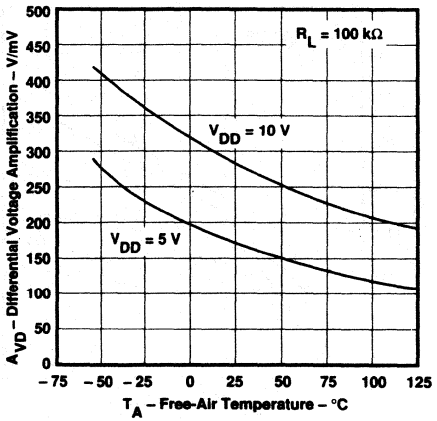


FIGURE 50

TYPICAL CHARACTERISTICS (MEDIUM-BIAS MODE)

INPUT BIAS CURRENT AND INPUT OFFSET CURRENT
vs
FREE-AIR TEMPERATURE

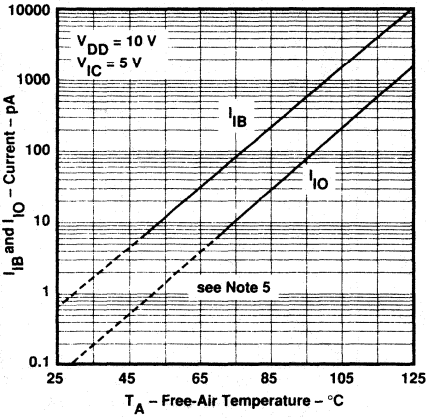


FIGURE 51

MAXIMUM INPUT VOLTAGE
vs
SUPPLY VOLTAGE

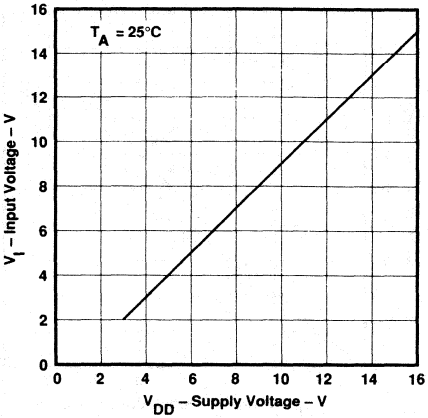


FIGURE 52

SUPPLY CURRENT
vs
SUPPLY VOLTAGE

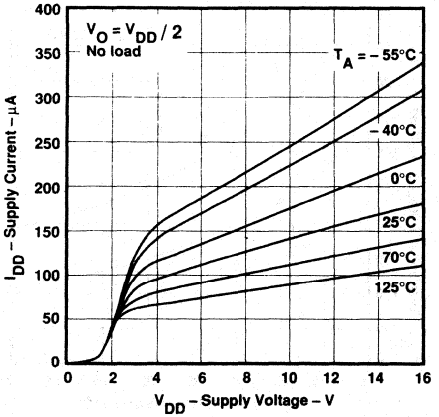


FIGURE 53

SUPPLY CURRENT
vs
FREE-AIR TEMPERATURE

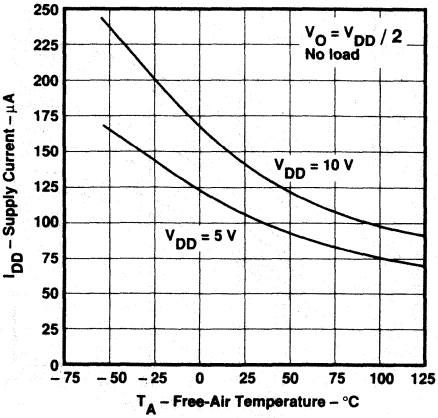


FIGURE 54

NOTE 5: The typical values of input bias current and input offset current below 5 pA were determined mathematically.

TYPICAL CHARACTERISTICS (MEDIUM-BIAS MODE)

SLEW RATE
vs
SUPPLY VOLTAGE

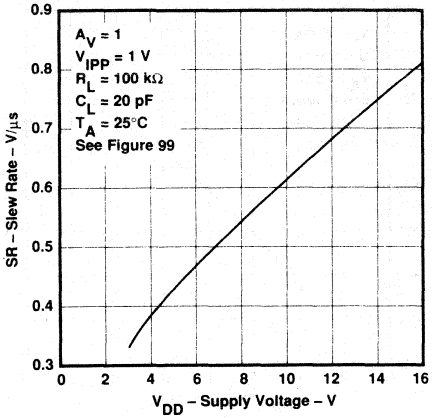


FIGURE 55

SLEW RATE
vs
FREE-AIR TEMPERATURE

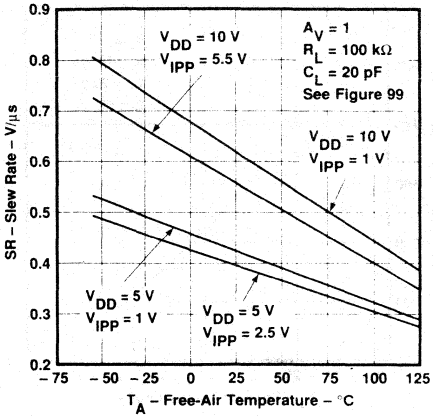


FIGURE56

BIAS SELECT CURRENT
vs
SUPPLY VOLTAGE

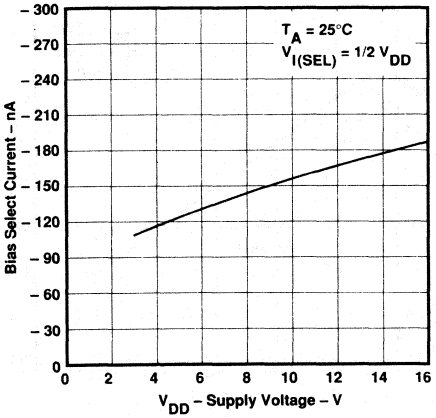


FIGURE 57

MAXIMUM PEAK-TO-PEAK OUTPUT VOLTAGE
vs
FREQUENCY

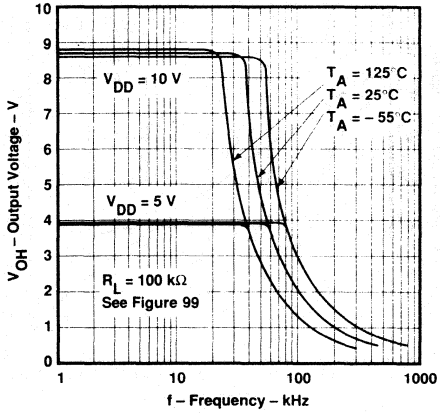


FIGURE 58

TYPICAL CHARACTERISTICS (MEDIUM-BIAS MODE)

UNITY-GAIN BANDWIDTH
vs
FREE-AIR TEMPERATURE

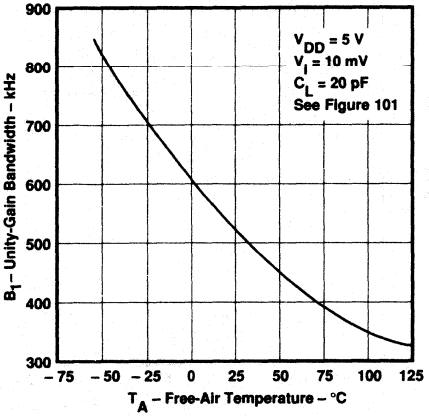


FIGURE 59

UNITY-GAIN BANDWIDTH
vs
SUPPLY VOLTAGE

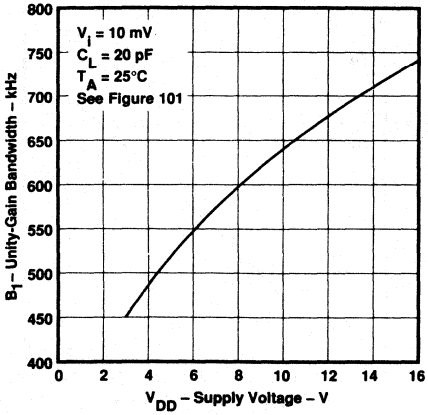


FIGURE 60

LARGE-SIGNAL DIFFERENTIAL VOLTAGE
AMPLIFICATION AND PHASE SHIFT
vs
FREQUENCY

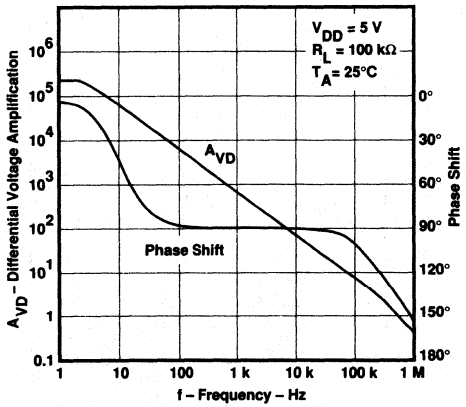


FIGURE 61

LARGE-SIGNAL DIFFERENTIAL VOLTAGE
AMPLIFICATION AND PHASE SHIFT
vs
FREQUENCY

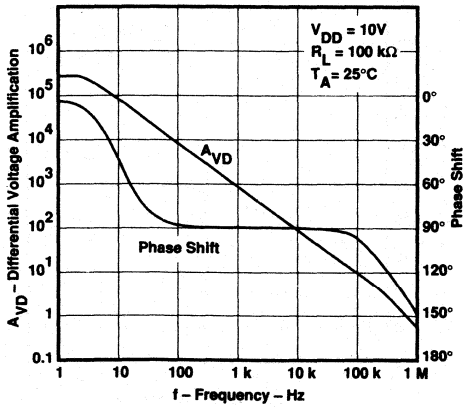


FIGURE 62

TYPICAL CHARACTERISTICS (MEDIUM-BIAS MODE)

PHASE MARGIN
vs
SUPPLY VOLTAGE

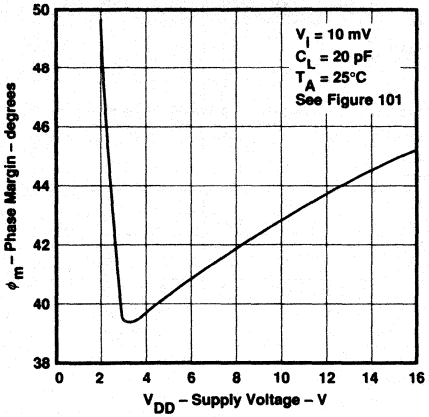


FIGURE 63

PHASE MARGIN
vs
FREE-AIR TEMPERATURE

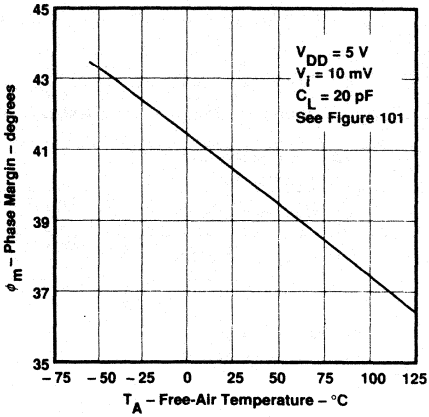


FIGURE 64

PHASE MARGIN
vs
CAPACITIVE LOAD

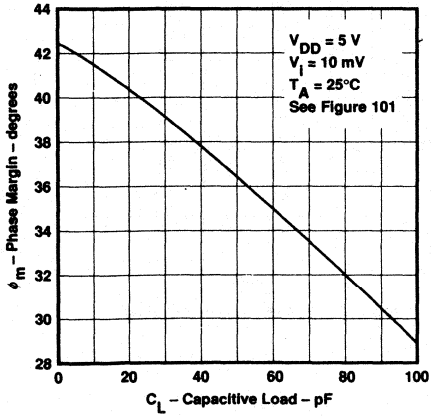


FIGURE 65

EQUIVALENT INPUT NOISE VOLTAGE
vs
FREQUENCY

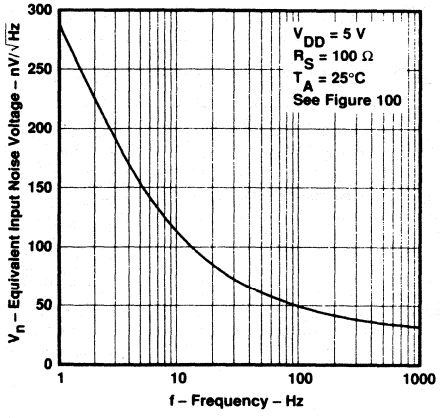


FIGURE 66

LOW-BIAS MODE

electrical characteristics over recommended free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS		C- SUFFIX TYPES V_{DD} = 5 V MIN	TYP	MAX	C- SUFFIX TYPES V_{DD} = 10 V MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage	TLC271C	V_O = 1.4 V, V_{IC} = 0 V, R_S = 50 Ω, R_L = 1 MΩ	25°C		1.1	10		1.1	10	mV
				Full range			12			12	
		TLC271AC		25°C		0.9	5		0.9	5	
				Full range			6.5			6.5	
		TLC271BC		25°C		0.24	2		0.26	2	
				Full range			3			3	
α_{VIO}	Average temperature coefficient of input offset voltage			25°C to 70°C		1.1			1		µV/°C
I_{IO}	Input offset current (see Note 5)		$V_O = V_{DD}/2$, $V_{IC} = V_{DD}/2$	25°C		0.1			0.1		pA
				70°C		7	300		8	300	
I_{IB}	Input bias current (see Note 5)		$V_O = V_{DD}/2$, $V_{IC} = V_{DD}/2$	25°C		0.6			0.7		pA
				70°C		40	600		50	600	
V_{ICR}	Common-mode input voltage range (see Note 6)			25°C	−0.2 to 4	−0.3 to 4.2		−0.2 to 9	−0.3 to 9.2		V
				Full range	−0.2 to 3.5			−0.2 to 8.5			V
V_{OH}	High-level output voltage		V_{ID} = 100 mV, R_L = 1 MΩ	25°C	3.2	4.1		8	8.9		V
				70°C	3	4.2		7.8	8.9		
				0°C	3	4.1		7.8	8.9		
V_{OL}	Low-level output voltage		V_{ID} = −100 mV, I_{OL} = 0	25°C		0	50		0	50	mV
				70°C		0	50		0	50	
				0°C		0	50		0	50	
A_{VD}	Large-signal differential voltage amplification		R_L = 1 MΩ, See Note 7	25°C	50	480		50	800		V/mV
				70°C	50	380		50	660		
				0°C	50	700		50	1100		
CMRR	Common-mode rejection ratio		$V_{IC} = V_{ICR}$min	25°C	65	94		65	97		dB
				70°C	60	95		60	97		
				0°C	60	95		60	97		
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{DD} / \Delta V_{IO}$)		V_{DD} = 5 V to 10 V, V_O = 1.4 V	25°C	70	97		70	97		dB
				70°C	60	98		60	98		
				0°C	60	97		60	97		
$I_{I(SEL)}$	Input current to bias select pin		$V_{I(SEL)} = V_{DD}$	25°C		65			95		nA
I_{DD}	Supply current		No load, $V_O = V_{DD}/2$, $V_{IC} = V_{DD}/2$	25°C		10	17		14	23	µA
				70°C		8	14		11	20	
				0°C		12	21		18	33	

NOTES: 5. The typical values of input bias current and input offset current below 5 pA were determined mathematically.
6. This range also applies to each input individually.
7. At V_{DD} = 5 V, V_O = 0.25 V to 2 V; at V_{DD} = 10 V, V_O = 1 V to 6 V.

LOW-BIAS MODE

electrical characteristics over recommended free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS		I- SUFFIX TYPES V_{DD} = 5 V MIN	TYP	MAX	I- SUFFIX TYPES V_{DD} = 10 V MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage	TLC271I	V_O = 1.4 V, V_{IC} = 0 V, R_S = 50 Ω, R_L = 1 MΩ	25°C		1.1	10		1.1	10	mV
				Full range			13			13	
		TLC271AI		25°C		0.9	5		0.9	5	
				Full range			7			7	
		TLC271BI		25°C		0.24	2		0.26	2	
				Full range			3.5			3.5	
α_{VIO}	Average temperature coefficient of input offset voltage			25°C to 85°C		1.1			1		μV/°C
I_{IO}	Input offset current (see Note 5)		V_O = V_{DD} / 2, V_{IC} = V_{DD} / 2	25°C		0.1			0.1		pA
				85°C		24	1000		26	1000	
I_{IB}	Input bias current (see Note 5)		V_O = V_{DD} / 2, V_{IC} = V_{DD} / 2	25°C		0.6			0.7		pA
				85°C		200	2000		220	2000	
V_{ICR}	Common-mode input voltage range (see Note 6)			25°C	−0.2 to 4	−0.3 to 4.2		−0.2 to 9	−0.3 to 9.2		V
				Full range	−0.2 to 3.5			−0.2 to 8.5			V
V_{OH}	High-level output voltage		V_{ID} = 100 mV, R_L = 1 MΩ	25°C	3.2	4.1		8	8.9		V
				85°C	3	4.2		7.8	8.9		
				−40°C	3	4.1		7.8	8.9		
V_{OL}	Low-level output voltage		V_{ID} = −100 mV, I_{OL} = 0	25°C		0	50		0	50	mV
				85°C		0	50		0	50	
				−40°C		0	50		0	50	
A_{VD}	Large-signal differential voltage amplification		R_L = 1 MΩ, See Note 7	25°C	50	480		50	800		V/mV
				85°C	50	330		50	585		
				−40°C	50	900		50	1550		
CMRR	Common-mode rejection ratio		V_{IC} = V_{ICR}min	25°C	65	94		65	97		dB
				85°C	60	95		60	98		
				−40°C	60	95		60	97		
k_{SVR}	Supply-voltage rejection ratio (ΔV_{DD} / ΔV_{IO})		V_{DD} = 5 V to 10 V, V_O = 1.4 V	25°C	70	97		70	97		dB
				85°C	60	98		60	98		
				−40°C	60	97		60	97		
$I_{I(SEL)}$	Input current to bias select pin		$V_{I(SEL)}$ = V_{DD}	25°C		65			95		nA
I_{DD}	Supply current		No load, V_O = V_{DD} / 2, V_{IC} = V_{DD} / 2	25°C		10	17		14	23	μA
				85°C		7	13		10	18	
				−40°C		16	27		25	43	

NOTES: 5. The typical values of input bias current and input offset current below 5 pA were determined mathematically.
6. This range also applies to each input individually.
7. At V_{DD} = 5 V, V_O = 0.25 V to 2 V; at V_{DD} = 10 V, V_O = 1 V to 6 V.

LOW-BIAS MODE

electrical characteristics over recommended free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		M- SUFFIX TYPES						UNIT
				V_{DD} = 5 V			V_{DD} = 10 V			
				MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	V_O = 1.4 V, V_{IC} = 0 V, R_S = 50 Ω, R_L = 1 MΩ	25°C		1.1	10		1.1	10	mV
			Full range			12			12	
α_{VIO}	Average temperature coefficient of input offset voltage		25°C to 125°C		1.4			1.4		μV/°C
I_{IO}	Input offset current (see Note 5)	$V_O = V_{DD}/2$, $V_{IC} = V_{DD}/2$	25°C		0.1			0.1		pA
			125°C		1.4	15		1.8	15	nA
I_{IB}	Input bias current (see Note 5)	$V_O = V_{DD}/2$, $V_{IC} = V_{DD}/2$	25°C		0.6			0.7		pA
			125°C		9	35		10	35	nA
V_{ICR}	Common-mode input voltage range (see Note 6)		25°C	0 to 4	−0.3 to 4.2		0 to 9	−0.3 to 9.2		V
			Full range	0 to 3.5			0 to 8.5			V
V_{OH}	High-level output voltage	V_{ID} = 100 mV, R_L = 1 MΩ	25°C	3.2	4.1		8	8.9		V
			125°C	3	4.2		7.8	9		
			−55°C	3	4.1		7.8	8.8		
V_{OL}	Low-level output voltage	V_{ID} = −100 mV, I_{OL} = 0	25°C		0	50		0	50	mV
			125°C		0	50		0	50	
			−55°C		0	50		0	50	
A_{VD}	Large-signal differential voltage amplification	R_L = 1 MΩ, See Note 7	25°C	50	480		50	800		V/mV
			125°C	25	200		25	380		
			−55°C	25	950		25	1750		
CMRR	Common-mode rejection ratio	$V_{IC} = V_{ICR}$min	25°C	65	94		65	97		dB
			125°C	60	85		60	91		
			−55°C	60	95		60	97		
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{DD}/\Delta V_{IO}$)	V_{DD} = 5 V to 10 V, V_O = 1.4 V	25°C	70	97		70	97		dB
			125°C	60	98		60	98		
			−55°C	60	97		60	97		
$I_{I(SEL)}$	Input current to bias select pin	$V_{I(SEL)} = V_{DD}$	25°C		65			95		nA
I_{DD}	Supply current	No load, $V_O = V_{DD}/2$, $V_{IC} = V_{DD}/2$	25°C		10	17		14	23	μA
			125°C		7	12		9	15	
			−55°C		17	30		28	48	

NOTES: 5. The typical values of input bias current and input offset current below 5 pA were determined mathematically.
6. This range also applies to each input individually.
7. At V_{DD} = 5 V, V_O = 0.25 V to 2 V; at V_{DD} = 10 V, V_O = 1 V to 6 V.

LOW-BIAS MODE

operating characteristics, V_{DD} = 5 V

PARAMETER		TEST CONDITIONS			C- SUFFIX TYPES MIN	TYP	MAX	UNIT
SR	Slew rate at unity gain	R_L = 1 MΩ, C_L = 20 pF, See Figure 99	V_{IPP} = 1 V	25°C		0.03		V/μs
				70°C		0.03		
				0°C		0.04		
			V_{IPP} = 2.5 V	25°C		0.03		
				70°C		0.02		
				0°C		0.03		
V_n	Equivalent input noise voltage	f = 1 kHz, R_S = 100 Ω, See Figure 100		25°C		68		nV/√Hz
B_{OM}	Maximum output swing bandwidth	$V_O = V_{OH}$, C_L = 20 pF, R_L = 1 MΩ, See Figure 99		25°C		5		kHz
				70°C		4.5		
				0°C		6		
B_1	Unity-gain bandwidth	V_i = 10 mV, C_L = 20 pF, See Figure 101		25°C		85		kHz
				70°C		65		
				0°C		100		
ϕ_m	Phase margin	f = B_1, V_i = 10 mV, C_L = 20 pF, See Figure 101		25°C		34°		
				70°C		30°		
				0°C		36°		

operating characteristics, V_{DD} = 10 V

PARAMETER		TEST CONDITIONS			C- SUFFIX TYPES MIN	TYP	MAX	UNIT
SR	Slew rate at unity gain	R_L = 1 MΩ, C_L = 20 pF, See Figure 99	V_{IPP} = 1 V	25°C		0.05		V/μs
				70°C		0.04		
				0°C		0.05		
			V_{IPP} = 5.5 V	25°C		0.04		
				70°C		0.04		
				0°C		0.05		
V_n	Equivalent input noise voltage	f = 1 kHz, R_S = 100 Ω, See Figure 100		25°C		68		nV/√Hz
B_{OM}	Maximum output swing bandwidth	$V_O = V_{OH}$, C_L = 20 pF, R_L = 1 MΩ, See Figure 99		25°C		1		kHz
				70°C		0.9		
				0°C		1.3		
B_1	Unity-gain bandwidth	V_i = 10 mV, C_L = 20 pF, See Figure 101		25°C		110		kHz
				70°C		90		
				0°C		125		
ϕ_m	Phase margin	f = B_1, V_i = 10 mV, C_L = 20 pF, See Figure 101		25°C		38°		
				70°C		34°		
				0°C		40°		

LOW-BIAS MODE

operating characteristics, V_{DD} = 5 V

PARAMETER		TEST CONDITIONS			I- SUFFIX TYPES MIN	TYP	MAX	UNIT
SR	Slew rate at unity gain	R_L = 1MΩ, C_L = 20 pF, See Figure 99	V_{IPP} = 1 V	25°C		0.03		V/μs
				85°C		0.03		
				– 40°C		0.04		
			V_{IPP} = 2.5 V	25°C		0.03		
				85°C		0.02		
				– 40°C		0.04		
V_n	Equivalent input noise voltage	f = 1 kHz, R_S = 100 Ω, See Figure 100		25°C		68		nV/√Hz
B_{OM}	Maximum output swing bandwidth	V_O = V_{OH}, C_L = 20 pF, R_L = 1MΩ, See Figure 99		25°C		5		kHz
				85°C		4		
				– 40°C		7		
B_1	Unity-gain bandwidth	V_i = 10 mV, C_L = 20 pF, See Figure 101		25°C		85		kHz
				85°C		55		
				– 40°C		130		
ϕ_m	Phase margin	f = B_1, V_i = 10 mV, C_L = 20 pF, See Figure 101		25°C		34°		
				85°C		28°		
				– 40°C		38°		

operating characteristics, V_{DD} = 10 V

PARAMETER		TEST CONDITIONS			I- SUFFIX TYPES MIN	TYP	MAX	UNIT
SR	Slew rate at unity gain	R_L = 1 MΩ, C_L = 20 pF, See Figure 99	V_{IPP} = 1 V	25°C		0.05		V/μs
				85°C		0.03		
				– 40°C		0.06		
			V_{IPP} = 5.5 V	25°C		0.04		
				85°C		0.03		
				– 40°C		0.05		
V_n	Equivalent input noise voltage	f = 1 kHz, R_S = 100 Ω, See Figure 100		25°C		68		nV/√Hz
B_{OM}	Maximum output swing bandwidth	V_O = V_{OH}, C_L = 20 pF, R_L = 1 MΩ, See Figure 99		25°C		1		kHz
				85°C		0.8		
				– 40°C		1.4		
B_1	Unity-gain bandwidth	V_i = 10 mV, C_L = 20 pF, See Figure 101		25°C		110		kHz
				85°C		80		
				– 40°C		155		
ϕ_m	Phase margin	f = B_1, V_i = 10 mV, C_L = 20 pF, See Figure 101		25°C		38°		
				85°C		32°		
				– 40°C		42°		

LOW-BIAS MODE

operating characteristics, V_{DD} = 5 V

PARAMETER		TEST CONDITIONS			M- SUFFIX TYPES MIN	TYP	MAX	UNIT
SR	Slew rate at unity gain	R_L = 1 MΩ, C_L = 20 pF, See Figure 99	V_{IPP} = 1 V	25°C		0.03		V/μs
				125°C		0.02		
				−55°C		0.04		
			V_{IPP} = 2.5 V	25°C		0.03		
				125°C		0.02		
				−55°C		0.04		
V_n	Equivalent input noise voltage	f = 1 kHz, R_S = 100 Ω, See Figure 100		25°C		68		nV/√Hz
B_{OM}	Maximum output swing bandwidth	$V_O = V_{OH}$, C_L = 20 pF, R_L = 1 MΩ, See Figure 99		25°C		5		kHz
				125°C		3		
				−55°C		8		
B_1	Unity-gain bandwidth	V_i = 10 mV, C_L = 20 pF, See Figure 101		25°C		85		kHz
				125°C		45		
				−55°C		140		
ϕ_m	Phase margin	f = B_1, V_i = 10 mV, C_L = 20 pF, See Figure 101		25°C		34°		
				125°C		25°		
				−55°C		39°		

operating characteristics, V_{DD} = 10 V

PARAMETER		TEST CONDITIONS			M- SUFFIX TYPES MIN	TYP	MAX	UNIT
SR	Slew rate at unity gain	R_L = 1 MΩ, C_L = 20 pF, See Figure 99	V_{IPP} = 1 V	25°C		0.05		V/μs
				125°C		0.03		
				−55°C		0.06		
			V_{IPP} = 5.5 V	25°C		0.04		
				125°C		0.03		
				−55°C		0.06		
V_n	Equivalent input noise voltage	f = 1 kHz, R_S = 100 Ω, See Figure 100		25°C		68		nV/√Hz
B_{OM}	Maximum output swing bandwidth	$V_O = V_{OH}$, C_L = 20 pF, R_L = 1 MΩ, See Figure 99		25°C		1		kHz
				125°C		0.7		
				−55°C		1.5		
B_1	Unity-gain bandwidth	V_i = 10 mV, C_L = 20 pF, See Figure 101		25°C		110		kHz
				125°C		70		
				−55°C		165		
ϕ_m	Phase margin	f = B_1, V_i = 10 mV, C_L = 20 pF, See Figure 101		25°C		38°		
				125°C		29°		
				−55°C		43°		

TYPICAL CHARACTERISTICS (LOW-BIAS MODE)

DISTRIBUTION OF TLC271
INPUT OFFSET VOLTAGE

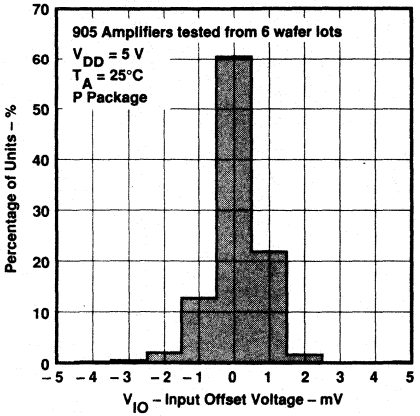


FIGURE 67

DISTRIBUTION OF TLC271
INPUT OFFSET VOLTAGE

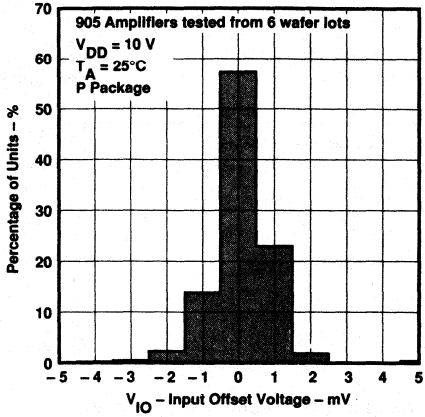


FIGURE 68

DISTRIBUTION OF TLC271
INPUT OFFSET VOLTAGE
TEMPERATURE COEFFICIENT

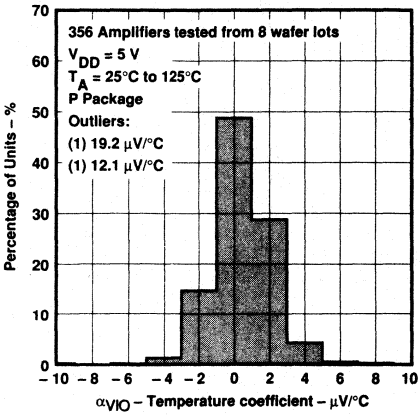


FIGURE 69

DISTRIBUTION OF TLC271
INPUT OFFSET VOLTAGE
TEMPERATURE COEFFICIENT

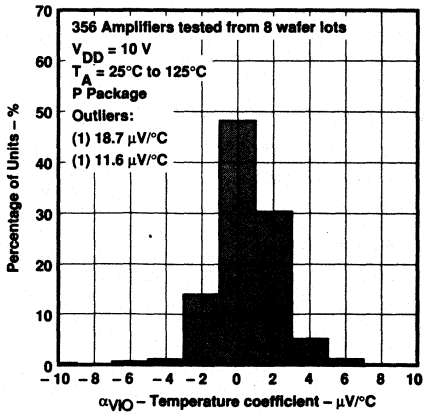


FIGURE 70

TYPICAL CHARACTERISTICS (LOW-BIAS MODE)

HIGH-LEVEL OUTPUT VOLTAGE
vs
HIGH-LEVEL OUTPUT CURRENT

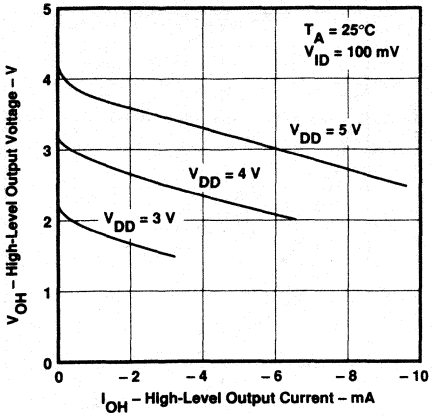


FIGURE 71

HIGH-LEVEL OUTPUT VOLTAGE
vs
HIGH-LEVEL OUTPUT CURRENT

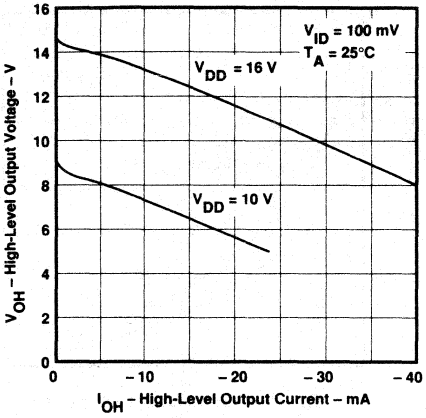


FIGURE 72

HIGH-LEVEL OUTPUT VOLTAGE
vs
SUPPLY VOLTAGE

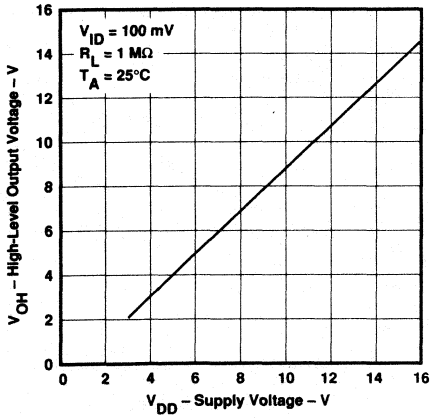


FIGURE 73

HIGH-LEVEL OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE

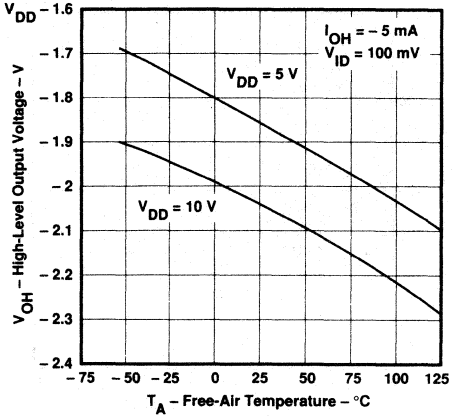


FIGURE 74

TYPICAL CHARACTERISTICS (LOW-BIAS MODE)

LOW-LEVEL OUTPUT VOLTAGE
vs
COMMON-MODE INPUT VOLTAGE

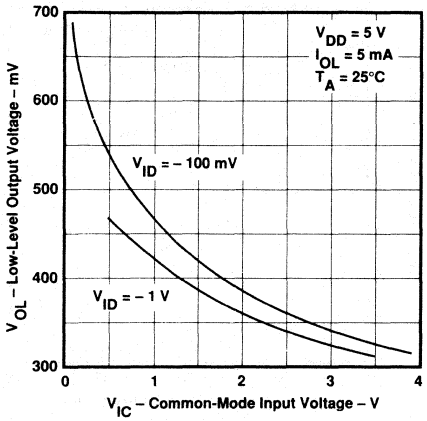


FIGURE 75

LOW-LEVEL OUTPUT VOLTAGE
vs
COMMON-MODE INPUT VOLTAGE

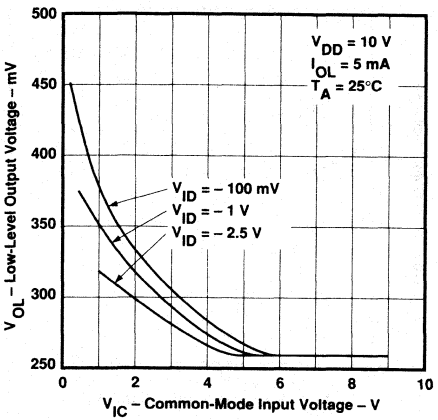


FIGURE 76

LOW-LEVEL OUTPUT VOLTAGE
vs
DIFFERENTIAL INPUT VOLTAGE

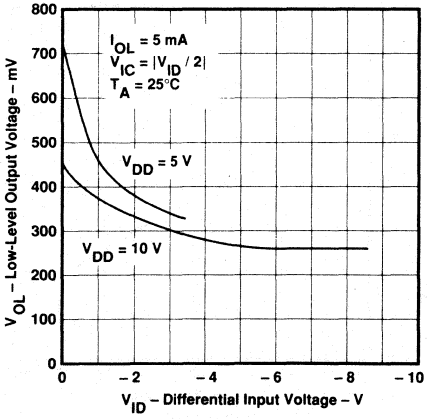


FIGURE 77

LOW-LEVEL OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE

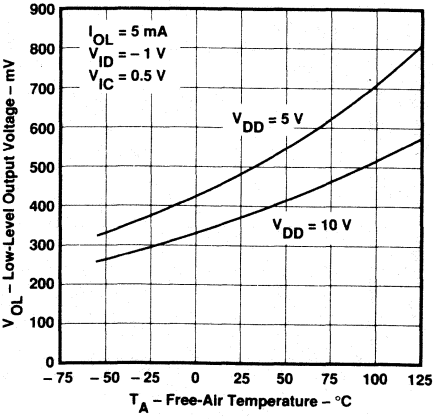


FIGURE 78

TYPICAL CHARACTERISTICS (LOW-BIAS MODE)

LOW-LEVEL OUTPUT VOLTAGE
vs
LOW-LEVEL OUTPUT CURRENT

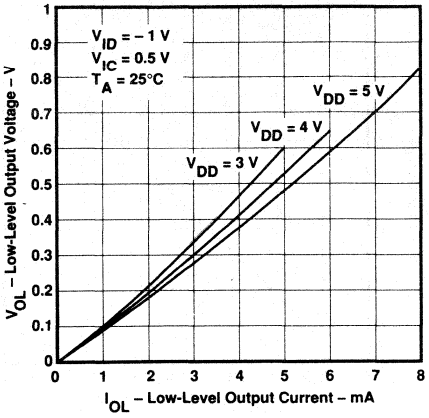


FIGURE 79

LOW-LEVEL OUTPUT VOLTAGE
vs
LOW-LEVEL OUTPUT CURRENT

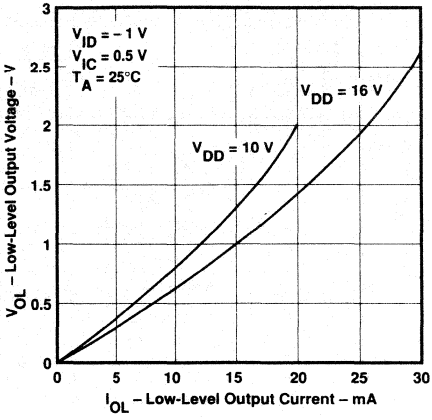


FIGURE 80

LARGE-SIGNAL
DIFFERENTIAL VOLTAGE AMPLIFICATION
vs
SUPPLY VOLTAGE

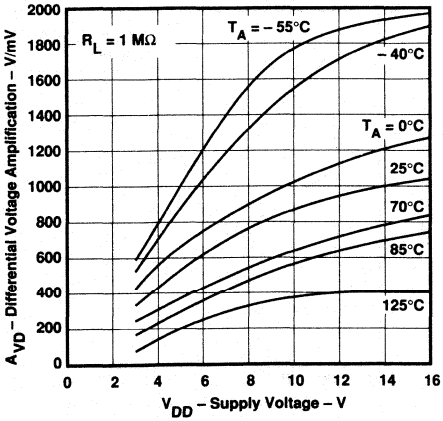


FIGURE 81

LARGE-SIGNAL
DIFFERENTIAL VOLTAGE AMPLIFICATION
vs
FREE-AIR TEMPERATURE

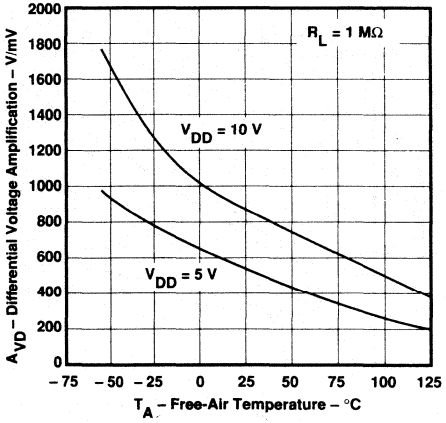


FIGURE 82

TYPICAL CHARACTERISTICS (LOW-BIAS MODE)

INPUT BIAS CURRENT AND INPUT OFFSET CURRENT
vs
FREE-AIR TEMPERATURE

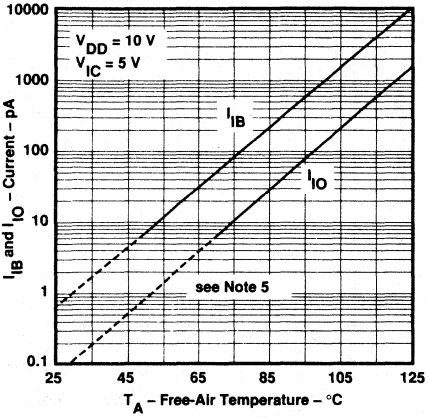


FIGURE 83

MAXIMUM INPUT VOLTAGE
vs
SUPPLY VOLTAGE

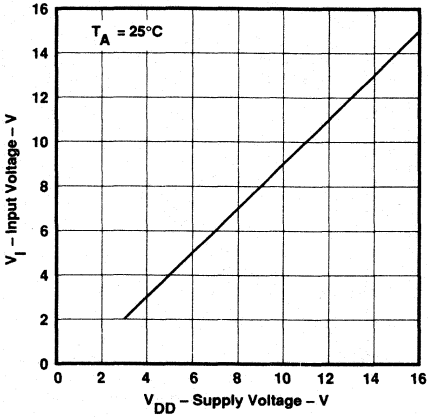


FIGURE 84

SUPPLY CURRENT
vs
SUPPLY VOLTAGE

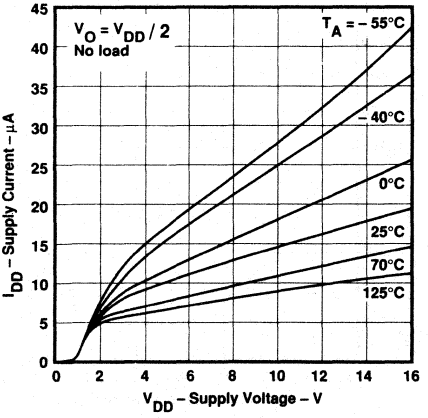


FIGURE 85

SUPPLY CURRENT
vs
FREE-AIR TEMPERATURE

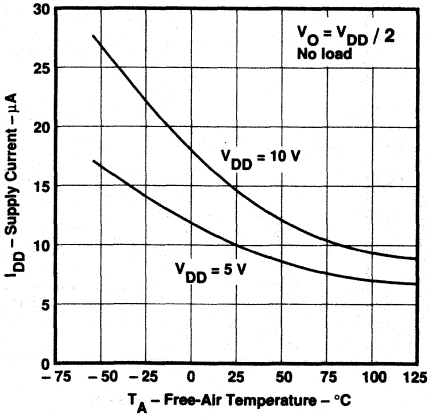


FIGURE 86

NOTE 5: The typical values of input bias current and input offset current below 5 pA were determined mathematically.

TYPICAL CHARACTERISTICS (LOW-BIAS MODE)

SLEW RATE
vs
SUPPLY VOLTAGE

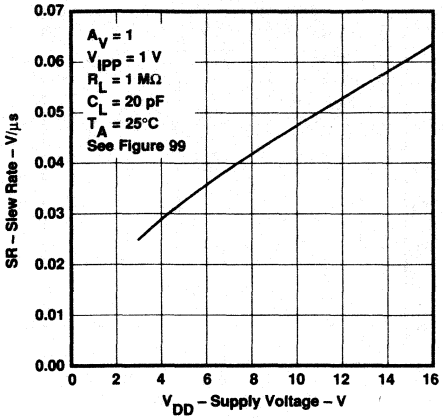


FIGURE 87

SLEW RATE
vs
FREE-AIR TEMPERATURE

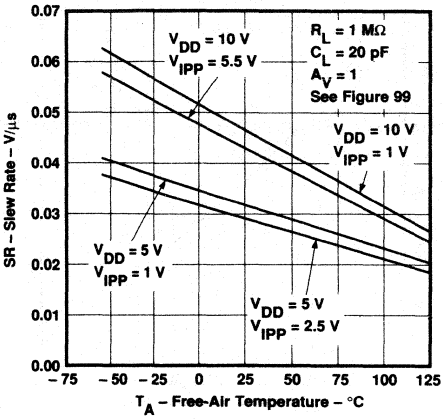


FIGURE 88

BIAS SELECT CURRENT
vs
SUPPLY VOLTAGE

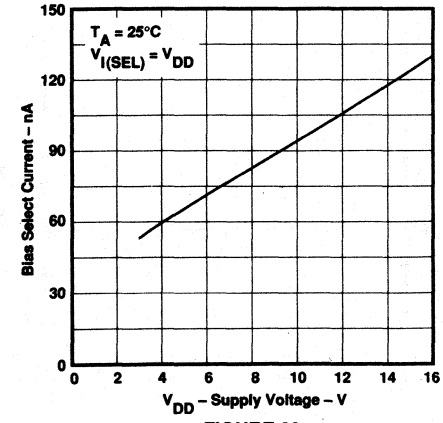


FIGURE 89

MAXIMUM PEAK-TO-PEAK OUTPUT VOLTAGE
vs
FREQUENCY

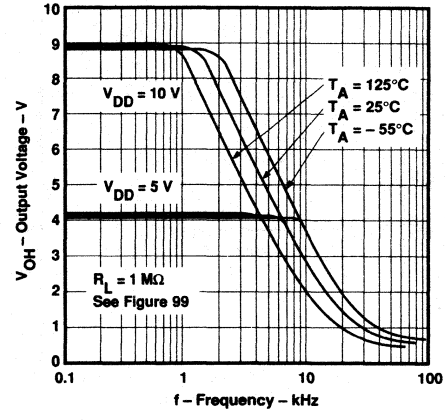


FIGURE 90

TYPICAL CHARACTERISTICS (LOW-BIAS MODE)

UNITY-GAIN BANDWIDTH
vs
FREE-AIR TEMPERATURE

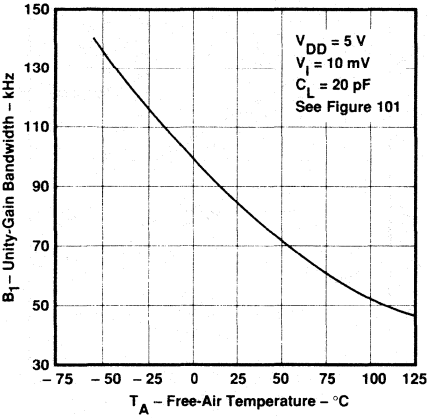


FIGURE 91

UNITY-GAIN BANDWIDTH
vs
SUPPLY VOLTAGE

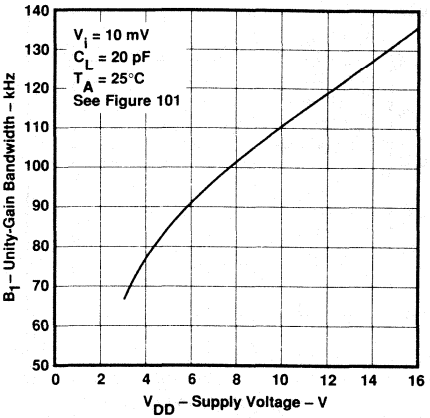


FIGURE 92

LARGE-SIGNAL DIFFERENTIAL VOLTAGE
AMPLIFICATION AND PHASE SHIFT
vs
FREQUENCY

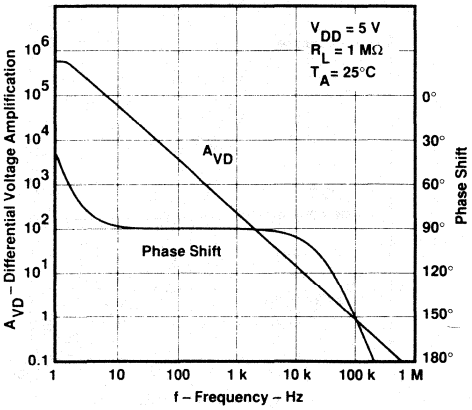


FIGURE 93

LARGE-SIGNAL DIFFERENTIAL VOLTAGE
AMPLIFICATION AND PHASE SHIFT
vs
FREQUENCY

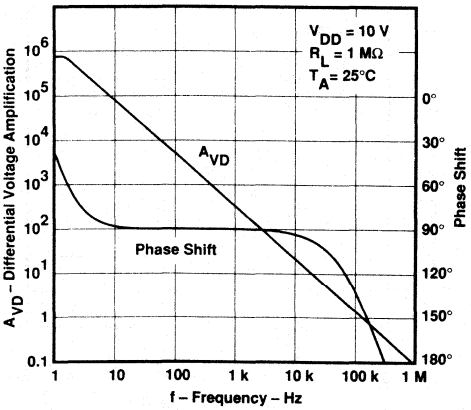


FIGURE 94

TYPICAL CHARACTERISTICS (LOW-BIAS MODE)

PHASE MARGIN
vs
SUPPLY VOLTAGE

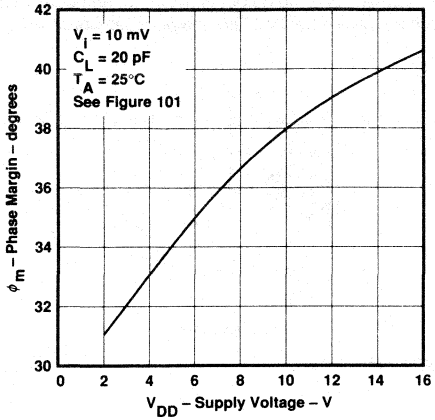


FIGURE 95

PHASE MARGIN
vs
FREE-AIR TEMPERATURE

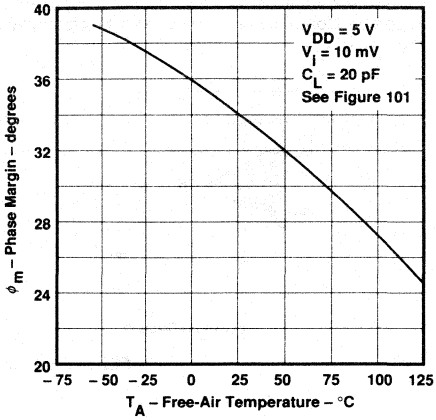


FIGURE 96

PHASE MARGIN
vs
CAPACITIVE LOAD

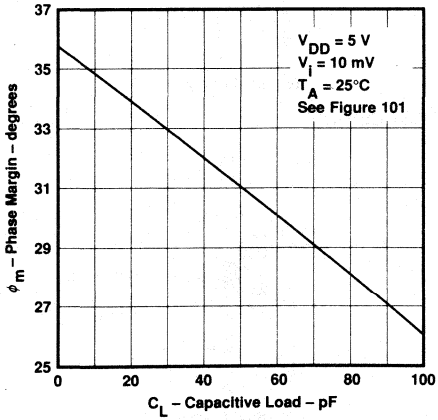


FIGURE 97

EQUIVALENT INPUT NOISE VOLTAGE
vs
FREQUENCY

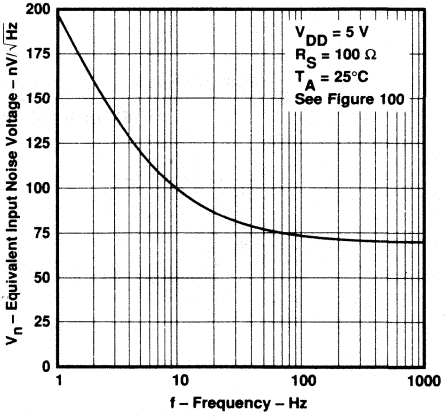
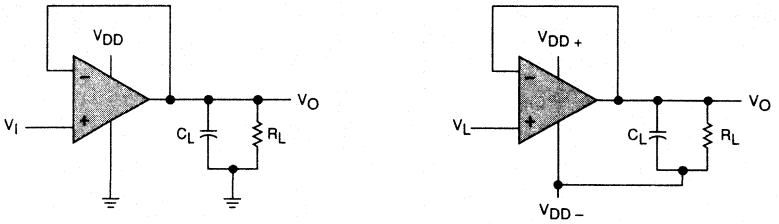


FIGURE 98

PARAMETER MEASUREMENT INFORMATION

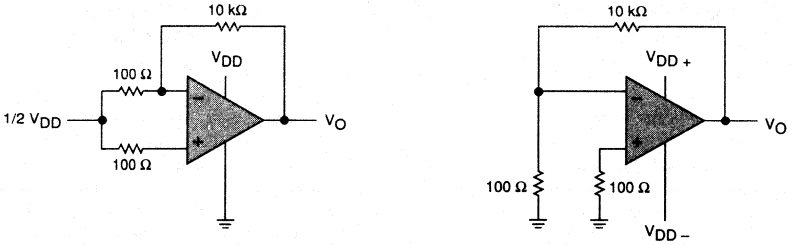
single-supply versus split-supply test circuits

Because the TLC271 is optimized for single-supply operation, circuit configurations used for the various tests often present some inconvenience since the input signal, in many cases, must be offset from ground. This inconvenience can be avoided by testing the device with split supplies and the output load tied to the negative rail. A comparison of single-supply versus split-supply test circuits is shown below. The use of either circuit will give the same result.



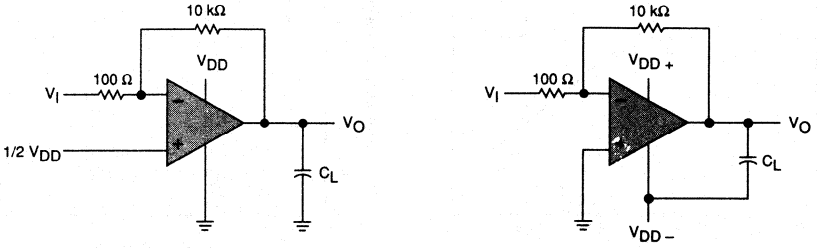
(a) Single-Supply (b) Split-Supply

FIGURE 99. UNITY-GAIN AMPLIFIER



(a) Single-Supply (b) Split-Supply

FIGURE 100. NOISE TEST CIRCUIT



(a) Single-Supply (b) Split-Supply

FIGURE 101. GAIN-OF-100 INVERTING AMPLIFIER

PARAMETER MEASUREMENT INFORMATION

input bias current

Because of the high input impedance of the TLC271 op amp, attempts to measure the input bias current can result in erroneous readings. The bias current at normal room ambient temperature is typically less than 1 pA, a value that is easily exceeded by leakages on the test socket. Two suggestions are offered to avoid erroneous measurements:

1. Isolate the device from other potential leakage sources. Use a grounded shield around and between the device inputs (see Figure 102). Leakages that would otherwise flow to the inputs will be shunted away.

2. Compensate for the leakage of the test socket by actually performing an input bias current test (using a picoammeter) with no device in the test socket. The actual input bias current can then be calculated by subtracting the "open-socket" leakage readings from the readings obtained with a device in the test socket.

   One word of caution . . . many automatic testers as well as some bench-top op amp testers use the servo-loop technique with a resistor in series with the device input to measure the input bias current (the voltage drop across the series resistor is measured and the bias current is calculated). This method requires that a device be inserted into the test socket to obtain a correct reading; therefore, an "open-socket" reading is not feasible using this method.

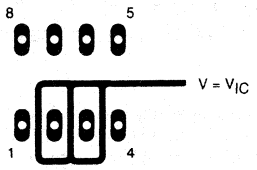


FIGURE 102. ISOLATION METAL AROUND DEVICE INPUTS (JG AND P DUAL-IN-LINE PACKAGE)

low-level output voltage

To obtain low-supply-voltage operation, some compromise was necessary in the input stage. This compromise results in the device low-level output being dependent on both the common-mode input voltage level as well as the differential input voltage level. When attempting to correlate low-level output readings with those quoted in the electrical specifications, these two conditions should be observed. If conditions other than these are to be used, please refer to the Typical Characteristics section of this data sheet.

input offset voltage temperature coefficient

Erroneous readings often result from attempts to measure temperature coefficient of input offset voltage. This parameter is actually a calculation using input offset voltage measurements obtained at two different temperatures. When one (or both) of the temperatures is below freezing, moisture can collect on both the device and the test socket. This moisture will result in leakage and contact resistance which can cause erroneous input offset voltage readings. The isolation techniques previously mentioned have no effect on the leakage since the moisture also covers the isolation metal itself, thereby rendering it useless. It is suggested that these measurements be performed at temperatures above freezing to minimize error.

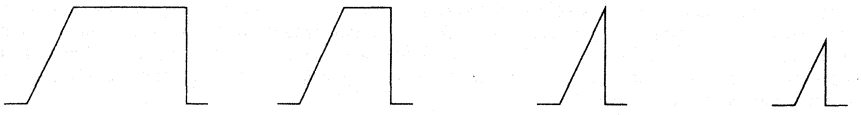
full power response

Full power response, the frequency above which the op amp slew rate limits the output voltage swing, is often specified two ways . . . full-linear response and full-peak response. The full-linear response is generally

PARAMETER MEASUREMENT INFORMATION

measured by monitoring the distortion level of the output while increasing the frequency of a sinusoidal input signal until the maximum frequency is found above which the output contains significant distortion. The full-peak response is defined as the maximum output frequency, without regard to distortion, above which full peak-to-peak output swing cannot be maintained.

Because there is no industry-wide accepted value for "significant" distortion, the full-peak response is specified in this data sheet and is measured using the circuit of Figure 99. The initial setup involves the use of a sinusoidal input to determine the maximum peak-to-peak output of the device (the amplitude of the sinusoidal wave is increased until clipping occurs). The sinusoidal wave is then replaced with a square wave of the same amplitude. The frequency is then increased until the maximum peak-to-peak output can no longer be maintained (Figure 103). A square wave is used to allow a more accurate determination of the point at which the maximum peak-to-peak output is reached.



(a) f = 100 Hz (b) B_{OM} > f > 100 Hz (c) f = B_{OM} (d) f > B_{OM}

FIGURE 103. FULL-POWER-RESPONSE OUTPUT SIGNAL

test time

Inadequate test time is a frequent problem, especially when testing CMOS devices in a high-volume, short-test-time environment. Internal capacitances are inherently higher in CMOS than in bipolar and BiFET devices, and require longer test times than their bipolar and BiFET counterparts. The problem becomes more pronounced with reduced supply levels and lower temperatures.

TYPICAL APPLICATION DATA

single-supply operation

While the TLC271 will perform well using dual power supplies (also called balanced or split supplies), the design is optimized for single-supply operation. This includes an input common mode voltage range that encompasses ground as well as an output voltage range that pulls down to ground. The supply voltage range extends down to 3 V (C- suffix types), thus allowing operation with supply levels commonly available for TTL and HCMOS; however, for maximum dynamic range, 16-V single-supply operation is recommended.

Many single-supply applications require that a voltage be applied to one input to establish a reference level that is above ground. A resistive voltage divider is usually sufficient to establish this reference level (see Figure 104). The low input bias current consumption of the TLC271 permits the use of very large resistive values to implement the voltage divider, thus minimizing power consumption.

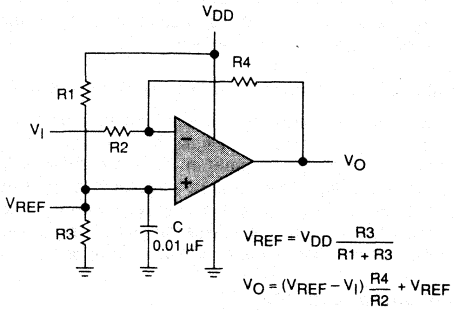
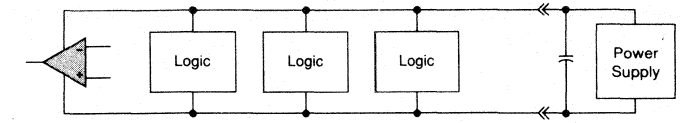


FIGURE 104. INVERTING AMPLIFIER WITH VOLTAGE REFERENCE

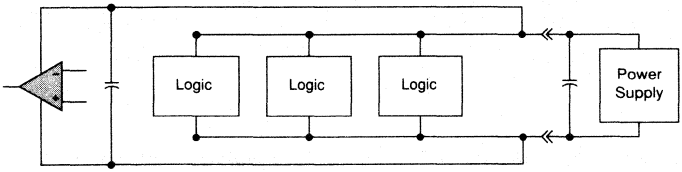
TYPICAL APPLICATION DATA

The TLC271 works well in conjunction with digital logic; however, when powering both linear devices and digital logic from the same power supply, the following precautions are recommended:

1. Power the linear devices from separate bypassed supply lines (see Figure 105); otherwise the linear device supply rails can fluctuate due to voltage drops caused by high switching currents in the digital logic.
2. Use proper bypass techniques to reduce the probability of noise-induced errors. Single capacitive decoupling is often adequate; however, RC decoupling may be necessary in high-frequency applications.



(a) Common Supply Rails

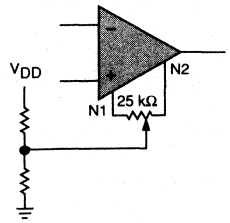


(b) Separate Bypassed Supply Rails (preferred)

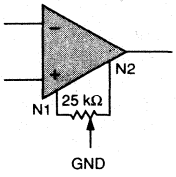
FIGURE 105. COMMON VERSUS SEPARATE SUPPLY RAILS

input offset voltage nulling

The TLC271 offers external input offset null control. Nulling of the input offset voltage may be achieved by adjusting a 25-kΩ potentiometer connected between the offset null terminals with the wiper connected as shown in Figure 106. The amount of nulling range varies with the bias selection. In the high-bias mode, the nulling range will allow the maximum offset voltage specified to be trimmed to zero. In low-bias and medium-bias modes, total nulling may not be possible.



(a) Single-Supply



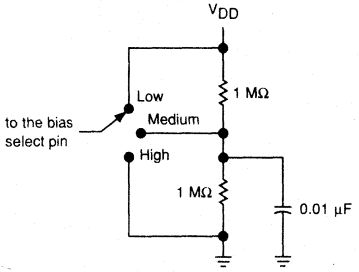
(b) Split-Supply

FIGURE 106. INPUT OFFSET VOLTAGE NULL CIRCUIT

TYPICAL APPLICATION DATA

bias selection

Bias selection is achieved by connecting the bias select pin to one of the three voltage levels (see Figure 107). For medium-bias applications, it is recommended that the bias select pin be connected to the mid-point between the supply rails. This is a simple procedure in split-supply applications, since this point is ground. In single-supply applications, the medium-bias mode will necessitate using a voltage divider as indicated. The use of large-value resistors in the voltage divider will reduce the current drain of the divider from the supply line. However, large-value resistors used in conjunction with a large-value capacitor will require significant time to charge up to the supply midpoint after the supply is switched on. A voltage other than the mid-point may be used if it is within the voltages specified in the following table.



BIAS MODE	BIAS SELECT VOLTAGE (Single Supply)
LOW	V_{DD}
MEDIUM	1 V to V_{DD} – 1 V
HIGH	GND

FIGURE 107. BIAS SELECTION FOR SINGLE-SUPPLY APPLICATIONS

input characteristics

The TLC271 is specified with a minimum and a maximum input voltage that, if exceeded at either input, could cause the device to malfunction. Exceeding this specified range is a common problem, especially in single-supply operation. Note that the lower range limit includes the negative rail, while the upper range limit is specified at V_{DD} – 1 V at T_A = 25°C and at V_{DD} – 1.5 V at all other temperatures.

The use of the polysilicon-gate process and the careful input circuit design gives the TLC271 very good input offset voltage drift characteristics relative to conventional metal-gate processes. Offset voltage drift in CMOS devices is highly influenced by threshold voltage shifts caused by polarization of the phosphorus dopant implanted in the oxide. Placing the phosphorus dopant in a conductor (such as a polysilicon gate) alleviates the polarization problem, thus reducing threshold voltage shifts by more than an order of magnitude. The offset voltage drift with time has been calculated to be typically 0.1 μV/month, including the first month of operation.

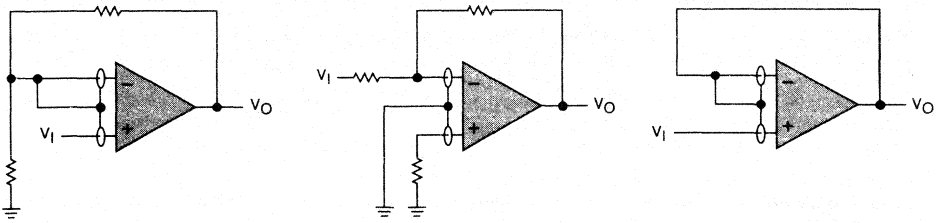
Because of the extremely high input impedance and resulting low bias current requirements, the TLC271 is well suited for low-level signal processing; however, leakage currents on printed circuit boards and sockets can easily exceed bias current requirements and cause a degradation in device performance. It is good practice to include guard rings around inputs (similar to those of Figure 102 in the PARAMETER MEASUREMENT INFORMATION section). These guards should be driven from a low-impedance source at the same voltage level as the common-mode input (see Figure 108).

The inputs of any unused amplifiers should be tied to ground to avoid possible oscillation.

noise performance

The noise specifications in op amp circuits are greatly dependent on the current in the first-stage differential amplifier. The low input bias current requirements of the TLC271 results in a very low noise current, which is insignificant in most applications. This feature makes the devices especially favorable over bipolar devices when using values of circuit impedance greater than 50 kΩ, since bipolar devices exhibit greater noise currents.

TYPICAL APPLICATION DATA



(a) Noninverting Amplifier (b) Inverting Amplifier (c) Unity Gain Amplifier

Figure 108. GUARD RING SCHEMES

feedback

Op amp circuits nearly always employ feedback, and since feedback is the first prerequisite for oscillation, a little caution is appropriate. Most oscillation problems result from driving capacitive loads and ignoring stray input capacitance. A small-value capacitor connected in parallel with the feedback resistor is an effective remedy (see Figure 109). The value of this capacitor is optimized empirically.

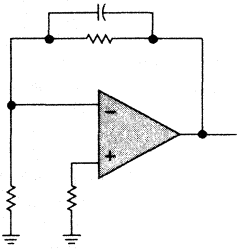


FIGURE 109. COMPENSATION FOR INPUT CAPACITANCE

electrostatic discharge protection

The TLC271 incorporates an internal electrostatic discharge (ESD) protection circuit that will prevent functional failures at voltages up to 2000 V as tested under MIL-STD-883C, Method 3015.2. Care should be exercised, however, when handling these devices as exposure to ESD may result in the degradation of the device parametric performance. The protection circuit also causes the input bias currents to be temperature dependent and have the characteristics of a reverse-biased diode.

latchup

Because CMOS devices are susceptible to latchup due to their inherent parasitic thyristors, the TLC271 inputs and output were designed to withstand −100-mA surge currents without sustaining latchup; however, techniques should be used to reduce the chance of latchup whenever possible. Internal protection diodes should not by design be forward biased. Applied input and output voltage should not exceed the supply voltage by more than 300 mV. Care should be exercised when using capacitive coupling on pulse generators. Supply transients should be shunted by the use of decoupling capacitors (0.1 μF typical) located across the supply rails as close to the device as possible.

The current path established if latchup occurs is usually between the positive supply rail and ground and can be triggered by surges on the supply lines and / or voltages on either the output or inputs that exceed the supply voltage. Once latchup occurs, the current flow is limited only by the impedance of the power supply and the forward resistance of the parasitic thyristor and usually results in the destruction of the device. The chance of latchup occuring increases with increasing temperature and supply voltages.

output characteristics

The output stage of the TLC271 is designed to sink and source relatively high amounts of current (see typical characteristics). If the output is subjected to a short-circuit condition, this high current capability can cause device damage under certain conditions. Output current capability increases with supply voltage.

All operating characteristics of the TLC271 were measured using a 20-pF load. The devices will drive higher capacitive loads; however, as output load capacitance increases, the resulting response pole occurs at lower frequencies, thereby causing ringing, peaking, or even oscillation (see Figures below). In many cases, adding some compensation in the form of a series resistor in the feedback loop will alleviate the problem.

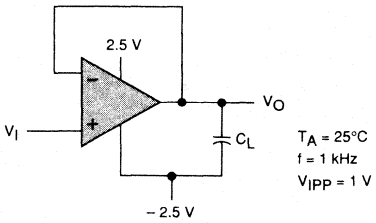
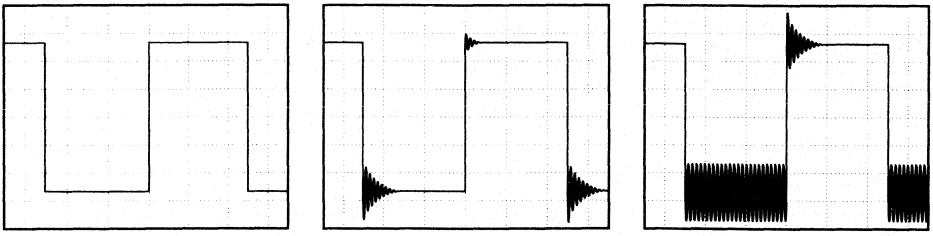
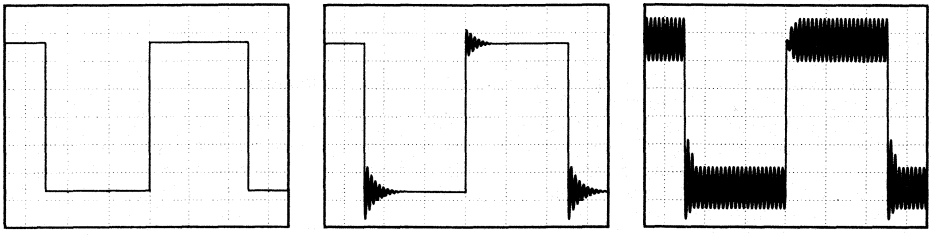


FIGURE 110. TEST CIRCUIT FOR OUTPUT CHARACTERISTICS



(a) C_L = 20 pF, R_L = no load | (a) C_L = 130 pF, R_L = no load | (a) C_L = 150 pF, R_L = no load

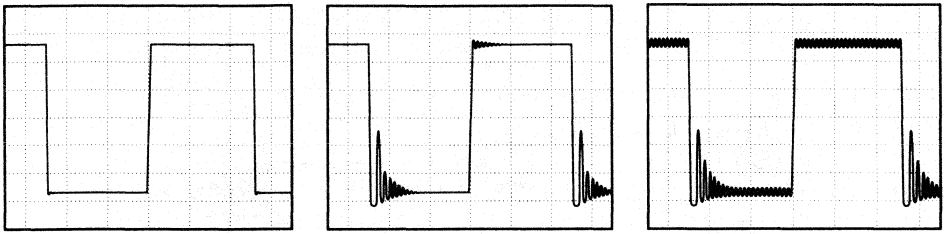
FIGURE 111. EFFECT OF CAPACITIVE LOADS IN HIGH-BIAS MODE



(a) C_L = 20 pF, R_L = no load | (a) C_L = 170 pF, R_L = no load | (a) C_L = 190 pF, R_L = no load

FIGURE 112. EFFECT OF CAPACITIVE LOADS IN MEDIUM-BIAS MODE

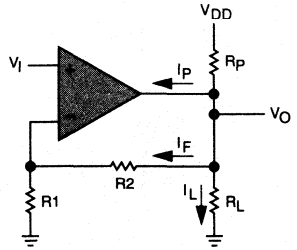
TYPICAL APPLICATION DATA



(a) C_L = 20 pF, R_L = no load (a) C_L = 260 pF, R_L = no load (a) C_L = 310 pF, R_L = no load

FIGURE 113. EFFECT OF CAPACITIVE LOADS IN LOW-BIAS MODE

Although the TLC271 possesses excellent high-level output voltage and current capability, methods are available for boosting this capability, if needed. The simplest method involves the use of a pull-up resistor (R_P) connected from the output to the positive supply rail (see Figure 114). There are two disadvantages to the use of this circuit. First, the NMOS pull-down transistor, N4 (see equivalent schematic) must sink a comparatively large amount of current. In this circuit, N4 behaves like a linear resistor with an on-resistance between approximately 60 Ω and 180 Ω, depending on how hard the op amp input is driven. With very low values of R_P, a voltage offset from 0 V at the output will occur. Secondly, pull-up resistor R_P acts as a drain load to N4 and the gain of the op amp is reduced at output voltage levels where N5 is not supplying the output current.

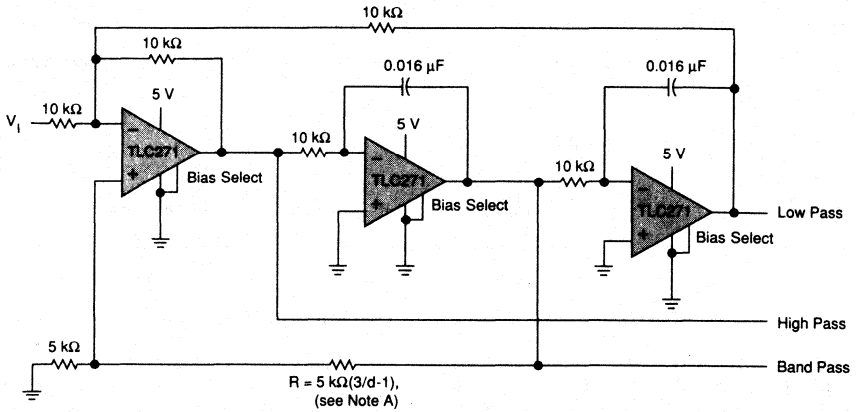


$$R_P = \frac{V_{DD} - V_O}{I_F + I_L + I_P}$$

I_P = Pull-up curent required by the op amp (typically 500 μA)

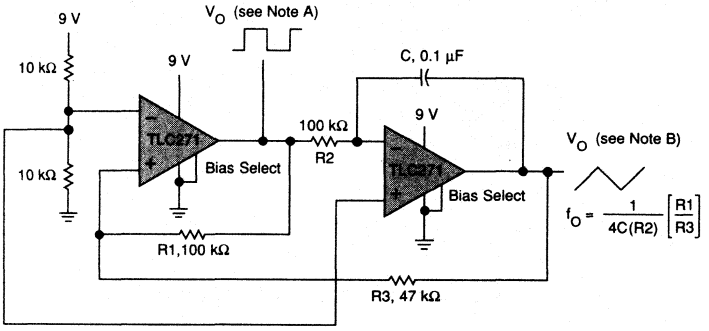
FIGURE 114. RESISTIVE PULL-UP TO INCREASE V_{OH}

TYPICAL APPLICATION DATA (HIGH-BIAS MODE)



NOTES: A. d = damping factor, 1/Q
B. Normalized to 10 kΩ and f_C = 1 kHz

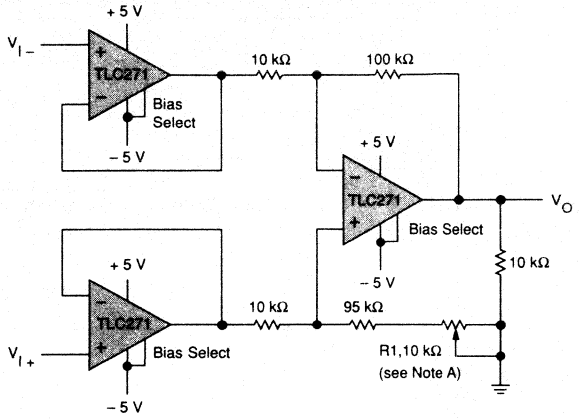
FIGURE 115. STATE VARIABLE FILTER



NOTES: A. V_{OPP} = 8 V
B. V_{OPP} = 4 V

FIGURE 116. SINGLE-SUPPLY FUNCTION GENERATOR

TYPICAL APPLICATION DATA (HIGH-BIAS MODE)



NOTE A: CMRR Adjustment (must be noninductive).

FIGURE 117. LOW-POWER INSTRUMENTATION AMPLIFIER

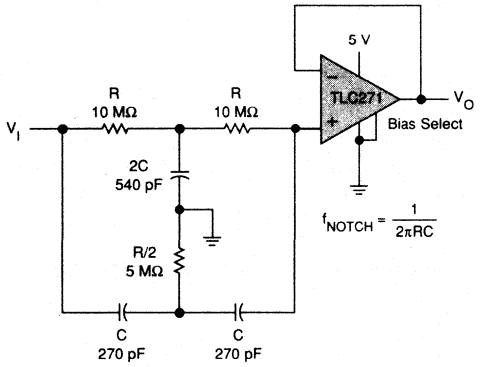
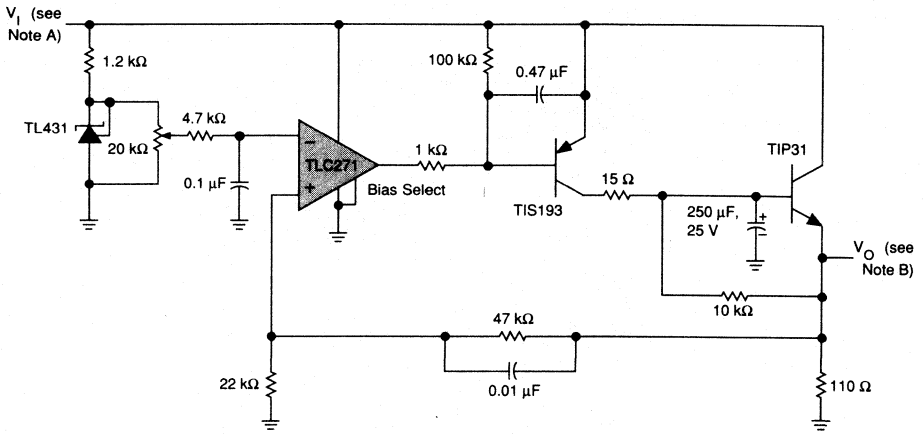


FIGURE 118. SINGLE-SUPPLY TWIN-T NOTCH FILTER

TYPICAL APPLICATION DATA (HIGH-BIAS MODE)



NOTES: A. V_I = 3.5 to 15 V
B. V_O = 2.0 V, 0 to 1 A

FIGURE 119. LOGIC ARRAY POWER SUPPLY

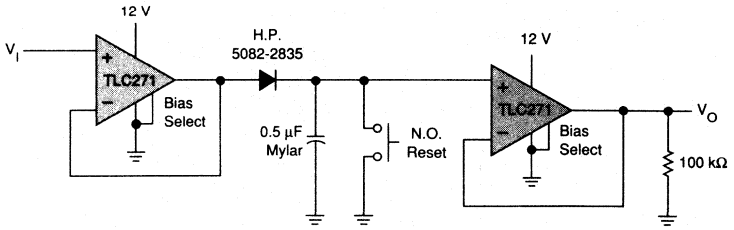
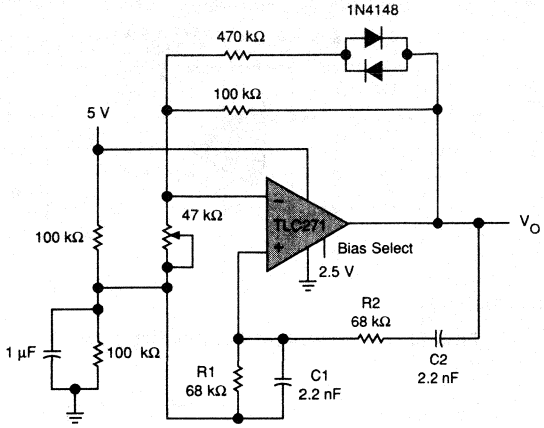


FIGURE 120. POSITIVE-PEAK DETECTOR

TYPICAL APPLICATION DATA (MEDIUM-BIAS MODE)



NOTES: $V_{OPP} \approx 2$ V

$$f_O = \frac{1}{2\pi\sqrt{R1R2C1C2}}$$

FIGURE 121. WIEN OSCILLATOR

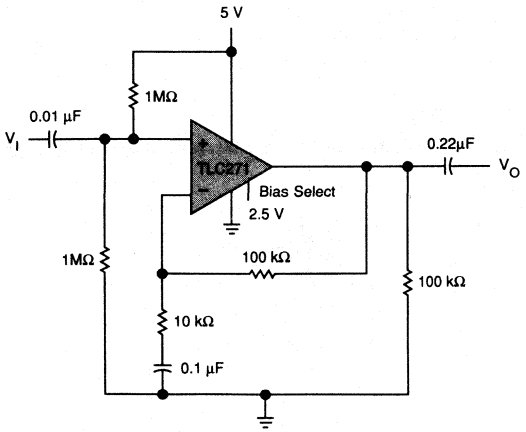
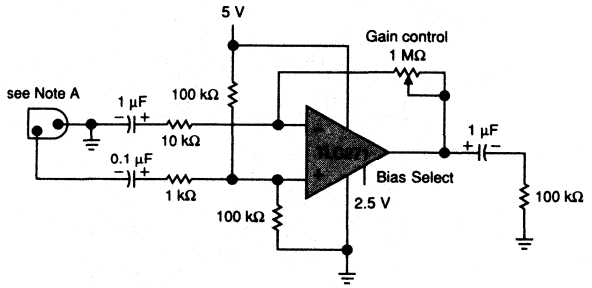


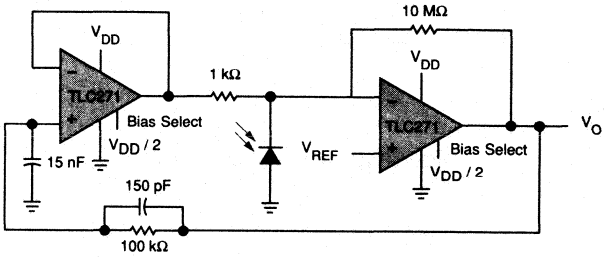
FIGURE 122. SINGLE-SUPPLY A.C. AMPLIFIER

TYPICAL APPLICATION DATA (MEDIUM-BIAS MODE)



NOTE A: Low to medium impedance dynamic mike

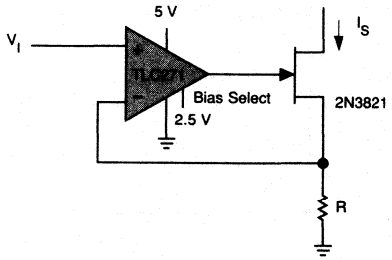
FIGURE 123. MICROPHONE PREAMPLIFIER



NOTES: V_{DD} = 4 V to 15 V

V_{REF} = 0 V to V_{DD} – 2 V

FIGURE 124. PHOTO DIODE AMPLIFIER WITH AMBIENT LIGHT REJECTION



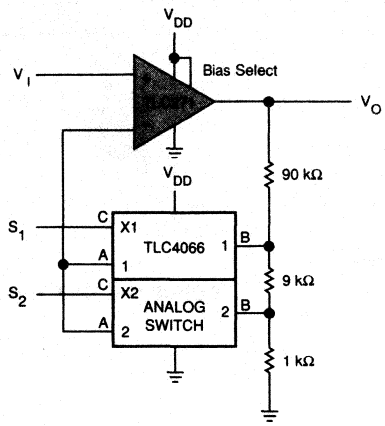
NOTES: V_I = 0 V TO 3 V

$$I_S = \frac{V_I}{R}$$

FIGURE 125. PRECISION LOW-CURRENT SINK

TYPICAL APPLICATION DATA (LOW-BIAS MODE)

Select:	S_1	S_2
A_V	10	100



NOTE: V_{DD} = 5 V to 12V

FIGURE 126. AMPLIFIER WITH DIGITAL GAIN SELECTION

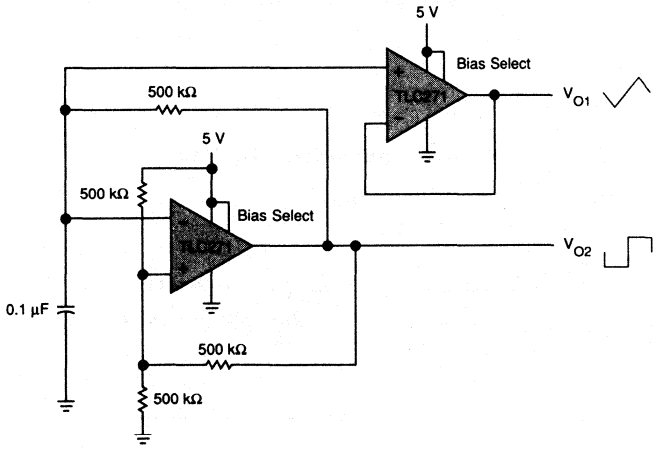
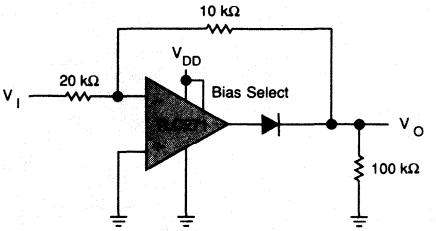


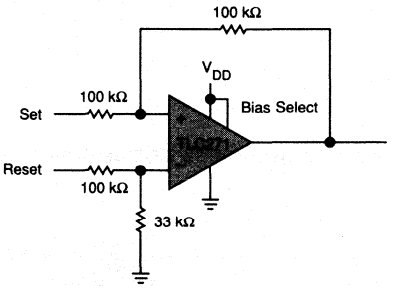
FIGURE 127. MULTIVIBRATOR

TYPICAL APPLICATION DATA (LOW-BIAS MODE)



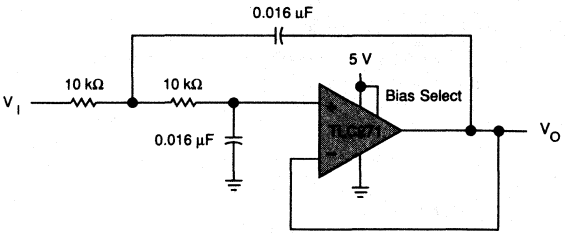
NOTE: V_{DD} = 5 V to 16V

FIGURE 128. FULL WAVE RECTIFIER



NOTE: V_{DD} = 5 V to 16V

FIGURE 129. SET / RESET FLIP-FLOP



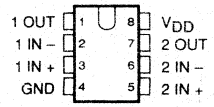
NOTE: Normalized to F_C = 1 kHz and R_L = 10 kΩ

FIGURE 130. TWO-POLE LOW-PASS BUTTERWORTH FILTER

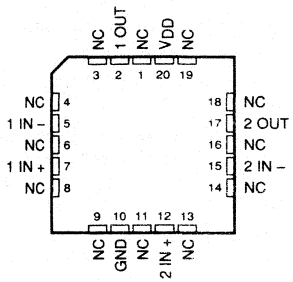
OCTOBER 1987

- **Trimmed Offset Voltage:**
  TLC277 ... 500 μV Max at 25°C, V_{DD} = 5 V
- **Input Offset Voltage Drift Typically**
  0.1 μV / Month, Including the First 30 Days
- **Wide Range of Supply Voltages over Specified Temperature Range:**
  – 55°C to125°C ... 4 V to 16 V
  – 40°C to 85°C ... 4 V to 16 V
  0°C to 70°C ... 3 V to 16 V
- **Single-Supply Operation**
- **Common-Mode Input Voltage Range Extends Below the Negative Rail (C- suffix, I- suffix types)**
- **Low Noise ... 25 nV/√Hz Typically at f = 1 kHz**
- **Output Voltage Range Includes Negative Rail**
- **High Input Impedance ... 10^{12} Ω Typical**
- **ESD Protection Circuitry**
- **Small-Outline Package Option Also Available in Tape-and-Reel**
- **Designed-in Latchup Immunity**

JG AND P DUAL-IN-LINE PACKAGE
D SMALL-OUTLINE PACKAGE
(TOP VIEW)



FK CHIP CARRIER PACKAGE
(TOP VIEW)



NC – No internal connection

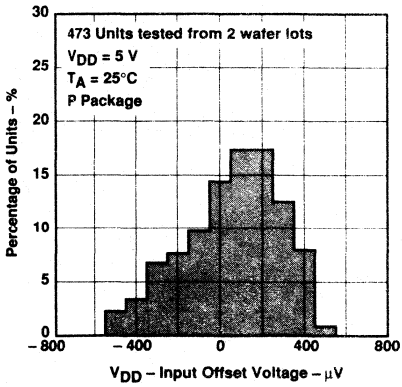
description

The TLC272 and TLC277 dual operational amplifiers combine a wide range of input offset voltage grades with low offset voltage drift, high input impedance, low noise, and speeds approaching that of general-purpose BiFET devices.

T_A	V_{IO}max at 25°C	PACKAGE			
		Small-Outline (D) See Note 1	Plastic DIP (P)	Ceramic DIP (JG)	Chip Carrier (FK)
0°C to 70°C	500 μV	TLC277CD	TLC277CP	TLC277CJG	—
	2 mV	TLC272BCD	TLC272BCP	TLC272BCJG	—
	5 mV	TLC272ACD	TLC272ACP	TLC272ACJG	—
	10 mV	TLC272CD	TLC272CP	TLC272CJG	—
– 40°C to 85°C	500 μV	TLC277ID	TLC277IP	TLC277IJG	—
	2 mV	TLC272BID	TLC272BIP	TLC272BIJG	—
	5 mV	TLC272AID	TLC272AIP	TLC272AIJG	—
	10 mV	TLC272ID	TLC272IP	TLC272IJG	—
– 55°C to 125°C	500 μV	—	—	TLC277MJG	TLC277MFK
	10 mV	—	—	TLC272MJG	TLC272MFK

NOTE 1: Available in tape-and-reel. Add "R" suffix to the device type when ordering (e.g., TLC277CDR).

DISTRIBUTION OF TLC277
INPUT OFFSET VOLTAGE



LinCMOS is a trademark of Texas Instruments Incorporated

description (continued)

These devices use Texas Instruments silicon-gate LinCMOS technology, which provides offset voltage stability far exceeding the stability available with conventional metal-gate processes.

The extremely high input impedance, low bias currents, and high slew rates make these cost-effective devices ideal for applications which have previously been reserved for BiFET and NFET products. Four offset voltage grades are available (C- suffix and I- suffix types), ranging from the low-cost TLC272 (10 mV) to the high-precision TLC277 (500 μV). These advantages, in combination with good common-mode rejection and supply voltage rejection, make these devices a good choice for new state-of-the-art designs as well as for upgrading existing designs.

In general, many features associated with bipolar technology are available on LinCMOS operational amplifiers, without the power penalties of bipolar technology. General applications such as transducer interfacing, analog calculations, amplifier blocks, active filters, and signal buffering are all easily designed with the TLC272 and TLC277. The devices also exhibit low voltage single supply operation making them ideally suited for remote and inaccessible battery-powered applications. The common-mode input voltage range includes the negative rail.

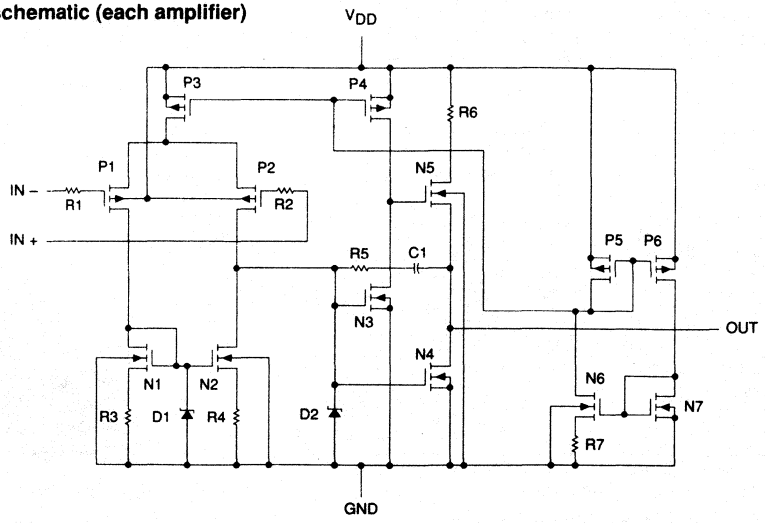
A wide range of packaging options is available, including small outline and chip carrier versions for high-density system applications.

The device inputs and outputs are designed to withstand −100-mA surge currents without sustaining latchup.

The TLC272 and TLC277 incorporate internal ESD protection circuits that will prevent functional failures at voltages up to 2000 V as tested under MIL-STD-883C, Method 3015.2; however, care should be exercised in handling these devices as exposure to ESD may result in the degradation of the device parametric performance.

The M- suffix devices are characterized for operation over the full military temperature range of −55°C to 125°C, the I- suffix devices from −40°C to 85°C, and the C- suffix devices from 0°C to 70°C.

equivalent schematic (each amplifier)



absolute maximum ratings over operating free-air temperature (unless otherwise noted)

Supply voltage, V_{DD} (see Note 2) . . . . . 18 V
Differential input voltage (see Note 3) . . . . . $\pm V_{DD}$
Input voltage range, V_I (any input) . . . . . −0.3 V to V_{DD}
Input current, I_I . . . . . ±5 mA
Output current, I_O (each output) . . . . . ±30 mA
Total current into V_{DD} terminal . . . . . 45 mA
Total current out of ground terminal . . . . . 45 mA
Duration of short-circuit current at (or below) 25°C (see Note 4) . . . . . Unlimited
Continuous total dissipation . . . . . See Dissipation Rating Table
Operating free-air temperature, T_A: C-suffix types . . . . . 0°C to 70°C
I-suffix types . . . . . −40°C to 85°C
M-suffix types . . . . . −55°C to 125°C
Storage temperature range . . . . . −65°C to 150°C
Case temperature for 60 seconds: FK package . . . . . 260°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds: JG package . . . . . 300°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: D and P package . . . . . 260°C

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING	$T_A = 85°C$ POWER RATING	$T_A = 125°C$ POWER RATING
D	725 mW	5.8 mW/°C	464 mW	377 mW	
FK	1375 mW	11 mW/°C	880 mW	715 mW	275 mW
JG (C-, I- suffix)	825 mW	6.6 mW/°C	528 mW	429 mW	
JG (M- suffix)	1050 mW	8.4 mW/°C	672 mW	546 mW	210 mW
P	1000 mW	8.0 mW/°C	640 mW	520 mW	

recommended operating conditions

		M- SUFFIX TYPES			I- SUFFIX TYPES			C- SUFFIX TYPES			
		MIN	NOM	MAX	MIN	NOM	MAX	MIN	NOM	MAX	UNIT
Supply voltage, V_{DD}		4		16	4		16	3		16	V
Common-mode input voltage, V_{IC}	$V_{DD} = 5$ V	0		3.5	−0.2		3.5	−0.2		3.5	V
	$V_{DD} = 10$ V	0		8.5	−0.2		8.5	−0.2		8.5	V
Input voltage, V_I	$V_{DD} = 5$ V	0		3.5	−0.2		3.5	−0.2		3.5	V
	$V_{DD} = 10$ V	0		8.5	−0.2		8.5	−0.2		8.5	V
Operating free-air temperature, T_A		−55		125	−40		85	0		70	°C

NOTES: 2. All voltage values, except differential voltages, are with respect to network ground.
3. Differential voltages are at the noninverting input with respect to the inverting input.
4. The output may be shorted to either supply. Temperature and/or supply voltages must be limited to ensure that the maximum dissipation rating is not exceeded (see application section).

electrical characteristics at specified free-air temperature, V_{DD} = 5 V (unless otherwise noted)

PARAMETER			TEST CONDITIONS		C- SUFFIX TYPES MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage	TLC272C	V_O = 1.4 V, V_{IC} = 0 V, R_S = 50 Ω, R_L = 10 kΩ	25°C		1.1	10	mV
				Full range			12	
		TLC272AC	V_O = 1.4 V, V_{IC} = 0 V, R_S = 50 Ω, R_L = 10 kΩ	25°C		0.9	5	
				Full range			6.5	
		TLC272BC	V_O = 1.4 V, V_{IC} = 0 V, R_S = 50 Ω, R_L = 10 kΩ	25°C		230	2000	μV
				Full range			3000	
		TLC277C	V_O = 1.4 V, V_{IC} = 0 V, R_S = 50 Ω, R_L = 10 kΩ	25°C		200	500	
				Full range			1500	
α_{VIO}	Average temperature coefficient of input offset voltage			25°C to 70°C		1.8		μV/°C
I_{IO}	Input offset current (see Note 5)		V_{IC} = 2.5 V, V_O = 2.5 V	25°C		0.1		pA
				70°C		7	300	
I_{IB}	Input bias current (see Note 5)		V_{IC} = 2.5 V, V_O = 2.5 V	25°C		0.6		pA
				70°C		40	600	
V_{ICR}	Common-mode input voltage range (see Note 6)			25°C	−0.2 to 4	−0.3 to 4.2		V
				Full range	−0.2 to 3.5			V
V_{OH}	High-level output voltage		V_{ID} = 100 mV, R_L = 10 kΩ	25°C	3.2	3.8		V
				70°C	3	3.8		
				0°C	3	3.8		
V_{OL}	Low-level output voltage		V_{ID} = −100 mV, I_{OL} = 0	25°C		0	50	mV
				70°C		0	50	
				0°C		0	50	
A_{VD}	Large-signal differential voltage amplification		V_O = 0.25 V to 2 V, R_L = 10 kΩ	25°C	5	23		V/mV
				70°C	4	20		
				0°C	4	27		
CMRR	Common-mode rejection ratio		V_{IC} = V_{ICR} min	25°C	65	80		dB
				70°C	60	85		
				0°C	60	84		
k_{SVR}	Supply-voltage rejection ratio (ΔV_{DD} / ΔV_{IO})		V_{DD} = 5 V to 10 V, V_O = 1.4 V	25°C	65	95		dB
				70°C	60	96		
				0°C	60	94		
I_{DD}	Supply current (two amplifiers)		No load, V_O = 2.5 V, V_{IC} = 2.5 V	25°C		1.4	3.2	mA
				70°C		1.2	2.6	
				0°C		1.6	3.6	

NOTES: 5. The typical values of input bias current and input offset current below 5 pA were determined mathematically.
6. This range also applies to each input individually.

electrical characteristics at specified free-air temperature, V_{DD} = 10 V (unless otherwise noted)

PARAMETER			TEST CONDITIONS		C- SUFFIX TYPES MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage	TLC272C	V_O = 1.4 V, V_{IC} = 0 V, R_S = 50 Ω, R_L = 10 kΩ	25°C		1.1	10	mV
				Full range			12	
		TLC272AC	V_O = 1.4 V, V_{IC} = 0 V, R_S = 50 Ω, R_L = 10 kΩ	25°C		0.9	5	
				Full range			6.5	
		TLC272BC	V_O = 1.4 V, V_{IC} = 0 V, R_S = 50 Ω, R_L = 10 kΩ	25°C		290	2000	μV
				Full range			3000	
		TLC277C	V_O = 1.4 V, V_{IC} = 0 V, R_S = 50 Ω, R_L = 10 kΩ	25°C		250	800	
				Full range			1900	
α_{VIO}	Average temperature coefficient of input offset voltage			25°C to 70°C		2		μV/°C
I_{IO}	Input offset current (see Note 5)		V_{IC} = 5 V, V_O = 5 V	25°C		0.1		pA
				70°C		8	300	
I_{IB}	Input bias current (see Note 5)		V_{IC} = 5 V, V_O = 5 V	25°C		0.7		pA
				70°C		50	600	
V_{ICR}	Common-mode input voltage range (see Note 6)			25°C	−0.2 to 9	−0.3 to 9.2		V
				Full range	−0.2 to 8.5			V
V_{OH}	High-level output voltage		V_{ID} = 100 mV, R_L = 10 kΩ	25°C	8	8.5		V
				70°C	7.8	8.4		
				0°C	7.8	8.5		
V_{OL}	Low-level output voltage		V_{ID} = −100 mV, I_{OL} = 0	25°C		0	50	mV
				70°C		0	50	
				0°C		0	50	
A_{VD}	Large-signal differential voltage amplification		V_O = 1 V to 6 V, R_L = 10 kΩ	25°C	10	36		V/mV
				70°C	7.5	32		
				0°C	7.5	42		
CMRR	Common-mode rejection ratio		V_{IC} = V_{ICR} min	25°C	65	85		dB
				70°C	60	88		
				0°C	60	88		
k_{SVR}	Supply-voltage rejection ratio (ΔV_{DD} / ΔV_{IO})		V_{DD} = 5 V to 10 V, V_O = 1.4 V	25°C	65	95		dB
				70°C	60	96		
				0°C	60	94		
I_{DD}	Supply current (two amplifiers)		No load, V_O = 5 V, V_{IC} = 5 V	25°C		1.9	4	mA
				70°C		1.5	3.4	
				0°C		2.3	4.4	

NOTES: 5. The typical values of input bias current and input offset current below 5 pA were determined mathematically.
6. This range also applies to each input individually.

electrical characteristics at specified free-air temperature, V_{DD} = 5 V (unless otherwise noted)

PARAMETER			TEST CONDITIONS		I- SUFFIX TYPES MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage	TLC272I	V_O = 1.4 V, V_{IC} = 0 V, R_S = 50 Ω, R_L = 10 kΩ	25°C		1.1	10	mV
				Full range			13	
		TLC272AI	V_O = 1.4 V, V_{IC} = 0 V, R_S = 50 Ω, R_L = 10 kΩ	25°C		0.9	5	
				Full range			7	
		TLC272BI	V_O = 1.4 V, V_{IC} = 0 V, R_S = 50 Ω, R_L = 10 kΩ	25°C		230	2000	µV
				Full range			3500	
		TLC277I	V_O = 1.4 V, V_{IC} = 0 V, R_S = 50 Ω, R_L = 10 kΩ	25°C		200	500	
				Full range			2000	
α_{VIO}	Average temperature coefficient of input offset voltage			25°C to 85°C		1.8		µV/°C
I_{IO}	Input offset current (see Note 5)		V_{IC} = 2.5 V, V_O = 2.5 V	25°C		0.1		pA
				85°C		24	1000	
I_{IB}	Input bias current (see Note 5)		V_{IC} = 2.5 V, V_O = 2.5 V	25°C		0.6		pA
				85°C		200	2000	
V_{ICR}	Common-mode input voltage range (see Note 6)			25°C	−0.2 to 4	−0.3 to 4.2		V
				Full range	−0.2 to 3.5			V
V_{OH}	High-level output voltage		V_{ID} = 100 mV, R_L = 10 kΩ	25°C	3.2	3.8		V
				85°C	3	3.8		
				−40°C	3	3.8		
V_{OL}	Low-level output voltage		V_{ID} = −100 mV, I_{OL} = 0	25°C		0	50	mV
				85°C		0	50	
				−40°C		0	50	
A_{VD}	Large-signal differential voltage amplification		V_O = 0.25 V to 2 V, R_L = 10 kΩ	25°C	5	23		V/mV
				85°C	3.5	19		
				−40°C	3.5	32		
CMRR	Common-mode rejection ratio		V_{IC} = V_{ICR} min	25°C	65	80		dB
				85°C	60	86		
				−40°C	60	81		
k_{SVR}	Supply-voltage rejection ratio (ΔV_{DD} / ΔV_{IO})		V_{DD} = 5 V to 10 V, V_O = 1.4 V	25°C	65	95		dB
				85°C	60	96		
				−40°C	60	92		
I_{DD}	Supply current (two amplifiers)		No load, V_O = 2.5 V, V_{IC} = 2.5 V	25°C		1.4	3.2	mA
				85°C		1.1	2.4	
				−40°C		1.9	4.4	

NOTES: 5. The typical values of input bias current and input offset current below 5 pA were determined mathematically.
6. This range also applies to each input individually.

electrical characteristics at specified free-air temperature, V_{DD} = 10 V (unless otherwise noted)

PARAMETER			TEST CONDITIONS		I-SUFFIX TYPES MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage	TLC272I	V_O = 1.4 V, V_{IC} = 0 V, R_S = 50 Ω, R_L = 10 kΩ	25°C		1.1	10	mV
				Full range			13	
		TLC272AI	V_O = 1.4 V, V_{IC} = 0 V, R_S = 50 Ω, R_L = 10 kΩ	25°C		0.9	5	mV
				Full range			7	
		TLC272BI	V_O = 1.4 V, V_{IC} = 0 V, R_S = 50 Ω, R_L = 10 kΩ	25°C		290	2000	μV
				Full range			3500	
		TLC277I	V_O = 1.4 V, V_{IC} = 0 V, R_S = 50 Ω, R_L = 10 kΩ	25°C		250	800	μV
				Full range			2900	
α_{VIO}	Average temperature coefficient of input offset voltage			25°C to 85°C		2		μV/°C
I_{IO}	Input offset current (see Note 5)		V_{IC} = 5 V, V_O = 5 V	25°C		0.1		pA
				85°C		26	1000	
I_{IB}	Input bias current (see Note 5)		V_{IC} = 5 V, V_O = 5 V	25°C		0.7		pA
				85°C		220	2000	
V_{ICR}	Common-mode input voltage range (see Note 6)			25°C	−0.2 to 9	−0.3 to 9.2		V
				Full range	−0.2 to 8.5			V
V_{OH}	High-level output voltage		V_{ID} = 100 mV, R_L = 10 kΩ	25°C	8	8.5		V
				85°C	7.8	8.5		
				−40°C	7.8	8.5		
V_{OL}	Low-level output voltage		V_{ID} = −100 mV, I_{OL} = 0	25°C		0	50	mV
				85°C		0	50	
				−40°C		0	50	
A_{VD}	Large-signal differential voltage amplification		V_O = 1 V to 6 V, R_L = 10 kΩ	25°C	10	36		V/mV
				85°C	7	31		
				−40°C	7	46		
CMRR	Common-mode rejection ratio		V_{IC} = V_{ICR} min	25°C	65	85		dB
				85°C	60	88		
				−40°C	60	87		
k_{SVR}	Supply-voltage rejection ratio (ΔV_{DD} / ΔV_{IO})		V_{DD} = 5 V to 10 V, V_O = 1.4 V	25°C	65	95		dB
				85°C	60	96		
				−40°C	60	92		
I_{DD}	Supply current (two amplifiers)		No load, V_O = 5 V, V_{IC} = 5 V	25°C		1.9	4	mA
				85°C		1.5	3.2	
				−40°C		2.8	5	

NOTES: 5. The typical values of input bias current and input offset current below 5 pA were determined mathematically.
6. This range also applies to each input individually.

electrical characteristics at specified free-air temperature, V_{DD} = 5 V (unless otherwise noted)

PARAMETER			TEST CONDITIONS		M- SUFFIX TYPES MIN	M- SUFFIX TYPES TYP	M- SUFFIX TYPES MAX	UNIT
V_{IO}	Input offset voltage	TLC272M	V_O = 1.4 V, V_{IC} = 0 V, R_S = 50 Ω, R_L = 10 kΩ	25°C		1.1	10	mV
				Full range			12	
		TLC277M	V_O = 1.4 V, V_{IC} = 0 V, R_S = 50 Ω, R_L = 10 kΩ	25°C		200	500	μV
				Full range			3750	
α_{VIO}	Average temperature coefficient of input offset voltage			25°C to 125°C		2.1		μV/°C
I_{IO}	Input offset current (see Note 5)		V_{IC} = 2.5 V, V_O = 2.5 V	25°C		0.1		pA
				125°C		1.4	15	nA
I_{IB}	Input bias current (see Note 5)		V_{IC} = 2.5 V, V_O = 2.5 V	25°C		0.6		pA
				125°C		9	35	nA
V_{ICR}	Common-mode input voltage range (see Note 6)			25°C	0 to 4	−0.3 to 4.2		V
				Full range	0 to 3.5			V
V_{OH}	High-level output voltage		V_{ID} = 100 mV, R_L = 10 kΩ	25°C	3.2	3.8		V
				125°C	3	3.8		
				−55°C	3	3.8		
V_{OL}	Low-level output voltage		V_{ID} = −100 mV, I_{OL} = 0	25°C		0	50	mV
				125°C		0	50	
				−55°C		0	50	
A_{VD}	Large-signal differential voltage amplification		V_O = 0.25 V to 2 V, R_L = 10 kΩ	25°C	5	23		V/mV
				125°C	3.5	16		
				−55°C	3.5	35		
CMRR	Common-mode rejection ratio		V_{IC} = V_{ICR} min	25°C	65	80		dB
				125°C	60	84		
				−55°C	60	81		
k_{SVR}	Supply-voltage rejection ratio (ΔV_{DD} / ΔV_{IO})		V_{DD} = 5 V to 10 V, V_O = 1.4 V	25°C	65	95		dB
				125°C	60	97		
				−55°C	60	90		
I_{DD}	Supply current (two amplifiers)		No load, V_O = 2.5 V, V_{IC} = 2.5 V	25°C		1.4	3.2	mA
				125°C		1	2.2	
				−55°C		2	5	

NOTES: 5. The typical values of input bias current and input offset current below 5 pA were determined mathematically.
6. This range also applies to each input individually.

electrical characteristics at specified free-air temperature, V_{DD} = 10 V (unless otherwise noted)

PARAMETER			TEST CONDITIONS		M- SUFFIX TYPES MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage	TLC272M	V_O = 1.4 V, V_{IC} = 0 V, R_S = 50 Ω, R_L = 10 kΩ	25°C		1.1	10	mV
				Full range			12	
		TLC277M	V_O = 1.4 V, V_{IC} = 0 V, R_S = 50 Ω, R_L = 10 kΩ	25°C		250	800	μV
				Full range			4300	
α_{VIO}	Average temperature coefficient of input offset voltage			25°C to 125°C		2.2		μV/°C
I_{IO}	Input offset current (see Note 5)		V_{IC} = 5 V, V_O = 5 V	25°C		0.1		pA
				125°C		1.8	15	nA
I_{IB}	Input bias current (see Note 5)		V_{IC} = 5 V, V_O = 5 V	25°C		0.7		pA
				125°C		10	35	nA
V_{ICR}	Common-mode input voltage range (see Note 6)			25°C	0 to 9	−0.3 to 9.2		V
				Full range	0 to 8.5			V
V_{OH}	High-level output voltage		V_{ID} = 100 mV, R_L = 10 kΩ	25°C	8	8.5		V
				125°C	7.8	8.4		
				−55°C	7.8	8.5		
V_{OL}	Low-level output voltage		V_{ID} = −100 mV, I_{OL} = 0	25°C		0	50	mV
				125°C		0	50	
				−55°C		0	50	
A_{VD}	Large-signal differential voltage amplification		V_O = 1 V to 6 V, R_L = 10 kΩ	25°C	10	36		V/mV
				125°C	7	27		
				−55°C	7	50		
CMRR	Common-mode rejection ratio		V_{IC} = V_{ICR} min	25°C	65	85		dB
				125°C	60	86		
				−55°C	60	87		
k_{SVR}	Supply-voltage rejection ratio (ΔV_{DD} / ΔV_{IO})		V_{DD} = 5 V to 10 V, V_O = 1.4 V	25°C	65	95		dB
				125°C	60	97		
				−55°C	60	90		
I_{DD}	Supply current (two amplifiers)		No load, V_O = 5 V, V_{IC} = 5 V	25°C		1.9	4	mA
				125°C		1.3	2.8	
				−55°C		3	6	

NOTES: 5. The typical values of input bias current and input offset current below 5 pA were determined mathematically.
6. This range also applies to each input individually.

operating characteristics, V_{DD} = 5 V

PARAMETER		TEST CONDITIONS			C- SUFFIX TYPES MIN	C- SUFFIX TYPES TYP	C- SUFFIX TYPES MAX	UNIT
SR	Slew rate at unity gain	R_L = 10 kΩ, C_L = 20 pF, See Figure 1	V_{IPP} = 1 V	25°C		3.6		V/μs
				70°C		3		
				0°C		3.9		
			V_{IPP} = 2.5 V	25°C		2.9		
				70°C		2.5		
				0°C		3.1		
V_n	Equivalent input noise voltage	f = 1 kHz, R_S = 100 Ω, See Figure 2		25°C		25		nV/√Hz
B_{OM}	Maximum output swing bandwidth	$V_O = V_{OH}$, C_L = 20 pF, R_L = 10 kΩ, See Figure 1		25°C		320		kHz
				70°C		260		
				0°C		340		
B_1	Unity-gain bandwidth	V_i = 10 mV, C_L = 20 pF, See Figure 3		25°C		1.7		MHz
				70°C		1.3		
				0°C		2		
ϕ_m	Phase margin	f = B_1, V_i = 10 mV, C_L = 20 pF, See Figure 3		25°C		46°		
				70°C		43°		
				0°C		47°		

operating characteristics, V_{DD} = 10 V

PARAMETER		TEST CONDITIONS			C- SUFFIX TYPES MIN	C- SUFFIX TYPES TYP	C- SUFFIX TYPES MAX	UNIT
SR	Slew rate at unity gain	R_L = 10 kΩ, C_L = 20 pF, See Figure 1	V_{IPP} = 1 V	25°C		5.3		V/μs
				70°C		4.3		
				0°C		5.9		
			V_{IPP} = 5.5 V	25°C		4.6		
				70°C		3.8		
				0°C		5.1		
V_n	Equivalent input noise voltage	f = 1 kHz, R_S = 100 Ω, See Figure 2		25°C		25		nV/√Hz
B_{OM}	Maximum output swing bandwidth	$V_O = V_{OH}$, C_L = 20 pF, R_L = 10 kΩ, See Figure 1		25°C		200		kHz
				70°C		140		
				0°C		220		
B_1	Unity-gain bandwidth	V_i = 10 mV, C_L = 20 pF, See Figure 3		25°C		2.2		MHz
				70°C		1.8		
				0°C		2.5		
ϕ_m	Phase margin	f = B_1, V_i = 10 mV, C_L = 20 pF, See Figure 3		25°C		49°		
				70°C		46°		
				0°C		50°		

operating characteristics, V_{DD} = 5 V

PARAMETER		TEST CONDITIONS			I-SUFFIX TYPES MIN	I-SUFFIX TYPES TYP	I-SUFFIX TYPES MAX	UNIT
SR	Slew rate at unity gain	R_L = 10 kΩ, C_L = 20 pF, See Figure 1	V_{IPP} = 1 V	25°C		3.6		V/μs
				85°C		2.8		
				−40°C		4.5		
			V_{IPP} = 2.5 V	25°C		2.9		
				85°C		2.3		
				−40°C		3.5		
V_n	Equivalent input noise voltage	f = 1 kHz, R_S = 100 Ω, See Figure 2		25°C		25		nV/√Hz
B_{OM}	Maximum output swing bandwidth	$V_O = V_{OH}$, C_L = 20 pF, R_L = 10 kΩ, See Figure 1		25°C		320		kHz
				85°C		250		
				−40°C		380		
B_1	Unity-gain bandwidth	V_i = 10 mV, C_L = 20 pF, See Figure 3		25°C		1.7		MHz
				85°C		1.2		
				−40°C		2.6		
ϕ_m	Phase margin	f = B_1, V_i = 10 mV, C_L = 20 pF, See Figure 3		25°C		46°		
				85°C		43°		
				−40°C		49°		

operating characteristics, V_{DD} = 10 V

PARAMETER		TEST CONDITIONS			I-SUFFIX TYPES MIN	I-SUFFIX TYPES TYP	I-SUFFIX TYPES MAX	UNIT
SR	Slew rate at unity gain	R_L = 10 kΩ, C_L = 20 pF, See Figure 1	V_{IPP} = 1 V	25°C		5.3		V/μs
				85°C		4		
				−40°C		6.7		
			V_{IPP} = 5.5 V	25°C		4.6		
				85°C		3.5		
				−40°C		5.8		
V_n	Equivalent input noise voltage	f = 1 kHz, R_S = 100 Ω, See Figure 2		25°C		25		nV/√Hz
B_{OM}	Maximum output swing bandwidth	$V_O = V_{OH}$, C_L = 20 pF, R_L = 10 kΩ, See Figure 1		25°C		200		kHz
				85°C		130		
				−40°C		260		
B_1	Unity-gain bandwidth	V_i = 10 mV, C_L = 20 pF, See Figure 3		25°C		2.2		MHz
				85°C		1.7		
				−40°C		3.1		
ϕ_m	Phase margin	f = B_1, V_i = 10 mV, C_L = 20 pF, See Figure 3		25°C		49°		
				85°C		46°		
				−40°C		52°		

operating characteristics, V_{DD} = 5 V

PARAMETER		TEST CONDITIONS			M- SUFFIX TYPES MIN	M- SUFFIX TYPES TYP	M- SUFFIX TYPES MAX	UNIT
SR	Slew rate at unity gain	R_L = 10 kΩ, C_L = 20 pF, See Figure 1	V_{IPP} = 1 V	25°C		3.6		V/μs
				125°C		2.3		
				– 55°C		4.7		
			V_{IPP} = 2.5 V	25°C		2.9		
				125°C		2		
				– 55°C		3.7		
V_n	Equivalent input noise voltage	f = 1 kHz, R_S = 100 Ω, See Figure 2		25°C		25		nV/√Hz
B_{OM}	Maximum output swing bandwidth	V_O = V_{OH}, C_L = 20 pF, R_L = 10 kΩ, See Figure 1		25°C		320		kHz
				125°C		230		
				– 55°C		400		
B_1	Unity-gain bandwidth	V_i = 10 mV, C_L = 20 pF, See Figure 3		25°C		1.7		MHz
				125°C		1.1		
				– 55°C		2.9		
ϕ_m	Phase margin	f = B_1, V_i = 10 mV, C_L = 20 pF, See Figure 3		25°C		46°		
				125°C		41°		
				– 55°C		49°		

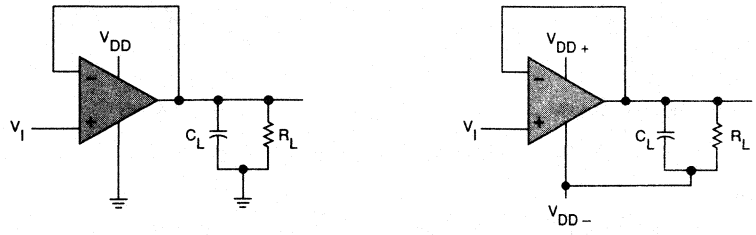
operating characteristics, V_{DD} = 10 V

PARAMETER		TEST CONDITIONS			M- SUFFIX TYPES MIN	M- SUFFIX TYPES TYP	M- SUFFIX TYPES MAX	UNIT
SR	Slew rate at unity gain	R_L = 10 kΩ, C_L = 20 pF, See Figure 1	V_{IPP} = 1 V	25°C		5.3		V/μs
				125°C		3.1		
				– 55°C		7.1		
			V_{IPP} = 5.5 V	25°C		4.6		
				125°C		2.7		
				– 55°C		6.1		
V_n	Equivalent input noise voltage	f = 1 kHz, R_S = 100 Ω, See Figure 2		25°C		25		nV/√Hz
B_{OM}	Maximum output swing bandwidth	V_O = V_{OH}, C_L = 20 pF, R_L = 10 kΩ, See Figure 1		25°C		200		kHz
				125°C		110		
				– 55°C		280		
B_1	Unity-gain bandwidth	V_i = 10 mV, C_L = 20 pF, See Figure 3		25°C		2.2		MHz
				125°C		1.6		
				– 55°C		3.4		
ϕ_m	Phase margin	f = B_1, V_i = 10 mV, C_L = 20 pF, See Figure 3		25°C		49°		
				125°C		44°		
				– 55°C		52°		

PARAMETER MEASUREMENT INFORMATION

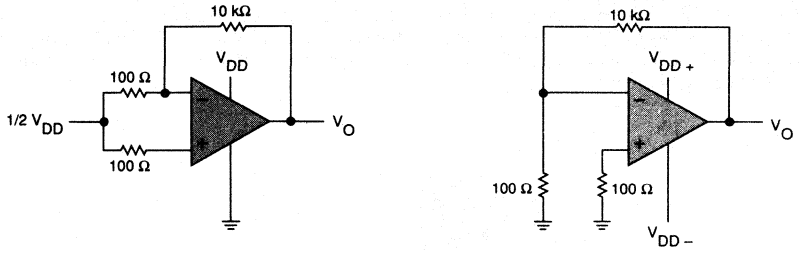
single-supply versus split-supply test circuits

Because the TLC272 and TLC277 are optimized for single-supply operation, circuit configurations used for the various tests often present some inconvenience since the input signal, in many cases, must be offset from ground. This inconvenience can be avoided by testing the device with split supplies and the output load tied to the negative rail. A comparison of single-supply versus split-supply test circuits is shown below. The use of either circuit will give the same result.



(a) Single-Supply (b) Split-Supply

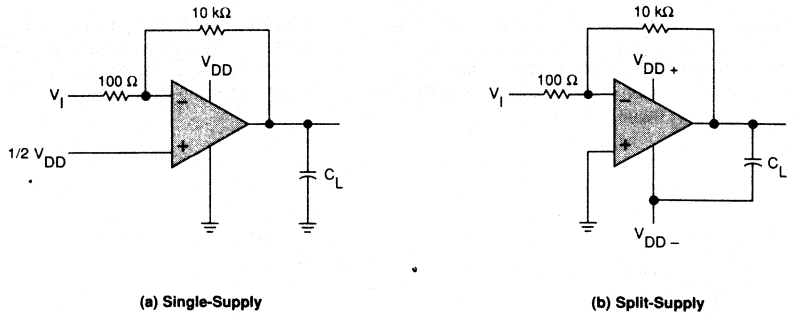
FIGURE 1. UNITY-GAIN AMPLIFIER



(a) Single-Supply (b) Split-Supply

FIGURE 2. NOISE TEST CIRCUIT

PARAMETER MEASUREMENT INFORMATION



(a) Single-Supply (b) Split-Supply

FIGURE 3. GAIN-OF-100 INVERTING AMPLIFIER

input bias current

Because of the high input impedance of the TLC272 and TLC277 op amps, attempts to measure the input bias current can result in erroneous readings. The bias current at normal room ambient temperature is typically less than 1 pA, a value that is easily exceeded by leakages on the test socket. Two suggestions are offered to avoid erroneous measurements:

1 Isolate the device from other potential leakage sources. Use a grounded shield around and between the device inputs (see Figure 4). Leakages that would otherwise flow to the inputs will be shunted away.

2 Compensate for the leakage of the test socket by actually performing an input bias current test (using a picoammeter) with no device in the test socket. The actual input bias current can then be calculated by subtracting the "open-socket" leakage readings from the readings obtained with a device in the test socket.

One word of caution . . . many automatic testers as well as some bench-top op amp testers use the servo-loop technique with a resistor in series with the device input to measure the input bias current (the voltage drop across the series resistor is measured and the bias current is calculated). This method requires that a device be inserted into the test socket to obtain a correct reading; therefore, an "open-socket" reading is not feasible using this method.

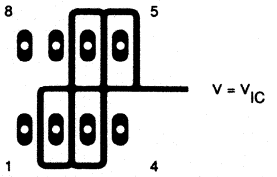


FIGURE 4. ISOLATION METAL AROUND DEVICE INPUTS
(P AND JG DUAL-IN-LINE PACKAGE)

PARAMETER MEASUREMENT INFORMATION

low-level output voltage

To obtain low-supply-voltage operation, some compromise was necessary in the input stage. This compromise results in the device low-level output being dependent on both the common-mode input voltage level as well as the differential input voltage level. When attempting to correlate low-level output readings with those quoted in the electrical specifications, these two conditions should be observed. If conditions other than these are to be used, please refer to Figures 14 thru 19 in the Typical Characteristics section of this data sheet.

input offset voltage temperature coefficient

Erroneous readings often result from attempts to measure temperature coefficient of input offset voltage. This parameter is actually a calculation using input offset voltage measurements obtained at two different temperatures. When one (or both) of the temperatures is below freezing, moisture can collect on both the device and the test socket. This moisture will result in leakage and contact resistance which can cause erroneous input offset voltage readings. The isolation techniques previously mentioned have no affect on the leakage since the moisture also covers the isolation metal itself, thereby rendering it useless. It is suggested that these measurements be performed at temperatures above freezing to minimize error.

full power response

Full power response, the frequency above which the op amp slew rate limits the output voltage swing, is often specified two ways . . . full-linear response and full-peak response. The full-linear response is generally measured by monitoring the distortion level of the output while increasing the frequency of a sinusoidal input signal until the maximum frequency is found above which the output contains significant distortion. The full-peak response is defined as the maximum output frequency, without regard to distortion, above which full peak-to-peak output swing cannot be maintained.

Because there is no industry-wide accepted value for "significant" distortion, the full-peak response is specified in this data sheet and is measured using the circuit of Figure 1. The initial setup involves the use of a sinusoidal input to determine the maximum peak-to-peak output of the device (the amplitude of the sinusoidal wave is increased until clipping occurs). The sinusoidal wave is then replaced with a square wave of the same amplitude. The frequency is then increased until the maximum peak-to-peak output can no longer be maintained (Figure 5). A square wave is used to allow a more accurate determination of the point at which the maximum peak-to-peak output is reached.

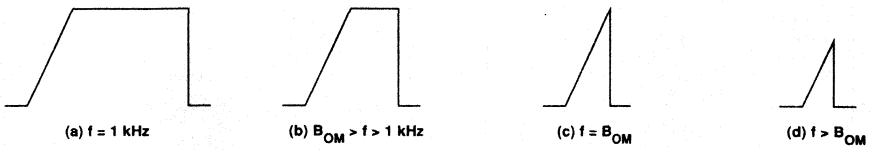


FIGURE 5. FULL-POWER-RESPONSE OUTPUT SIGNAL

test time

Inadequate test time is a frequent problem, especially when testing CMOS devices in a high-volume, short-test-time environment. Internal capacitances are inherently higher in CMOS than in bipolar and BiFET devices, and require longer test times than their bipolar and BiFET counterparts. The problem becomes more pronounced with reduced supply levels and lower temperatures.

TYPICAL CHARACTERISTICS

DISTRIBUTION OF TLC272
INPUT OFFSET VOLTAGE

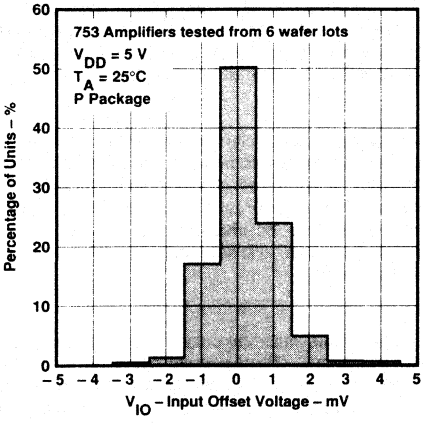


FIGURE 6

DISTRIBUTION OF TLC272
INPUT OFFSET VOLTAGE

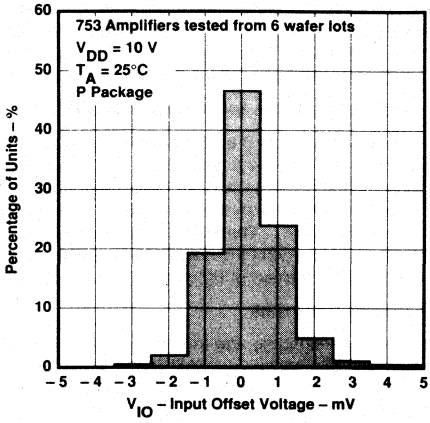


FIGURE 7

DISTRIBUTION OF TLC272 AND TLC277
INPUT OFFSET VOLTAGE
TEMPERATURE COEFFICIENT

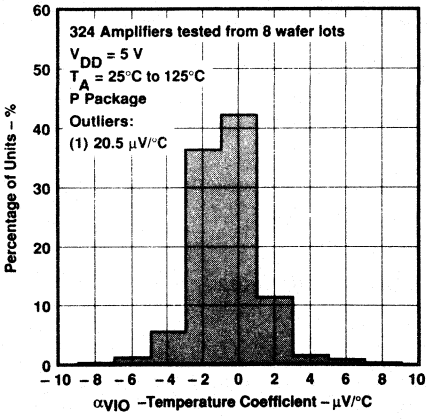


FIGURE 8

DISTRIBUTION OF TLC272 AND TLC277
INPUT OFFSET VOLTAGE
TEMPERATURE COEFFICIENT

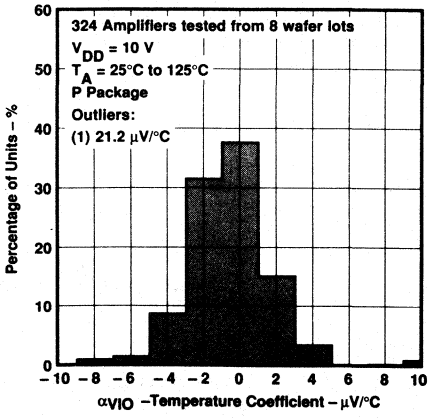


FIGURE 9

TYPICAL CHARACTERISTICS

HIGH-LEVEL OUTPUT VOLTAGE
vs
HIGH-LEVEL OUTPUT CURRENT

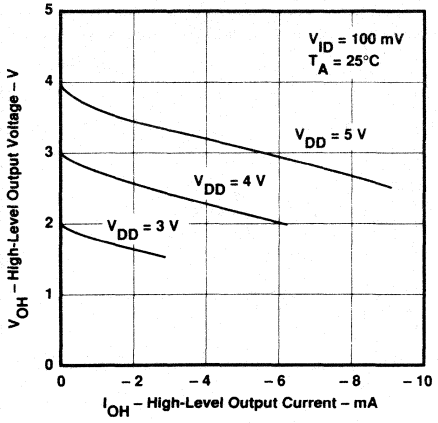


FIGURE 10

HIGH-LEVEL OUTPUT VOLTAGE
vs
HIGH-LEVEL OUTPUT CURRENT

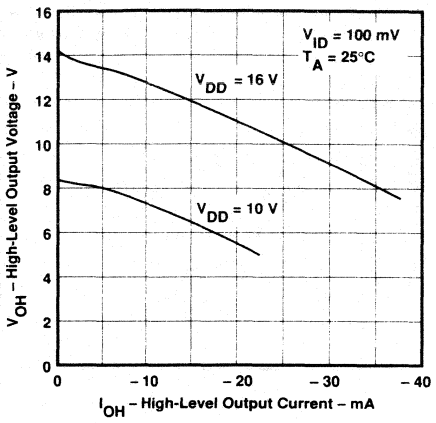


FIGURE 11

HIGH-LEVEL OUTPUT VOLTAGE
vs
SUPPLY VOLTAGE

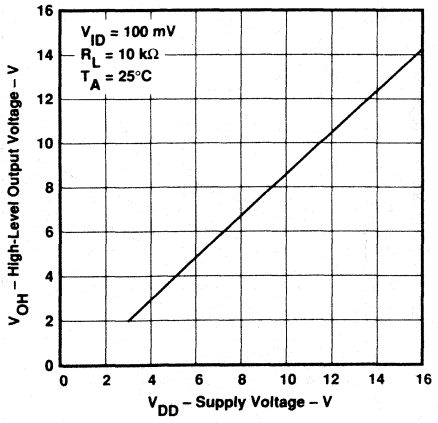


FIGURE 12

HIGH-LEVEL OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE

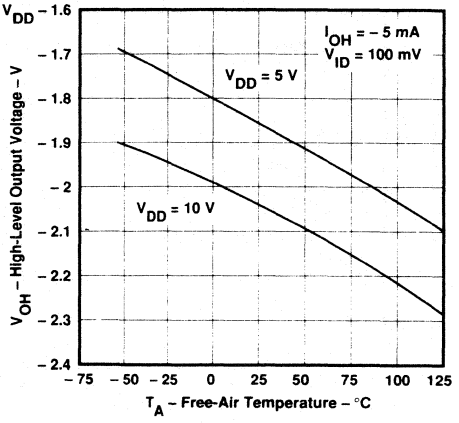


FIGURE 13

TYPICAL CHARACTERISTICS

LOW-LEVEL OUTPUT VOLTAGE
vs
COMMON-MODE INPUT VOLTAGE

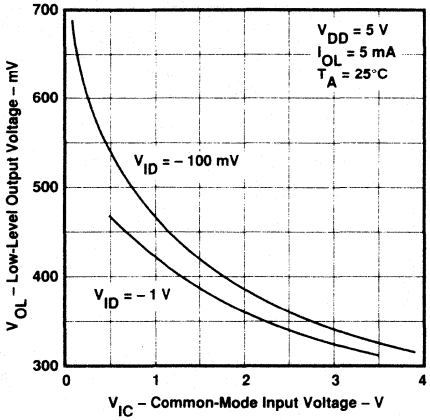


FIGURE 14

LOW-LEVEL OUTPUT VOLTAGE
vs
COMMON-MODE INPUT VOLTAGE

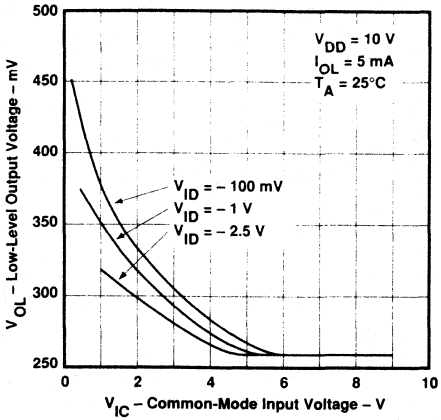


FIGURE 15

LOW-LEVEL OUTPUT VOLTAGE
vs
DIFFERENTIAL INPUT VOLTAGE

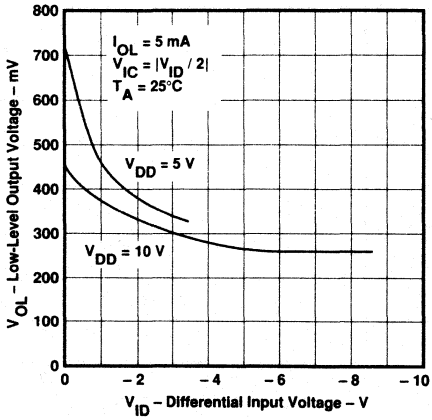


FIGURE 16

LOW-LEVEL OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE

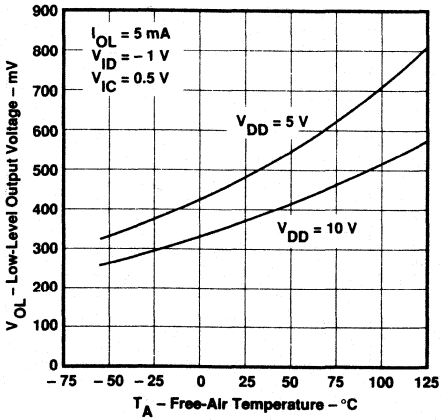


FIGURE 17

TYPICAL CHARACTERISTICS

LOW-LEVEL OUTPUT VOLTAGE
vs
LOW-LEVEL OUTPUT CURRENT

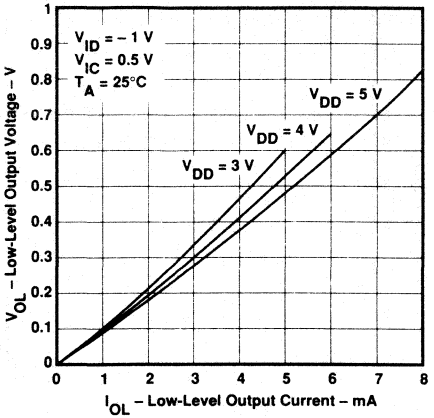


FIGURE 18

LOW-LEVEL OUTPUT VOLTAGE
vs
LOW-LEVEL OUTPUT CURRENT

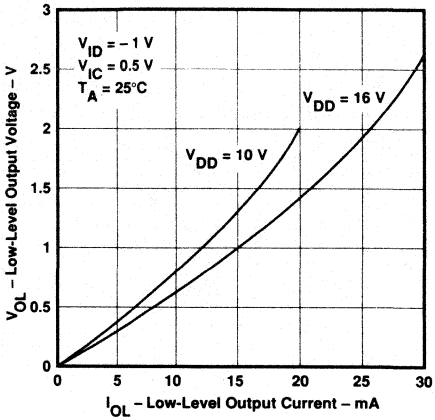


FIGURE 19

LARGE-SIGNAL
DIFFERENTIAL VOLTAGE AMPLIFICATION
vs
SUPPLY VOLTAGE

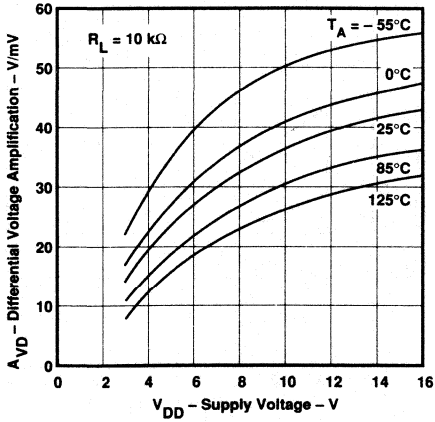


FIGURE 20

LARGE-SIGNAL
DIFFERENTIAL VOLTAGE AMPLIFICATION
vs
FREE-AIR TEMPERATURE

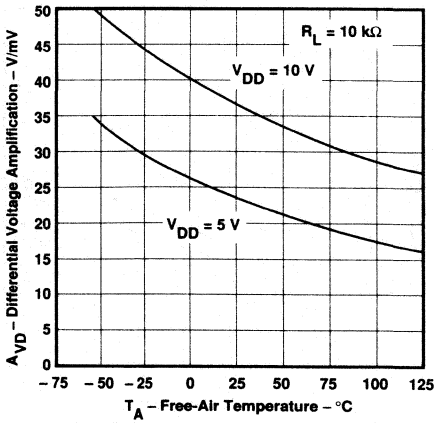


FIGURE 21

TYPICAL CHARACTERISTICS

INPUT BIAS CURRENT AND INPUT OFFSET CURRENT
vs
FREE-AIR TEMPERATURE

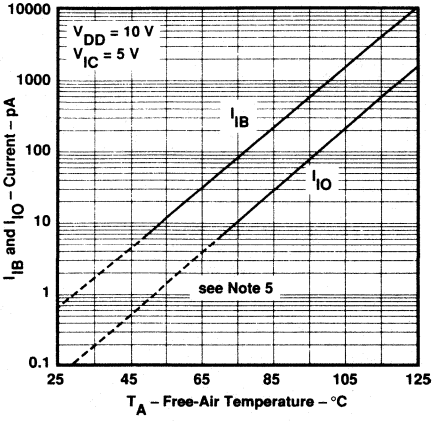


FIGURE 22

MAXIMUM INPUT VOLTAGE
vs
SUPPLY VOLTAGE

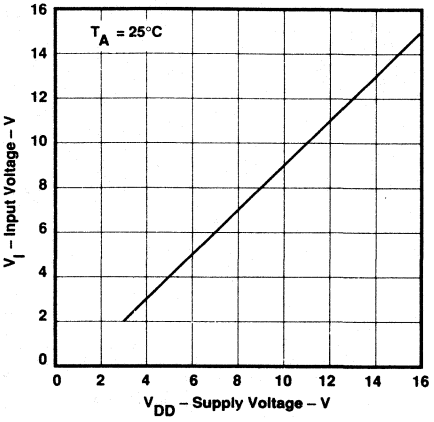


FIGURE 23

SUPPLY CURRENT
vs
SUPPLY VOLTAGE

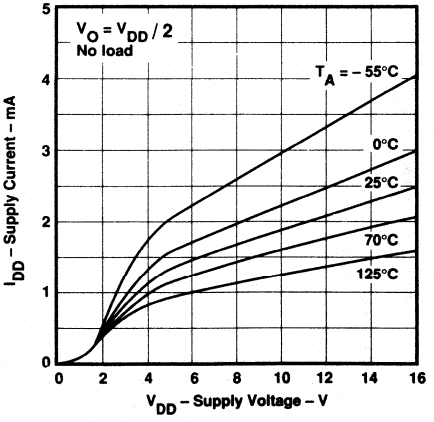


FIGURE 24

SUPPLY CURRENT
vs
FREE-AIR TEMPERATURE

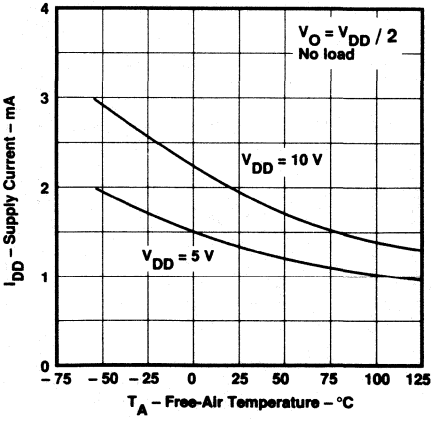


FIGURE 25

NOTE 5: The typical values of input bias current and input offset current below 5 pA were determined mathematically.

TYPICAL CHARACTERISTICS

SLEW RATE
vs
SUPPLY VOLTAGE

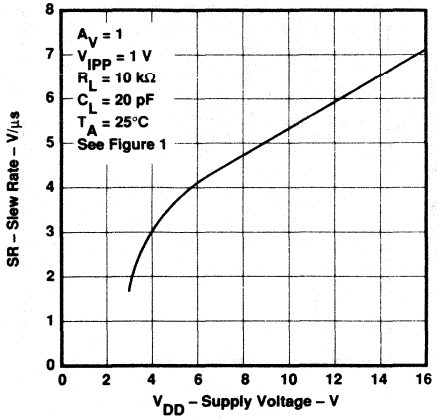


FIGURE 26

SLEW RATE
vs
FREE-AIR TEMPERATURE

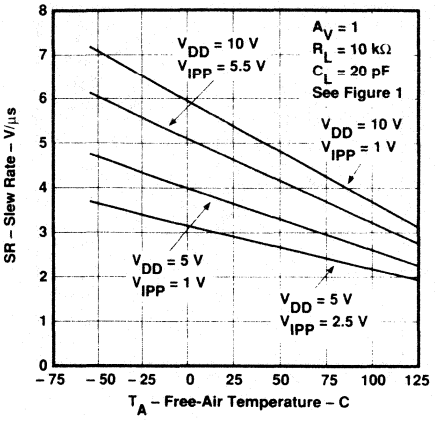


FIGURE 27

NORMALIZED SLEW RATE
vs
FREE-AIR TEMPERATURE

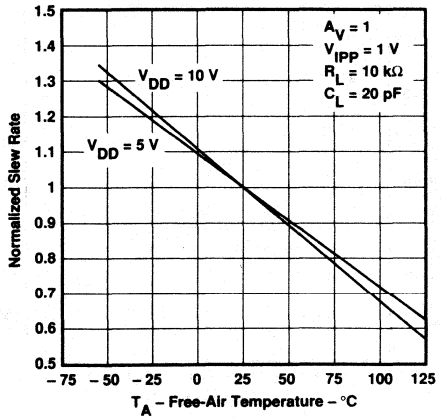


FIGURE 28

MAXIMUM PEAK-TO-PEAK OUTPUT VOLTAGE
vs
FREQUENCY

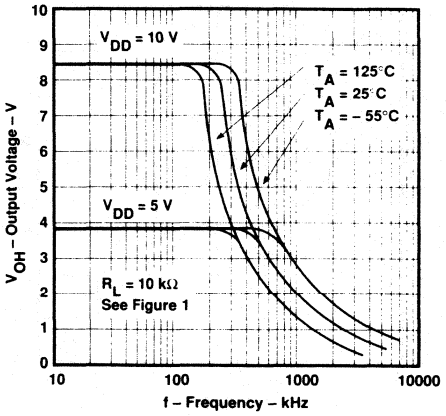


FIGURE 29

TYPICAL CHARACTERISTICS

UNITY-GAIN BANDWIDTH
vs
FREE-AIR TEMPERATURE

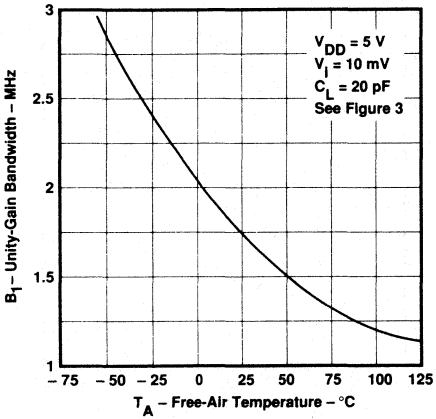


FIGURE 30

UNITY-GAIN BANDWIDTH
vs
SUPPLY VOLTAGE

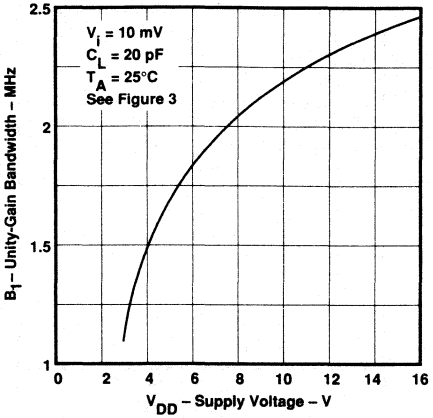


FIGURE 31

LARGE-SIGNAL DIFFERENTIAL VOLTAGE
AMPLIFICATION AND PHASE SHIFT
vs
FREQUENCY

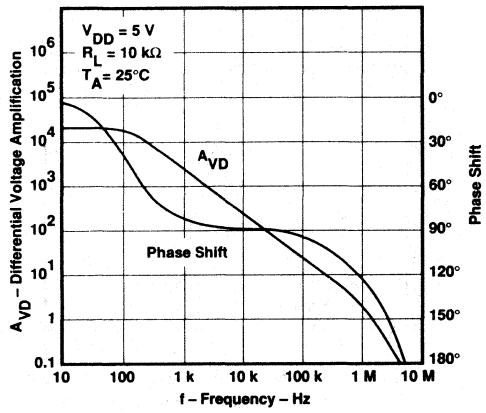


FIGURE 32

LARGE-SIGNAL DIFFERENTIAL VOLTAGE
AMPLIFICATION AND PHASE SHIFT
vs
FREQUENCY

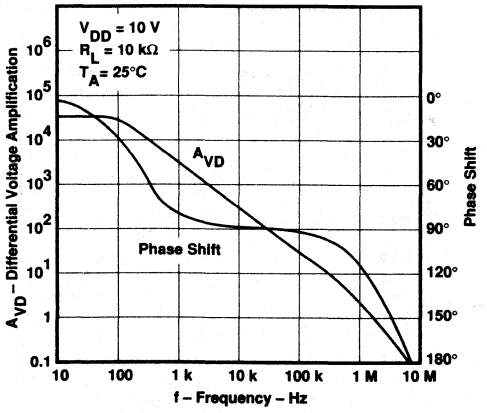


FIGURE 33

TYPICAL CHARACTERISTICS

PHASE MARGIN
vs
SUPPLY VOLTAGE

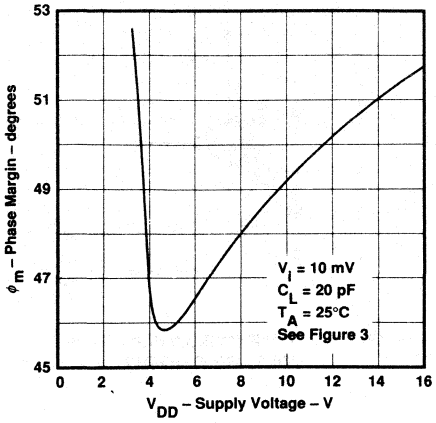


FIGURE 34

PHASE MARGIN
vs
FREE-AIR TEMPERATURE

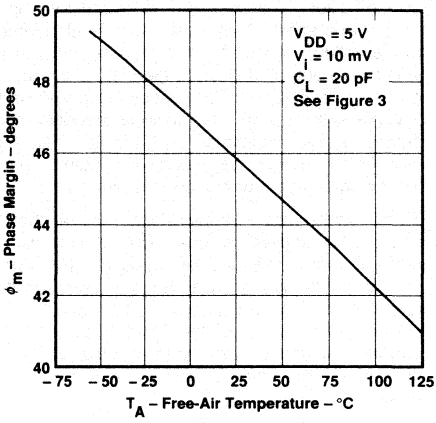


FIGURE 35

PHASE MARGIN
vs
CAPACITIVE LOAD

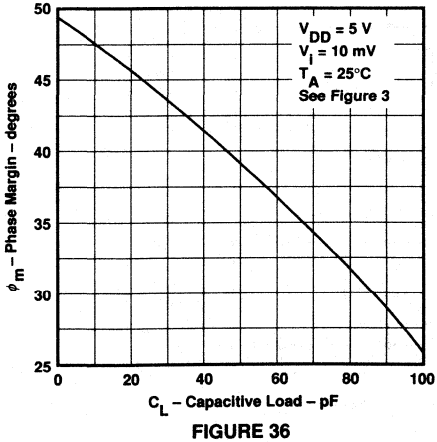


FIGURE 36

EQUIVALENT INPUT NOISE VOLTAGE
vs
FREQUENCY

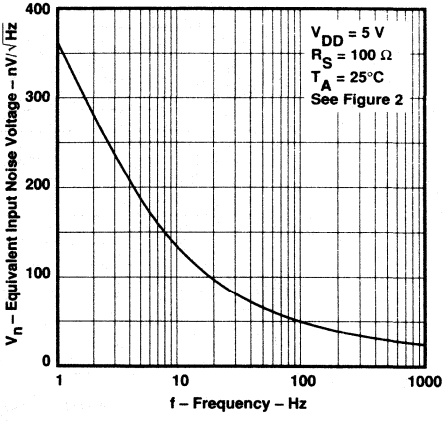


FIGURE 37

TYPICAL APPLICATION DATA

single-supply operation

While the TLC272 and TLC277 will perform well using dual power supplies (also called balanced or split supplies), the design is optimized for single-supply operation. This includes an input common mode voltage range that encompasses ground as well as an output voltage range that pulls down to ground. The supply voltage range extends down to 3 V (C- suffix types), thus allowing operation with supply levels commonly available for TTL and HCMOS; however, for maximum dynamic range, 16-V single-supply operation is recommended.

Many single-supply applications require that a voltage be applied to one input to establish a reference level that is above ground. A resistive voltage divider is usually sufficient to establish this reference level (see Figure 38). The low input bias current consumption of the TLC272 and TLC277 permits the use of very large resistive values to implement the voltage divider, thus minimizing power consumption.

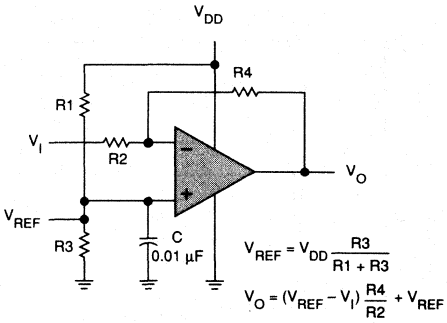
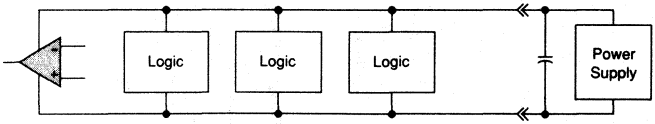


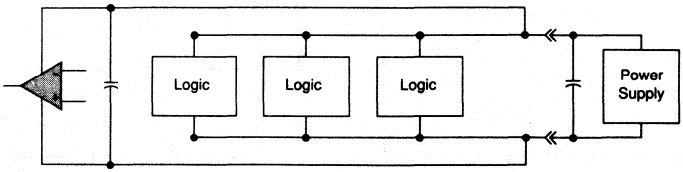
FIGURE 38. INVERTING AMPLIFIER WITH VOLTAGE REFERENCE

The TLC272 and TLC277 work well in conjunction with digital logic; however, when powering both linear devices and digital logic from the same power supply, the following precautions are recommended:

1. Power the linear devices from separate bypassed supply lines (see Figure 39); otherwise the linear device supply rails can fluctuate due to voltage drops caused by high switching currents in the digital logic.
2. Use proper bypass techniques to reduce the probability of noise-induced errors. Single capacitive decoupling is often adequate; however, RC decoupling may be necessary in high-frequency applications.



(a) Common Supply Rails



(b) Separate Bypassed Supply Rails (preferred)

FIGURE 39. COMMON VERSUS SEPARATE SUPPLY RAILS

TYPICAL APPLICATION DATA

input characteristics

The TLC272 and TLC277 are specified with a minimum and a maximum input voltage that, if exceeded at either input, could cause the device to malfunction. Exceeding this specified range is a common problem, especially in single-supply operation. Note that the lower range limit includes the negative rail, while the upper range limit is specified at V_{DD} – 1 V at T_A = 25°C and at V_{DD} – 1.5 V at all other temperatures.

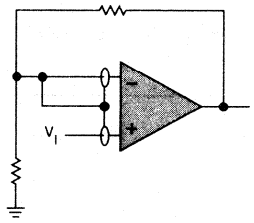
The use of the polysilicon-gate process and the careful input circuit design gives the TLC272 and TLC277 very good input offset voltage drift characteristics relative to conventional metal-gate processes. Offset voltage drift in CMOS devices is highly influenced by threshold voltage shifts caused by polarization of the phosphorus dopant implanted in the oxide. Placing the phosphorus dopant in a conductor (such as a polysilicon gate) alleviates the polarization problem, thus reducing threshold voltage shifts by more than an order of magnitude. The offset voltage drift with time has been calculated to be typically 0.1 μV/month, including the first month of operation.

Because of the extremely high input impedance and resulting low bias current requirements, the TLC272 and TLC277 are well suited for low-level signal processing; however, leakage currents on printed circuit boards and sockets can easily exceed bias current requirements and cause a degradation in device performance. It is good practice to include guard rings around inputs (similar to those of Figure 4 in the PARAMETER MEASUREMENT INFORMATION section). These guards should be driven from a low-impedance source at the same voltage level as the common-mode input (see Figure 40).

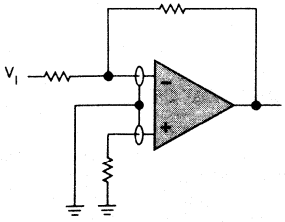
The inputs of any unused amplifiers should be tied to ground to avoid possible oscillation.

noise performance

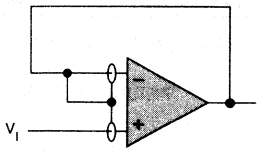
The noise specifications in op amp circuits are greatly dependent on the current in the first-stage differential amplifier. The low input bias current requirements of the TLC272 and TLC277 result in a very low noise current, which is insignificant in most applications. This feature makes the devices especially favorable over bipolar devices when using values of circuit impedance greater than 50 kΩ, since bipolar devices exhibit greater noise currents.



(a) Noninverting Amplifier



(b) Inverting Amplifier



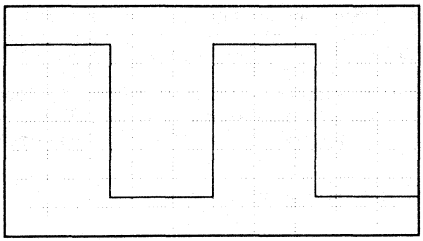
(c) Unity Gain Amplifier

Figure 40. GUARD RING SCHEMES

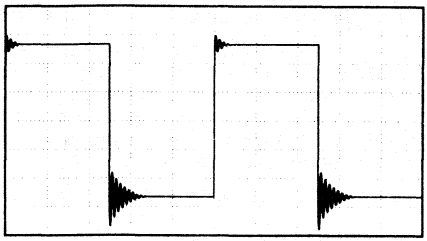
output characteristics

The output stage of the TLC272 and TLC277 is designed to sink and source relatively high amounts of current (see typical characteristics). If the output is subjected to a short-circuit condition, this high current capability can cause device damage under certain conditions. Output current capability increases with supply voltage.

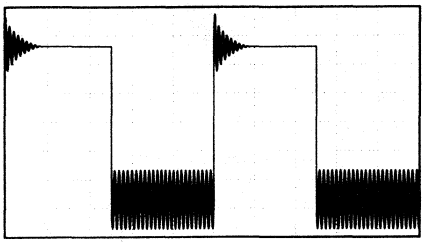
All operating characteristics of the TLC272 and TLC277 were measured using a 20-pF load. The devices will drive higher capacitive loads; however, as output load capacitance increases, the resulting response pole occurs at lower frequencies, thereby causing ringing, peaking, or even oscillation (see Figure 41). In many cases, adding some compensation in the form of a series resistor in the feedback loop will alleviate the problem.



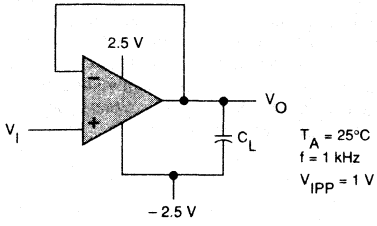
(a) C_L = 20 pF, R_L = no load



(b) C_L = 130 pF, R_L = no load



(c) C_L = 150 pF, R_L = no load



(d) Test Circuit

FIGURE 41. EFFECT OF CAPACITIVE LOADS AND TEST CIRCUIT

Although the TLC272 and TLC277 possess excellent high-level output voltage and current capability, methods are available for boosting this capability, if needed. The simplest method involves the use of a pull-up resistor connected from the output to the positive supply rail. There are two disadvantages to the use of this circuit. First, the NMOS pull-down transistor, N4 (see Figure 42) must sink a comparatively large amount of current. In this circuit, N4 behaves like a linear resistor with an on resistance between approximately 60 Ω and 180 Ω, depending on how hard the op amp input is driven. With very low values of R6, a voltage offset from 0 V at the output will occur. Secondly, pull-up resistor R6 acts as a drain load to N4 and the gain of the op amp is reduced at output voltage levels where N5 is not supplying the output current.

TYPICAL APPLICATION DATA

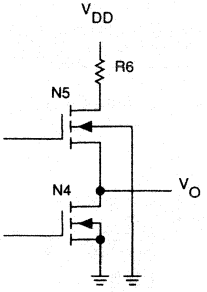


FIGURE 42. TLC272 / TLC277 OUTPUT STAGE

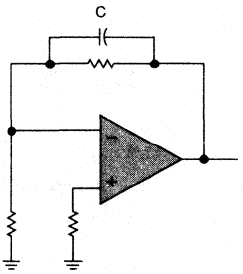


FIGURE 43. COMPENSATION FOR INPUT CAPACITANCE

feedback

Op amp circuits nearly always employ feedback, and since feedback is the first prerequisite for oscillation, a little caution is appropriate. Most oscillation problems result from driving capacitive loads (discussed previously) and ignoring stray input capacitance. A small-value capacitor connected in parallel with the feedback resistor is an effective remedy (see Figure 43). The value of this capacitor is optimized empirically.

electrostatic discharge protection

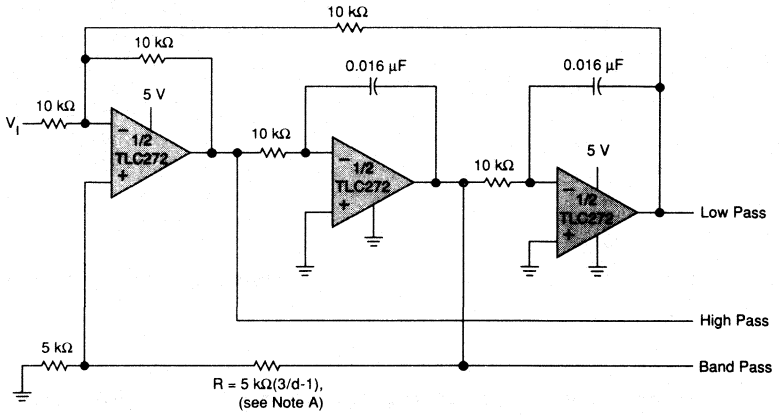
The TLC272 and TLC277 incorporate an internal electrostatic discharge (ESD) protection circuit that will prevent functional failures at voltages up to 2000 V as tested under MIL-STD-883C, Method 3015.2. Care should be exercised, however, when handling these devices as exposure to ESD may result in the degradation of the device parametric performance. The protect circuit also causes the input bias currents to be temperature dependent and have the characteristics of a reverse-biased diode.

latchup

Because CMOS devices are susceptible to latchup due to their inherent parasitic thyristors, the TLC272 and TLC277 inputs and outputs were designed to withstand −100-mA surge currents without sustaining latchup; however, techniques should be used to reduce the chance of latchup whenever possible. Internal protection diodes should not by design be forward biased. Applied input and output voltage should not exceed the supply voltage by more than 300 mV. Care should be exercised when using capacitive coupling on pulse generators. Supply transients should be shunted by the use of decoupling capacitors (0.1 μF typical) located across the supply rails as close to the device as possible.

The current path established if latchup occurs is usually between the positive supply rail and ground and can be triggered by surges on the supply lines and / or voltages on either the output or inputs that exceed the supply voltage. Once latchup occurs, the current flow is limited only by the impedance of the power supply and the forward resistance of the parasitic thyristor and usually results in the destruction of the device. The chance of latchup occuring increases with increasing temperature and supply voltages.

TYPICAL APPLICATION DATA



NOTES: A. d = damping factor, 1/Q
B. Normalized to 10 kΩ and f_C = 1 kHz

FIGURE 44. STATE VARIABLE FILTER

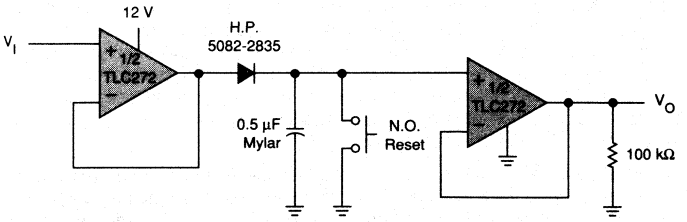
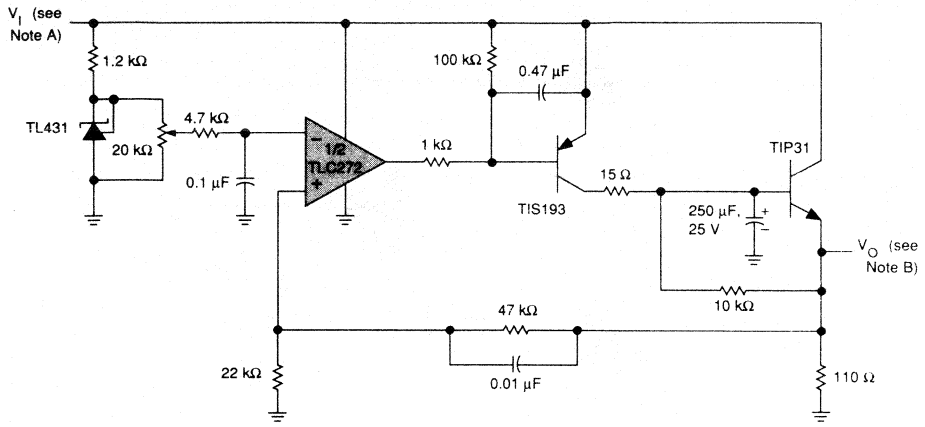


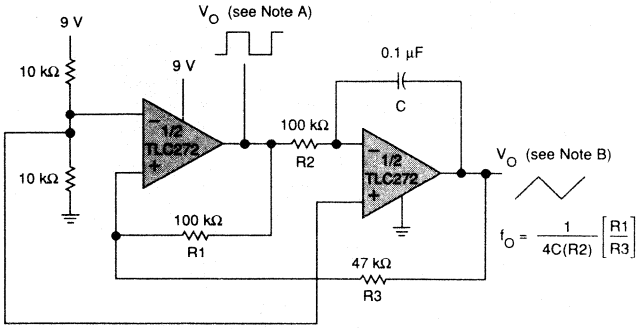
FIGURE 45. POSITIVE-PEAK DETECTOR

TYPICAL APPLICATION DATA



NOTES: A. V_I = 3.5 to 15 V
B. V_O = 2.0 V, 0 to 1 A

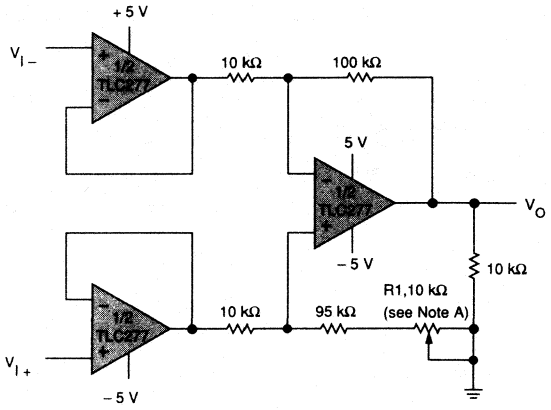
FIGURE 46. LOGIC ARRAY POWER SUPPLY



NOTES: A. V_{OPP} = 8 V
B. V_{OPP} = 4 V

FIGURE 47. SINGLE-SUPPLY FUNCTION GENERATOR

TYPICAL APPLICATION DATA



NOTE A: CMRR Adjustment (must be noninductive).

FIGURE 48. LOW-POWER INSTRUMENTATION AMPLIFIER

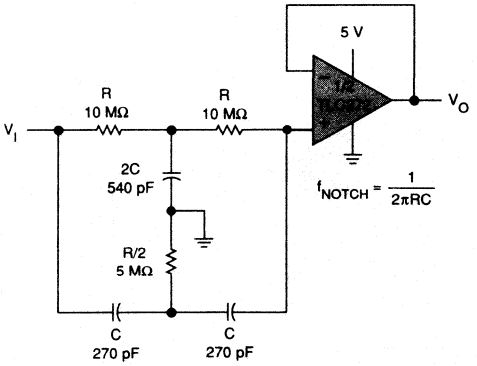
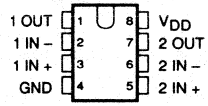


FIGURE 49. SINGLE-SUPPLY TWIN-T NOTCH FILTER

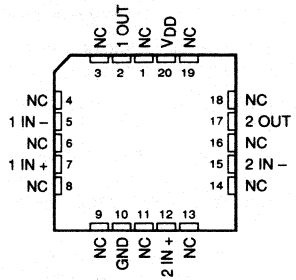
OCTOBER 1987

- **Trimmed Offset Voltage:**
  TLC27M7 . . . 500 μV Max at 25°C, V_{DD} = 5 V
- **Input Offset Voltage Drift Typically**
  0.1 μV / Month, Including the First 30 Days
- **Wide Range of Supply Voltages over Specified Temperature Range:**
  – 55°C to125°C . . . 4 V to 16 V
  – 40°C to 85°C . . . 4 V to 16 V
  0°C to 70°C . . . 3 V to 16 V
- **Single-Supply Operation**
- **Common-Mode Input Voltage Range Extends Below the Negative Rail (C- suffix, I- suffix types)**
- **Low Noise . . . 32 nV/√Hz Typically at f = 1 kHz**
- **Low Power . . . 2.1 mW Typically at 25°C, V_{DD} = 5 V**
- **Output Voltage Range Includes Negative Rail**
- **High Input Impedance . . . 10^{12} Ω Typical**
- **ESD Protection Circuitry**
- **Small-Outline Package Option Also Available in Tape-and-Reel**
- **Designed-In Latchup Immunity**

JG AND P DUAL-IN-LINE PACKAGE
D SMALL-OUTLINE PACKAGE
(TOP VIEW)



FK CHIP CARRIER PACKAGE
(TOP VIEW)



NC – No internal connection

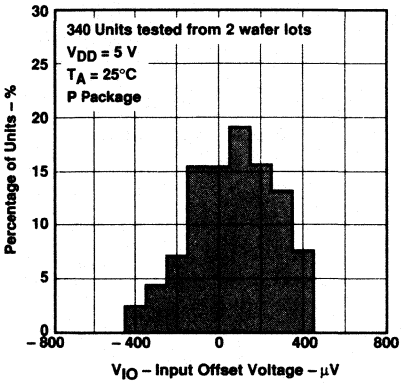
description

The TLC27M2 and TLC27M7 dual operational amplifiers combine a wide range of input offset voltage grades with low offset voltage drift, high input impedance, low noise, and speeds

T_A	V_{IO}max at 25°C	PACKAGE			
		Small-Outline (D) See Note 1	Plastic DIP (P)	Ceramic DIP (JG)	Chip Carrier (FK)
0°C to 70°C	500 μV	TLC27M7CD	TLC27M7CP	TLC27M7CJG	—
	2 mV	TLC27M2BCD	TLC27M2BCP	TLC27M2BCJG	—
	5 mV	TLC27M2ACD	TLC27M2ACP	TLC27M2ACJG	—
	10 mV	TLC27M2CD	TLC27M2CP	TLC27M2CJG	—
– 40°C to 85°C	500 μV	TLC27M7ID	TLC27M7IP	TLC27M7IJG	—
	2 mV	TLC27M2BID	TLC27M2BIP	TLC27M2BIJG	—
	5 mV	TLC27M2AID	TLC27M2AIP	TLC27M2AIJG	—
	10 mV	TLC27M2ID	TLC27M2IP	TLC27M2IJG	—
– 55°C to 125°C	500 μV	—	—	TLC27M7MJG	TLC27M7MFK
	10 mV	—	—	TLC27M2MJG	TLC27M2MFK

NOTE 1: Available in tape-and-reel. Add "R" suffix to the device type when ordering (e.g., TLC27M7CDR).

DISTRIBUTION OF TLC27M7
INPUT OFFSET VOLTAGE



LinCMOS is a trademark of Texas Instruments Incorporated

description (continued)

comparable to that of general-purpose bipolar devices. These devices use Texas Instruments silicon-gate LinCMOS technology, which provides offset voltage stability far exceeding the stability available with conventional metal-gate processes.

The extremely high input impedance and low bias currents make these cost-effective devices ideal for applications which have previously been reserved for general-purpose bipolar products, but with only a fraction of the power consumption. Four offset voltage grades are available (C- suffix and I- suffix types), ranging from the low-cost TLC27M2 (10 mV) to the high-precision TLC27M7 (500 μV). These advantages, in combination with good common-mode rejection and supply voltage rejection, make these devices a good choice for new state-of-the-art designs as well as for upgrading existing designs.

In general, many features associated with bipolar technology are avaliable on LinCMOS operational amplifiers, without the power penalties of bipolar technology. General applications such as transducer interfacing, analog calculations, amplifier blocks, active filters, and signal buffering are all easily designed with the TLC27M2 and TLC27M7. The devices also exhibit low voltage single supply operation and low power consumption making them ideally suited for remote and inaccessible battery-powered applications. The common-mode input voltage range includes the negative rail.

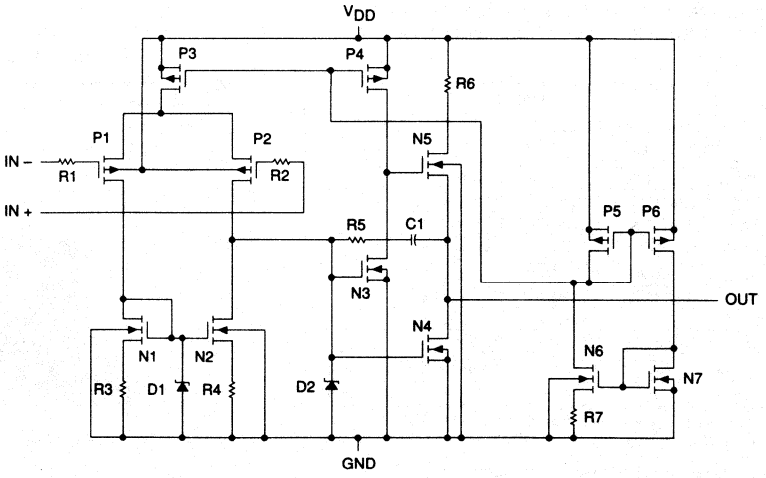
A wide range of packaging options is available, including small outline and chip carrier versions for high-density system applications.

The device inputs and outputs are designed to withstand – 100-mA surge currents without sustaining latchup.

The TLC27M2 and TLC27M7 incorporate internal ESD protection circuits that will prevent functional failures at voltages up to 2000 V as tested under MIL-STD-883C, Method 3015.2; however, care should be exercised in handling these devices as exposure to ESD may result in the degradation of the device parametric performance.

The M- suffix devices are characterized for operation over the full military temperature range of – 55°C to 125°C, the I- suffix devices from – 40°C to 85°C, and the C- suffix devices from 0°C to 70°C.

equivalent schematic (each amplifier)



absolute maximum ratings over operating free-air temperature (unless otherwise noted)

Supply voltage, V_{DD} (see Note 2) . . . . . 18 V
Differential input voltage (see Note 3) . . . . . ± V_{DD}
Input voltage range, V_I (any input) . . . . . − 0.3 V to V_{DD}
Input current, I_I . . . . . ± 5 mA
Output current, I_O (each output) . . . . . ± 30 mA
Total current into V_{DD} terminal . . . . . 45 mA
Total current out of ground terminal . . . . . 45 mA
Duration of short-circuit current at (or below) 25°C (see Note 4) . . . . . Unlimited
Continuous total dissipation . . . . . See Dissipation Rating Table
Operating free-air temperature, T_A: C-suffix types . . . . . 0°C to 70°C
I-suffix types . . . . . − 40°C to 85°C
M-suffix types . . . . . − 55°C to 125°C
Storage temperature range . . . . . − 65°C to 150°C
Case temperature for 60 seconds: FK package . . . . . 260°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds: JG package . . . . . 300°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: D and P package . . . . . 260°C

DISSIPATION RATING TABLE

PACKAGE	$T_A \leq 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING	$T_A = 85°C$ POWER RATING	$T_A = 125°C$ POWER RATING
D	725 mW	5.8 mW/°C	464 mW	377 mW	
FK	1375 mW	11 mW/°C	880 mW	715 mW	275 mW
JG (C-, I- suffix)	825 mW	6.6 mW/°C	528 mW	429 mW	
JG (M- suffix)	1050 mW	8.4 mW/°C	672 mW	546 mW	210 mW
P	1000 mW	8.0 mW/°C	640 mW	520 mW	

recommended operating conditions

		M- SUFFIX TYPES			I- SUFFIX TYPES			C- SUFFIX TYPES			
		MIN	NOM	MAX	MIN	NOM	MAX	MIN	NOM	MAX	UNIT
Supply voltage, V_{DD}		4		16	4		16	3		16	V
Common-mode input voltage, V_{IC}	$V_{DD} = 5$ V	0		3.5	− 0.2		3.5	− 0.2		3.5	V
	$V_{DD} = 10$ V	0		8.5	− 0.2		8.5	− 0.2		8.5	V
Input voltage, V_I	$V_{DD} = 5$ V	0		3.5	− 0.2		3.5	− 0.2		3.5	V
	$V_{DD} = 10$ V	0		8.5	− 0.2		8.5	− 0.2		8.5	V
Operating free-air temperature, T_A		− 55		125	− 40		85	0		70	°C

NOTES: 2. All voltage values, except differential voltages, are with respect to network ground.
3. Differential voltages are at the noninverting input with respect to the inverting input.
4. The output may be shorted to either supply. Temperature and/or supply voltages must be limited to ensure that the maximum dissipation rating is not exceeded (see application section).

electrical characteristics at specified free-air temperature, V_{DD} = 5 V (unless otherwise noted)

PARAMETER			TEST CONDITIONS		C- SUFFIX TYPES MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage	TLC27M2C	V_O = 1.4 V, V_{IC} = 0 V, R_S = 50 Ω, R_L = 100 kΩ	25°C		1.1	10	mV
				Full range			12	
		TLC27M2AC	V_O = 1.4 V, V_{IC} = 0 V, R_S = 50 Ω, R_L = 100 kΩ	25°C		0.9	5	
				Full range			6.5	
		TLC27M2BC	V_O = 1.4 V, V_{IC} = 0 V, R_S = 50 Ω, R_L = 100 kΩ	25°C		220	2000	μV
				Full range			3000	
		TLC27M7C	V_O = 1.4 V, V_{IC} = 0 V, R_S = 50 Ω, R_L = 100 kΩ	25°C		185	500	
				Full range			1500	
α_{VIO}	Average temperature coefficient of input offset voltage			25°C to 70°C		1.7		μV/°C
I_{IO}	Input offset current (see Note 5)		V_{IC} = 2.5 V, V_O = 2.5 V	25°C		0.1		pA
				70°C		7	300	
I_{IB}	Input bias current (see Note 5)		V_{IC} = 2.5 V, V_O = 2.5 V	25°C		0.6		pA
				70°C		40	600	
V_{ICR}	Common-mode input voltage range (see Note 6)			25°C	−0.2 to 4	−0.3 to 4.2		V
				Full range	−0.2 to 3.5			V
V_{OH}	High-level output voltage		V_{ID} = 100 mV, R_L = 100 kΩ	25°C	3.2	3.9		V
				70°C	3	4		
				0°C	3	3.9		
V_{OL}	Low-level output voltage		V_{ID} = −100 mV, I_{OL} = 0	25°C		0	50	mV
				70°C		0	50	
				0°C		0	50	
A_{VD}	Large-signal differential voltage amplification		V_O = 0.25 V to 2 V, R_L = 100 kΩ	25°C	25	170		V/mV
				70°C	15	140		
				0°C	15	200		
CMRR	Common-mode rejection ratio		V_{IC} = V_{ICR} min	25°C	65	91		dB
				70°C	60	92		
				0°C	60	91		
k_{SVR}	Supply-voltage rejection ratio (ΔV_{DD} / ΔV_{IO})		V_{DD} = 5 V to 10 V, V_O = 1.4 V	25°C	70	93		dB
				70°C	60	94		
				0°C	60	92		
I_{DD}	Supply current (two amplifiers)		No load, V_O = 2.5 V, V_{IC} = 2.5 V	25°C		210	560	μA
				70°C		170	440	
				0°C		250	640	

NOTES: 5. The typical values of input bias current and input offset current below 5 pA were determined mathematically.
6. This range also applies to each input individually.

electrical characteristics at specified free-air temperature, V_{DD} = 10 V (unless otherwise noted)

PARAMETER			TEST CONDITIONS		C- SUFFIX TYPES MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage	TLC27M2C	V_O = 1.4 V, V_{IC} = 0 V, R_S = 50 Ω, R_L = 100 kΩ	25°C		1.1	10	mV
				Full range			12	
		TLC27M2AC	V_O = 1.4 V, V_{IC} = 0 V, R_S = 50 Ω, R_L = 100 kΩ	25°C		0.9	5	
				Full range			6.5	
		TLC27M2BC	V_O = 1.4 V, V_{IC} = 0 V, R_S = 50 Ω, R_L = 100 kΩ	25°C		224	2000	μV
				Full range			3000	
		TLC27M7C	V_O = 1.4 V, V_{IC} = 0 V, R_S = 50 Ω, R_L = 100 kΩ	25°C		190	800	
				Full range			1900	
α_{VIO}	Average temperature coefficient of input offset voltage			25°C to 70°C		2.1		μV/°C
I_{IO}	Input offset current (see Note 5)		V_{IC} = 5 V, V_O = 5 V	25°C		0.1		pA
				70°C		8	300	
I_{IB}	Input bias current (see Note 5)		V_{IC} = 5 V, V_O = 5 V	25°C		0.7		pA
				70°C		50	600	
V_{ICR}	Common-mode input voltage range (see Note 6)			25°C	−0.2 to 9	−0.3 to 9.2		V
				Full range	−0.2 to 8.5			V
V_{OH}	High-level output voltage		V_{ID} = 100 mV, R_L = 100 kΩ	25°C	8	8.7		V
				70°C	7.8	8.7		
				0°C	7.8	8.7		
V_{OL}	Low-level output voltage		V_{ID} = −100 mV, I_{OL} = 0	25°C		0	50	mV
				70°C		0	50	
				0°C		0	50	
A_{VD}	Large-signal differential voltage amplification		V_O = 1 V to 6 V, R_L = 100 kΩ	25°C	25	275		V/mV
				70°C	15	230		
				0°C	15	320		
CMRR	Common-mode rejection ratio		V_{IC} = V_{ICR} min	25°C	65	94		dB
				70°C	60	94		
				0°C	60	94		
k_{SVR}	Supply-voltage rejection ratio (ΔV_{DD} / ΔV_{IO})		V_{DD} = 5 V to 10 V, V_O = 1.4 V	25°C	70	93		dB
				70°C	60	94		
				0°C	60	92		
I_{DD}	Supply current (two amplifiers)		No load, V_O = 5 V, V_{IC} = 5 V	25°C		285	600	μA
				70°C		220	560	
				0°C		345	800	

NOTES: 5. The typical values of input bias current and input offset current below 5 pA were determined mathematically.
6. This range also applies to each input individually.

electrical characteristics at specified free-air temperature, V_{DD} = 5 V (unless otherwise noted)

PARAMETER			TEST CONDITIONS		I- SUFFIX TYPES MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage	TLC27M2I	V_O = 1.4 V, V_{IC} = 0 V, R_S = 50 Ω, R_L = 100 kΩ	25°C		1.1	10	mV
				Full range			13	
		TLC27M2AI	V_O = 1.4 V, V_{IC} = 0 V, R_S = 50 Ω, R_L = 100 kΩ	25°C		0.9	5	
				Full range			7	
		TLC27M2BI	V_O = 1.4 V, V_{IC} = 0 V, R_S = 50 Ω, R_L = 100 kΩ	25°C		220	2000	µV
				Full range			3500	
		TLC27M7I	V_O = 1.4 V, V_{IC} = 0 V, R_S = 50 Ω, R_L = 100 kΩ	25°C		185	500	
				Full range			2000	
α_{VIO}	Average temperature coefficient of input offset voltage			25°C to 85°C		1.7		µV/°C
I_{IO}	Input offset current (see Note 5)		V_{IC} = 2.5 V, V_O = 2.5 V	25°C		0.1		pA
				85°C		24	1000	
I_{IB}	Input bias current (see Note 5)		V_{IC} = 2.5 V, V_O = 2.5 V	25°C		0.6		pA
				85°C		200	2000	
V_{ICR}	Common-mode input voltage range (see Note 6)			25°C	−0.2 to 4	−0.3 to 4.2		V
				Full range	−0.2 to 3.5			V
V_{OH}	High-level output voltage		V_{ID} = 100 mV, R_L = 100 kΩ	25°C	3.2	3.9		V
				85°C	3	4		
				−40°C	3	3.9		
V_{OL}	Low-level output voltage		V_{ID} = −100 mV, I_{OL} = 0	25°C		0	50	mV
				85°C		0	50	
				−40°C		0	50	
A_{VD}	Large-signal differential voltage amplification		V_O = 0.25 V to 2 V, R_L = 100 kΩ	25°C	25	170		V/mV
				85°C	15	130		
				−40°C	15	270		
CMRR	Common-mode rejection ratio		V_{IC} = V_{ICR} min	25°C	65	91		dB
				85°C	60	90		
				−40°C	60	90		
k_{SVR}	Supply-voltage rejection ratio (ΔV_{DD} / ΔV_{IO})		V_{DD} = 5 V to 10 V, V_O = 1.4 V	25°C	70	93		dB
				85°C	60	94		
				−40°C	60	91		
I_{DD}	Supply current (two amplifiers)		No load, V_O = 2.5 V, V_{IC} = 2.5 V	25°C		210	560	µA
				85°C		160	400	
				−40°C		315	800	

NOTES: 5. The typical values of input bias current and input offset current below 5 pA were determined mathematically.
6. This range also applies to each input individually.

electrical characteristics at specified free-air temperature, V_{DD} = 10 V (unless otherwise noted)

PARAMETER			TEST CONDITIONS		I- SUFFIX TYPES MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage	TLC27M2I	V_O = 1.4 V, V_{IC} = 0 V, R_S = 50 Ω, R_L = 100 kΩ	25°C		1.1	10	mV
				Full range			13	
		TLC27M2AI	V_O = 1.4 V, V_{IC} = 0 V, R_S = 50 Ω, R_L = 100 kΩ	25°C		0.9	5	
				Full range			7	
		TLC27M2BI	V_O = 1.4 V, V_{IC} = 0 V, R_S = 50 Ω, R_L = 100 kΩ	25°C		224	2000	μV
				Full range			3500	
		TLC27M7I	V_O = 1.4 V, V_{IC} = 0 V, R_S = 50 Ω, R_L = 100 kΩ	25°C		190	800	
				Full range			2900	
α_{VIO}	Average temperature coefficient of input offset voltage			25°C to 85°C		2.1		μV/°C
I_{IO}	Input offset current (see Note 5)		V_{IC} = 5 V, V_O = 5 V	25°C		0.1		pA
				85°C		26	1000	
I_{IB}	Input bias current (see Note 5)		V_{IC} = 5 V, V_O = 5 V	25°C		0.7		pA
				85°C		220	2000	
V_{ICR}	Common-mode input voltage range (see Note 6)			25°C	−0.2 to 9	−0.3 to 9.2		V
				Full range	−0.2 to 8.5			V
V_{OH}	High-level output voltage		V_{ID} = 100 mV, R_L = 100 kΩ	25°C	8	8.7		V
				85°C	7.8	8.7		
				−40°C	7.8	8.7		
V_{OL}	Low-level output voltage		V_{ID} = −100 mV, I_{OL} = 0	25°C		0	50	mV
				85°C		0	50	
				−40°C		0	50	
A_{VD}	Large-signal differential voltage amplification		V_O = 1 V to 6 V, R_L = 100 kΩ	25°C	25	275		V/mV
				85°C	15	220		
				−40°C	15	390		
CMRR	Common-mode rejection ratio		V_{IC} = V_{ICR} min	25°C	65	94		dB
				85°C	60	94		
				−40°C	60	93		
k_{SVR}	Supply-voltage rejection ratio (ΔV_{DD} / ΔV_{IO})		V_{DD} = 5 V to 10 V, V_O = 1.4 V	25°C	70	93		dB
				85°C	60	94		
				−40°C	60	91		
I_{DD}	Supply current (two amplifiers)		No load, V_O = 5 V, V_{IC} = 5 V	25°C		285	600	μA
				85°C		205	520	
				−40°C		450	900	

NOTES: 5. The typical values of input bias current and input offset current below 5 pA were determined mathematically.
6. This range also applies to each input individually.

electrical characteristics at specified free-air temperature, V_{DD} = 5 V (unless otherwise noted)

PARAMETER			TEST CONDITIONS		M- SUFFIX TYPES MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage	TLC27M2M	V_O = 1.4 V, V_{IC} = 0 V, R_S = 50 Ω, R_L = 100 kΩ	25°C		1.1	10	mV
				Full range			12	
		TLC27M7M	V_O = 1.4 V, V_{IC} = 0 V, R_S = 50 Ω, R_L = 100 kΩ	25°C		185	500	μV
				Full range			3750	
α_{VIO}	Average temperature coefficient of input offset voltage			25°C to 125°C		1.7		μV/°C
I_{IO}	Input offset current (see Note 5)		V_{IC} = 2.5 V, V_O = 2.5 V	25°C		0.1		pA
				125°C		1.4	15	nA
I_{IB}	Input bias current (see Note 5)		V_{IC} = 2.5 V, V_O = 2.5 V	25°C		0.6		pA
				125°C		9	35	nA
V_{ICR}	Common-mode input voltage range (see Note 6)			25°C	0 to 4	−0.3 to 4.2		V
				Full range	0 to 3.5			V
V_{OH}	High-level output voltage		V_{ID} = 100 mV, R_L = 100 kΩ	25°C	3.2	3.9		V
				125°C	3	4		
				−55°C	3	3.9		
V_{OL}	Low-level output voltage		V_{ID} = −100 mV, I_{OL} = 0	25°C		0	50	mV
				125°C		0	50	
				−55°C		0	50	
A_{VD}	Large-signal differential voltage amplification		V_O = 0.25 V to 2 V, R_L = 100 kΩ	25°C	25	170		V/mV
				125°C	15	120		
				−55°C	15	290		
CMRR	Common-mode rejection ratio		V_{IC} = V_{ICR} min	25°C	65	91		dB
				125°C	60	91		
				−55°C	60	89		
k_{SVR}	Supply-voltage rejection ratio (ΔV_{DD} / ΔV_{IO})		V_{DD} = 5 V to 10 V, V_O = 1.4 V	25°C	70	93		dB
				125°C	60	94		
				−55°C	60	91		
I_{DD}	Supply current (two amplifiers)		No load, V_O = 2.5 V, V_{IC} = 2.5 V	25°C		210	560	μA
				125°C		140	360	
				−55°C		340	880	

NOTES: 5. The typical values of input bias current and input offset current below 5 pA were determined mathematically.
6. This range also applies to each input individually.

electrical characteristics at specified free-air temperature, V_{DD} = 10 V (unless otherwise noted)

PARAMETER			TEST CONDITIONS		M- SUFFIX TYPES MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage	TLC27M2M	V_O = 1.4 V, V_{IC} = 0 V, R_S = 50 Ω, R_L = 100 kΩ	25°C		1.1	10	mV
				Full range			12	
		TLC27M7M	V_O = 1.4 V, V_{IC} = 0 V, R_S = 50 Ω, R_L = 100 kΩ	25°C		190	800	μV
				Full range			4300	
α_{VIO}	Average temperature coefficient of input offset voltage			25°C to 125°C		2.1		μV/°C
I_{IO}	Input offset current (see Note 5)		V_{IC} = 5 V, V_O = 5 V	25°C		0.1		pA
				125°C		1.8	15	nA
I_{IB}	Input bias current (see Note 5)		V_{IC} = 5 V, V_O = 5 V	25°C		0.7		pA
				125°C		10	35	nA
V_{ICR}	Common-mode input voltage range (see Note 6)			25°C	0 to 9	−0.3 to 9.2		V
				Full range	0 to 8.5			V
V_{OH}	High-level output voltage		V_{ID} = 100 mV, R_L = 100 kΩ	25°C	8	8.7		V
				125°C	7.8	8.8		
				−55°C	7.8	8.6		
V_{OL}	Low-level output voltage		V_{ID} = −100 mV, I_{OL} = 0	25°C		0	50	mV
				125°C		0	50	
				−55°C		0	50	
A_{VD}	Large-signal differential voltage amplification		V_O = 1 V to 6 V, R_L = 100 kΩ	25°C	25	275		V/mV
				125°C	15	190		
				−55°C	15	420		
CMRR	Common-mode rejection ratio		V_{IC} = V_{ICR} min	25°C	65	94		dB
				125°C	60	93		
				−55°C	60	93		
k_{SVR}	Supply-voltage rejection ratio (ΔV_{DD} / ΔV_{IO})		V_{DD} = 5 V to 10 V, V_O = 1.4 V	25°C	70	93		dB
				125°C	60	94		
				−55°C	60	91		
I_{DD}	Supply current (two amplifiers)		No load, V_O = 5 V, V_{IC} = 5 V	25°C		285	600	μA
				125°C		180	480	
				−55°C		490	1000	

NOTES: 5. The typical values of input bias current and input offset current below 5 pA were determined mathematically.
6. This range also applies to each input individually.

operating characteristics, V_{DD} = 5 V

PARAMETER		TEST CONDITIONS			C- SUFFIX TYPES MIN	C- SUFFIX TYPES TYP	C- SUFFIX TYPES MAX	UNIT
SR	Slew rate at unity gain	R_L = 100 kΩ, C_L = 20 pF, See Figure 1	V_{IPP} = 1 V	25°C		0.43		V/μs
				70°C		0.36		
				0°C		0.46		
			V_{IPP} = 2.5 V	25°C		0.40		
				70°C		0.34		
				0°C		0.43		
V_n	Equivalent input noise voltage	f = 1 kHz, R_S = 100 Ω, See Figure 2		25°C		32		nV/√Hz
B_{OM}	Maximum output swing bandwidth	V_O = V_{OH}, C_L = 20 pF, R_L = 100 kΩ, See Figure 1		25°C		55		kHz
				70°C		50		
				0°C		60		
B_1	Unity-gain bandwidth	V_i = 10 mV, C_L = 20 pF, See Figure 3		25°C		525		kHz
				70°C		400		
				0°C		600		
ϕ_m	Phase margin	f = B_1, V_i = 10 mV, C_L = 20 pF, See Figure 3		25°C		40°		
				70°C		39°		
				0°C		41°		

operating characteristics, V_{DD} = 10 V

PARAMETER		TEST CONDITIONS			C- SUFFIX TYPES MIN	C- SUFFIX TYPES TYP	C- SUFFIX TYPES MAX	UNIT
SR	Slew rate at unity gain	R_L = 100 kΩ, C_L = 20 pF, See Figure 1	V_{IPP} = 1 V	25°C		0.62		V/μs
				70°C		0.51		
				0°C		0.67		
			V_{IPP} = 5.5 V	25°C		0.56		
				70°C		0.46		
				0°C		0.61		
V_n	Equivalent input noise voltage	f = 1 kHz, R_S = 100 Ω, See Figure 2		25°C		32		nV/√Hz
B_{OM}	Maximum output swing bandwidth	V_O = V_{OH}, C_L = 20 pF, R_L = 100 kΩ, See Figure 1		25°C		35		kHz
				70°C		30		
				0°C		40		
B_1	Unity-gain bandwidth	V_i = 10 mV, C_L = 20 pF, See Figure 3		25°C		635		kHz
				70°C		510		
				0°C		710		
ϕ_m	Phase margin	f = B_1, V_i = 10 mV, C_L = 20 pF, See Figure 3		25°C		43°		
				70°C		42°		
				0°C		44°		

operating characteristics, V_{DD} = 5 V

PARAMETER		TEST CONDITIONS			I-SUFFIX TYPES MIN	TYP	MAX	UNIT
SR	Slew rate at unity gain	R_L = 100 kΩ, C_L = 20 pF, See Figure 1	V_{IPP} = 1 V	25°C		0.43		V/μs
				85°C		0.35		
				−40°C		0.51		
			V_{IPP} = 2.5 V	25°C		0.40		
				85°C		0.32		
				−40°C		0.48		
V_n	Equivalent input noise voltage	f = 1 kHz, R_S = 100 Ω, See Figure 2		25°C		32		nV/√Hz
B_{OM}	Maximum output swing bandwidth	V_O = V_{OH}, C_L = 20 pF, R_L = 100 kΩ, See Figure 1		25°C		55		kHz
				85°C		45		
				−40°C		75		
B_1	Unity-gain bandwidth	V_i = 10 mV, C_L = 20 pF, See Figure 3		25°C		525		kHz
				85°C		370		
				−40°C		770		
ϕ_m	Phase margin	f = B_1, V_i = 10 mV, C_L = 20 pF, See Figure 3		25°C		40°		
				85°C		38°		
				−40°C		43°		

operating characteristics, V_{DD} = 10 V

PARAMETER		TEST CONDITIONS			I-SUFFIX TYPES MIN	TYP	MAX	UNIT
SR	Slew rate at unity gain	R_L = 100 kΩ, C_L = 20 pF, See Figure 1	V_{IPP} = 1 V	25°C		0.62		V/μs
				85°C		0.47		
				−40°C		0.77		
			V_{IPP} = 5.5 V	25°C		0.56		
				85°C		0.44		
				−40°C		0.70		
V_n	Equivalent input noise voltage	f = 1 kHz, R_S = 100 Ω, See Figure 2		25°C		32		nV/√Hz
B_{OM}	Maximum output swing bandwidth	V_O = V_{OH}, C_L = 20 pF, R_L = 100 kΩ, See Figure 1		25°C		35		kHz
				85°C		25		
				−40°C		45		
B_1	Unity-gain bandwidth	V_i = 10 mV, C_L = 20 pF, See Figure 3		25°C		635		kHz
				85°C		480		
				−40°C		880		
ϕ_m	Phase margin	f = B_1, V_i = 10 mV, C_L = 20 pF, See Figure 3		25°C		43°		
				85°C		41°		
				−40°C		46°		

operating characteristics, V_{DD} = 5 V

PARAMETER		TEST CONDITIONS			M- SUFFIX TYPES MIN	TYP	MAX	UNIT
SR	Slew rate at unity gain	R_L = 100 kΩ, C_L = 20 pF, See Figure 1	V_{IPP} = 1 V	25°C		0.43		V/μs
				125°C		0.29		
				– 55°C		0.54		
			V_{IPP} = 2.5 V	25°C		0.40		
				125°C		0.28		
				– 55°C		0.50		
V_n	Equivalent input noise voltage	f = 1 kHz, R_S = 100 Ω, See Figure 2		25°C		32		nV/√Hz
B_{OM}	Maximum output swing bandwidth	V_O = V_{OH}, C_L = 20 pF, R_L = 100 kΩ, See Figure 1		25°C		55		kHz
				125°C		40		
				– 55°C		80		
B_1	Unity-gain bandwidth	V_i = 10 mV, C_L = 20 pF, See Figure 3		25°C		525		kHz
				125°C		330		
				– 55°C		850		
ϕ_m	Phase margin	f = B_1, V_i = 10 mV, C_L = 20 pF, See Figure 3		25°C		40°		
				125°C		36°		
				– 55°C		44°		

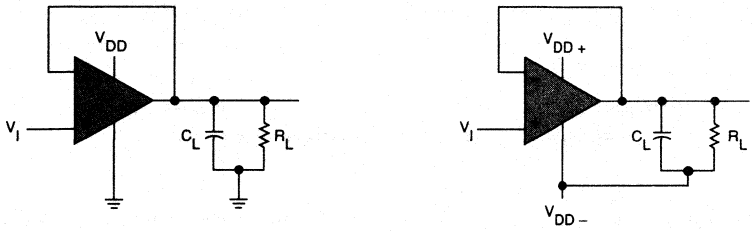
operating characteristics, V_{DD} = 10 V

PARAMETER		TEST CONDITIONS			M- SUFFIX TYPES MIN	TYP	MAX	UNIT
SR	Slew rate at unity gain	R_L = 100 kΩ, C_L = 20 pF, See Figure 1	V_{IPP} = 1 V	25°C		0.62		V/μs
				125°C		0.38		
				– 55°C		0.81		
			V_{IPP} = 5.5 V	25°C		0.56		
				125°C		0.35		
				– 55°C		0.73		
V_n	Equivalent input noise voltage	f = 1 kHz, R_S = 100 Ω, See Figure 2		25°C		32		nV/√Hz
B_{OM}	Maximum output swing bandwidth	V_O = V_{OH}, C_L = 20 pF, R_L = 100 kΩ, See Figure 1		25°C		35		kHz
				125°C		20		
				– 55°C		50		
B_1	Unity-gain bandwidth	V_i = 10 mV, C_L = 20 pF, See Figure 3		25°C		635		kHz
				125°C		440		
				– 55°C		960		
ϕ_m	Phase margin	f = B_1, V_i = 10 mV, C_L = 20 pF, See Figure 3		25°C		43°		
				125°C		39°		
				– 55°C		47°		

PARAMETER MEASUREMENT INFORMATION

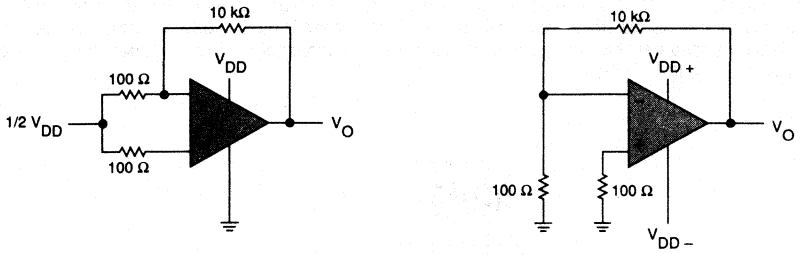
single-supply versus split-supply test circuits

Because the TLC27M2 and TLC27M7 are optimized for single-supply operation, circuit configurations used for the various tests often present some inconvenience since the input signal, in many cases, must be offset from ground. This inconvenience can be avoided by testing the device with split supplies and the output load tied to the negative rail. A comparison of single-supply versus split-supply test circuits is shown below. The use of either circuit will give the same result.



(a) Single-Supply (b) Split-Supply

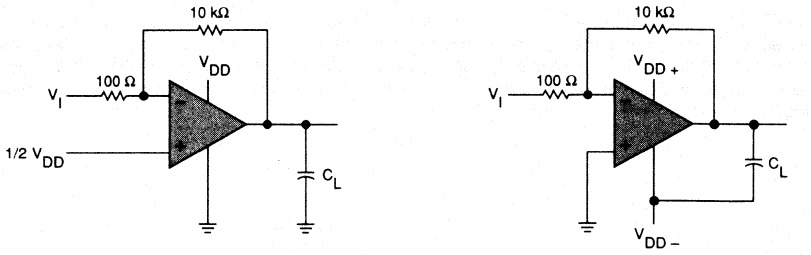
FIGURE 1. UNITY-GAIN AMPLIFIER



(a) Single-Supply (b) Split-Supply

FIGURE 2. NOISE TEST CIRCUIT

PARAMETER MEASUREMENT INFORMATION



(a) Single-Supply (b) Split-Supply

FIGURE 3. GAIN-OF-100 INVERTING AMPLIFIER

input bias current

Because of the high input impedance of the TLC27M2 and TLC27M7 op amps, attempts to measure the input bias current can result in erroneous readings. The bias current at normal room ambient temperature is typically less than 1 pA, a value that is easily exceeded by leakages on the test socket. Two suggestions are offered to avoid erroneous measurements:

1 Isolate the device from other potential leakage sources. Use a grounded shield around and between the device inputs (see Figure 4). Leakages that would otherwise flow to the inputs will be shunted away.

2 Compensate for the leakage of the test socket by actually performing an input bias current test (using a picoammeter) with no device in the test socket. The actual input bias current can then be calculated by subtracting the "open-socket" leakage readings from the readings obtained with a device in the test socket.

One word of caution . . . many automatic testers as well as some bench-top op amp testers use the servo-loop technique with a resistor in series with the device input to measure the input bias current (the voltage drop across the series resistor is measured and the bias current is calculated). This method requires that a device be inserted into the test socket to obtain a correct reading; therefore, an "open-socket" reading is not feasible using this method.

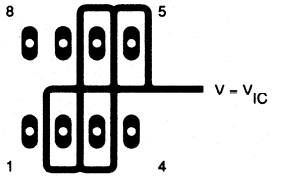


FIGURE 4. ISOLATION METAL AROUND DEVICE INPUTS (JG AND P DUAL-IN-LINE PACKAGE)

PARAMETER MEASUREMENT INFORMATION

low-level output voltage

To obtain low-supply-voltage operation, some compromise was necessary in the input stage. This compromise results in the device low-level output being dependent on both the common-mode input voltage level as well as the differential input voltage level. When attempting to correlate low-level output readings with those quoted in the electrical specifications, these two conditions should be observed. If conditions other than these are to be used, please refer to Figures 14 thru 19 in the Typical Characteristics section of this data sheet.

input offset voltage temperature coefficient

Erroneous readings often result from attempts to measure temperature coefficient of input offset voltage. This parameter is actually a calculation using input offset voltage measurements obtained at two different temperatures. When one (or both) of the temperatures is below freezing, moisture can collect on both the device and the test socket. This moisture will result in leakage and contact resistance which can cause erroneous input offset voltage readings. The isolation techniques previously mentioned have no affect on the leakage since the moisture also covers the isolation metal itself, thereby rendering it useless. It is suggested that these measurements be performed at temperatures above freezing to minimize error.

full power response

Full power response, the frequency above which the op amp slew rate limits the output voltage swing, is often specified two ways . . . full-linear response and full-peak response. The full-linear response is generally measured by monitoring the distortion level of the output while increasing the frequency of a sinusoidal input signal until the maximum frequency is found above which the output contains significant distortion. The full-peak response is defined as the maximum output frequency, without regard to distortion, above which full peak-to-peak output swing cannot be maintained.

Because there is no industry-wide accepted value for "significant" distortion, the full-peak response is specified in this data sheet and is measured using the circuit of Figure 1. The initial setup involves the use of a sinusoidal input to determine the maximum peak-to-peak output of the device (the amplitude of the sinusoidal wave is increased until clipping occurs). The sinusoidal wave is then replaced with a square wave of the same amplitude. The frequency is then increased until the maximum peak-to-peak output can no longer be maintained (Figure 5). A square wave is used to allow a more accurate determination of the point at which the maximum peak-to-peak output is reached.

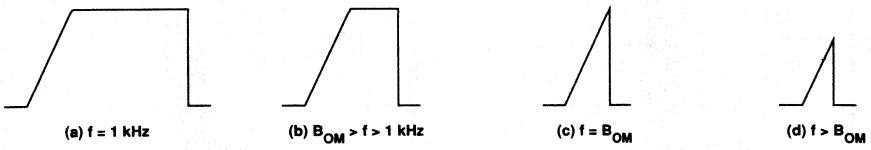


FIGURE 5. FULL-POWER-RESPONSE OUTPUT SIGNAL

test time

Inadequate test time is a frequent problem, especially when testing CMOS devices in a high-volume, short-test-time environment. Internal capacitances are inherently higher in CMOS than in bipolar and BiFET devices, and require longer test times than their bipolar and BiFET counterparts. The problem becomes more pronounced with reduced supply levels and lower temperatures.

TYPICAL CHARACTERISTICS

DISTRIBUTION OF TLC27M2
INPUT OFFSET VOLTAGE

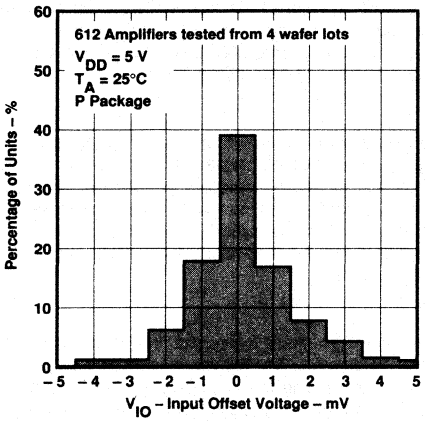


FIGURE 6

DISTRIBUTION OF TLC27M2
INPUT OFFSET VOLTAGE

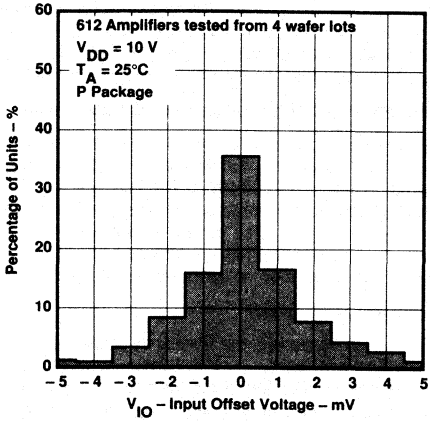


FIGURE 7

DISTRIBUTION OF TLC27M2 AND TLC27M7
INPUT OFFSET VOLTAGE
TEMPERATURE COEFFICIENT

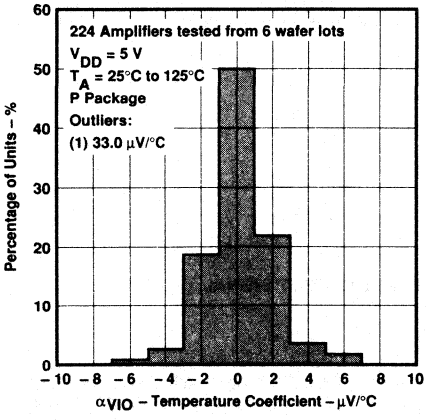


FIGURE 8

DISTRIBUTION OF TLC27M2 AND TLC27M7
INPUT OFFSET VOLTAGE
TEMPERATURE COEFFICIENT

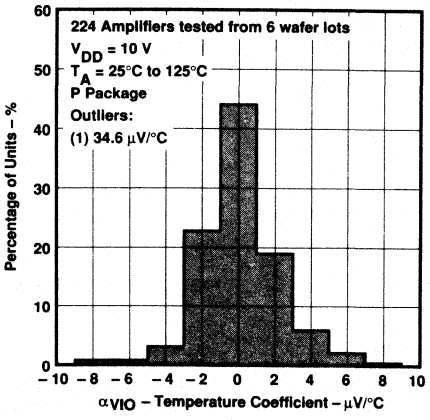


FIGURE 9

TYPICAL CHARACTERISTICS

HIGH-LEVEL OUTPUT VOLTAGE
vs
HIGH-LEVEL OUTPUT CURRENT

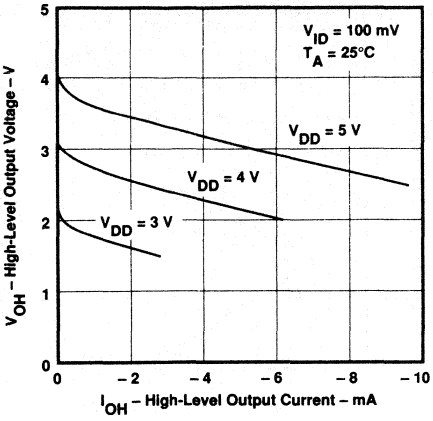


FIGURE 10

HIGH-LEVEL OUTPUT VOLTAGE
vs
HIGH-LEVEL OUTPUT CURRENT

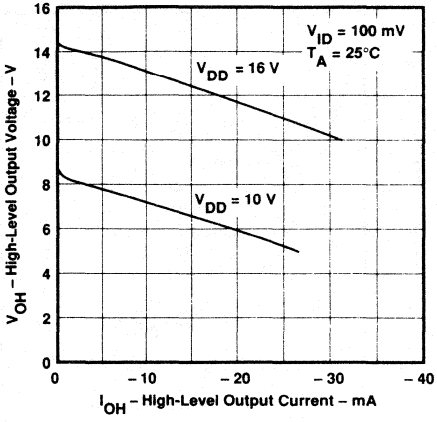


FIGURE 11

HIGH-LEVEL OUTPUT VOLTAGE
vs
SUPPLY VOLTAGE

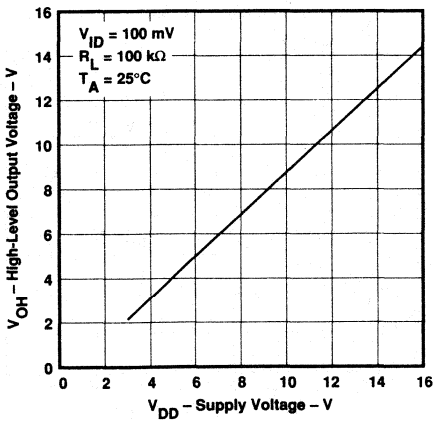


FIGURE 12

HIGH-LEVEL OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE

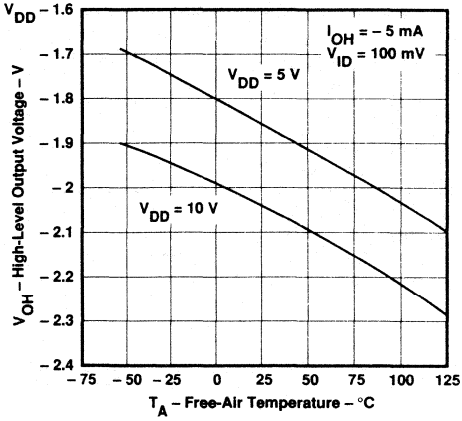


FIGURE 13

TYPICAL CHARACTERISTICS

LOW-LEVEL OUTPUT VOLTAGE
vs
COMMON-MODE INPUT VOLTAGE

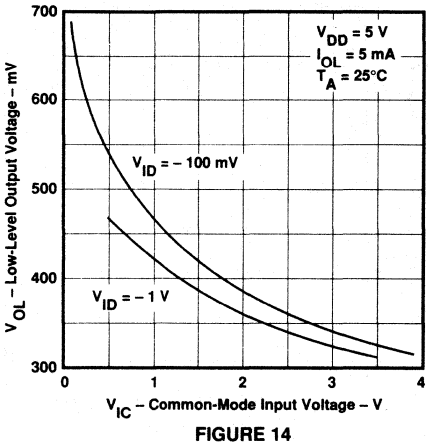


FIGURE 14

LOW-LEVEL OUTPUT VOLTAGE
vs
COMMON-MODE INPUT VOLTAGE

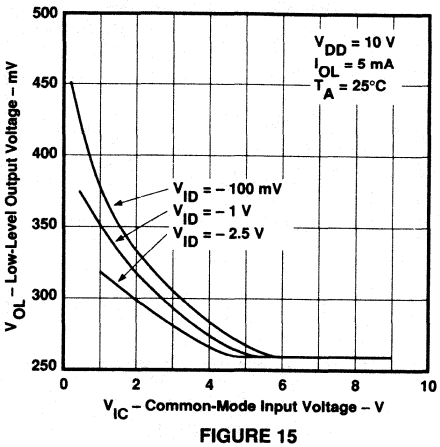


FIGURE 15

LOW-LEVEL OUTPUT VOLTAGE
vs
DIFFERENTIAL INPUT VOLTAGE

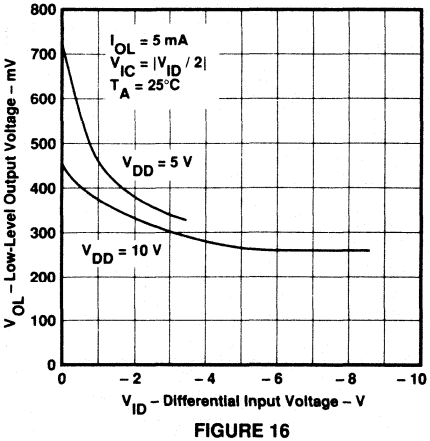


FIGURE 16

LOW-LEVEL OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE

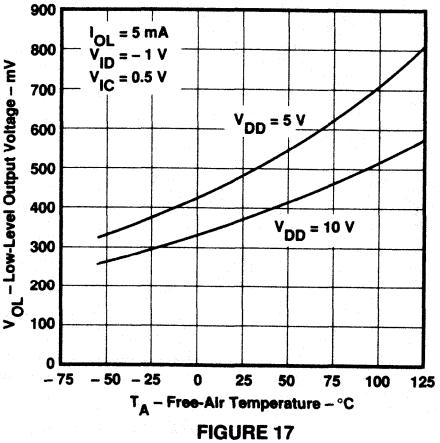


FIGURE 17

TYPICAL CHARACTERISTICS

LOW-LEVEL OUTPUT VOLTAGE
vs
LOW-LEVEL OUTPUT CURRENT

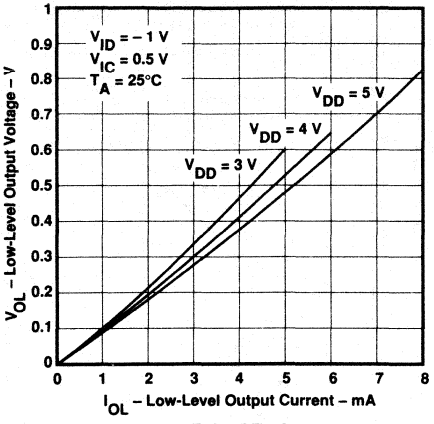


FIGURE 18

LOW-LEVEL OUTPUT VOLTAGE
vs
LOW-LEVEL OUTPUT CURRENT

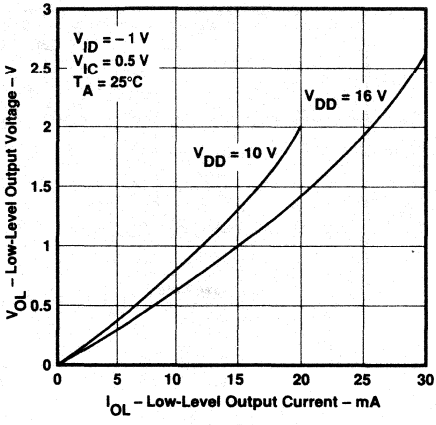


FIGURE 19

LARGE-SIGNAL
DIFFERENTIAL VOLTAGE AMPLIFICATION
vs
SUPPLY VOLTAGE

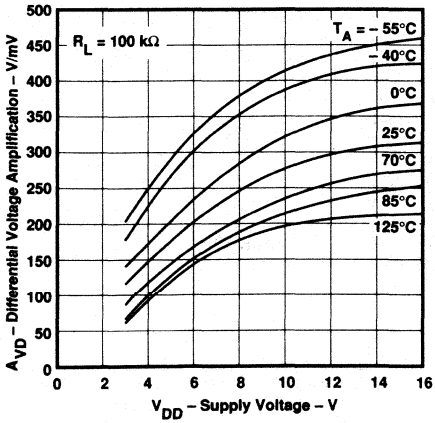


FIGURE 20

LARGE-SIGNAL
DIFFERENTIAL VOLTAGE AMPLIFICATION
vs
FREE-AIR TEMPERATURE

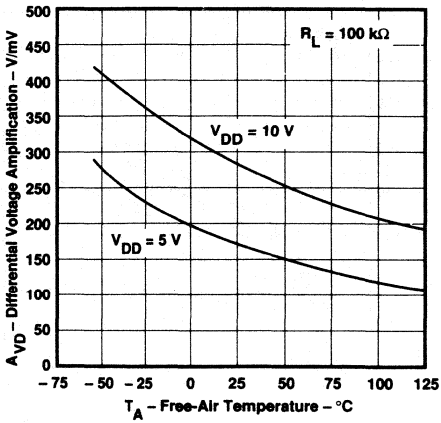


FIGURE 21

TYPICAL CHARACTERISTICS

INPUT BIAS CURRENT AND INPUT OFFSET CURRENT
vs
FREE-AIR TEMPERATURE

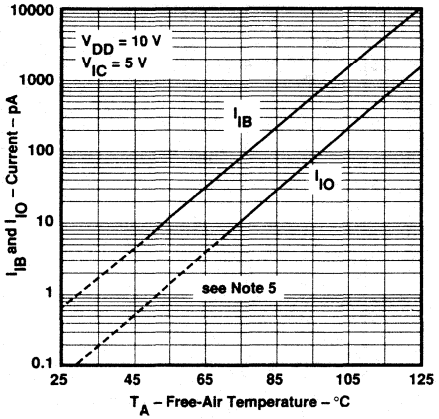


FIGURE 22

MAXIMUM INPUT VOLTAGE
vs
SUPPLY VOLTAGE

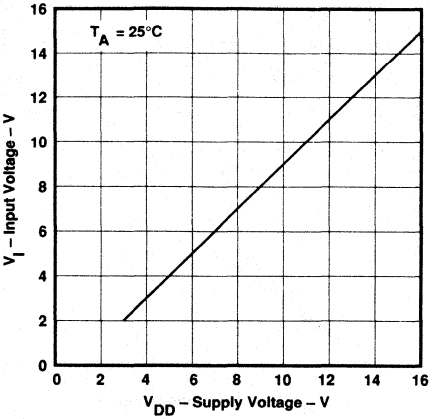


FIGURE 23

SUPPLY CURRENT
vs
SUPPLY VOLTAGE

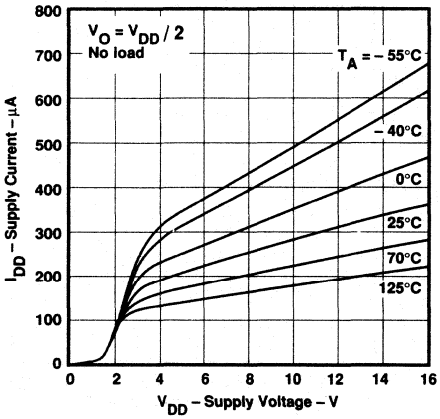


FIGURE 24

SUPPLY CURRENT
vs
FREE-AIR TEMPERATURE

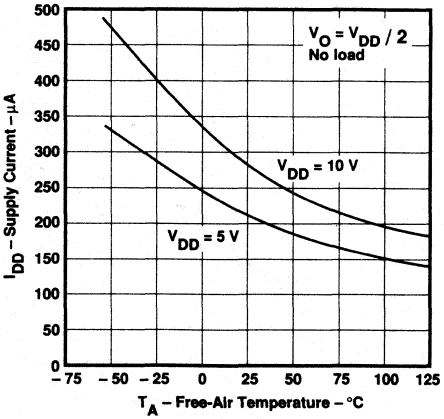


FIGURE 25

NOTE 5: The typical values of input bias current and input offset current below 5 pA were determined mathematically.

TYPICAL CHARACTERISTICS

SLEW RATE
vs
SUPPLY VOLTAGE

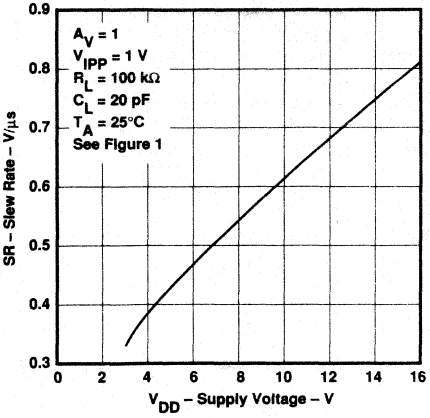


FIGURE 26

SLEW RATE
vs
FREE-AIR TEMPERATURE

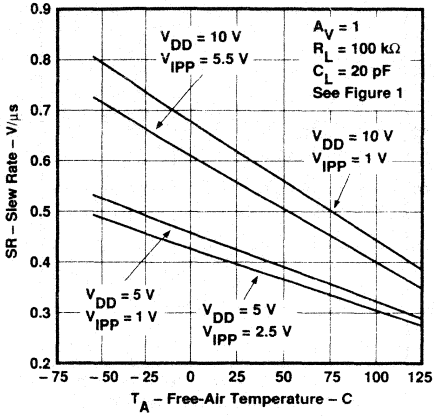


FIGURE 27

NORMALIZED SLEW RATE
vs
FREE-AIR TEMPERATURE

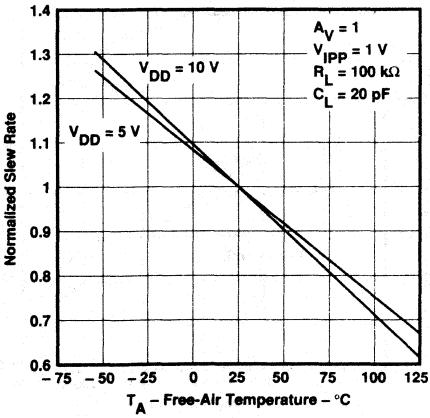


FIGURE 28

MAXIMUM PEAK-TO-PEAK OUTPUT VOLTAGE
vs
FREQUENCY

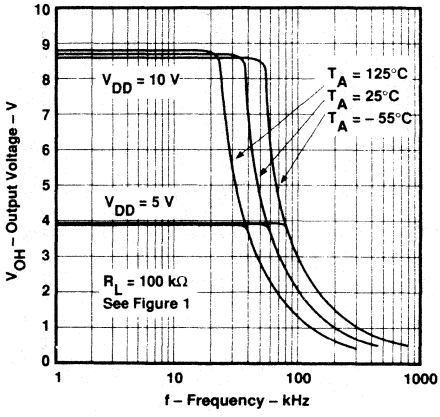


FIGURE 29

TYPICAL CHARACTERISTICS

UNITY-GAIN BANDWIDTH
vs
FREE-AIR TEMPERATURE

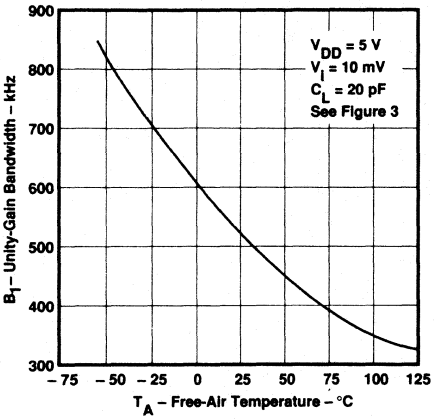


FIGURE 30

UNITY-GAIN BANDWIDTH
vs
SUPPLY VOLTAGE

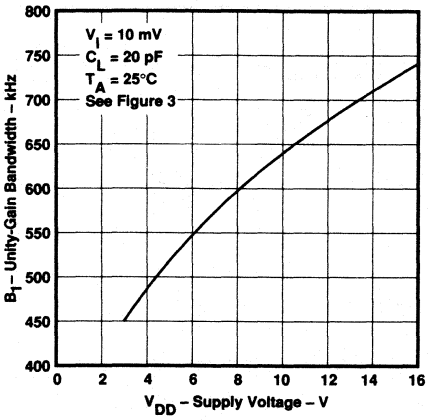


FIGURE 31

LARGE-SIGNAL DIFFERENTIAL VOLTAGE
AMPLIFICATION AND PHASE SHIFT
vs
FREQUENCY

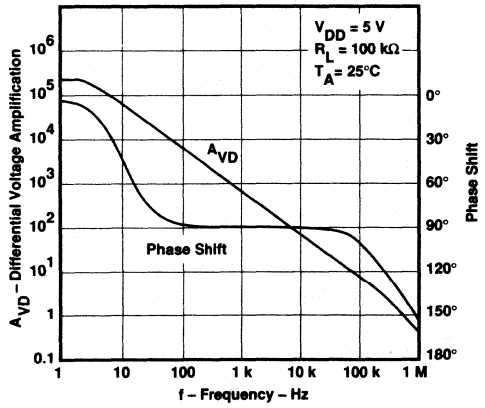


FIGURE 32

LARGE-SIGNAL DIFFERENTIAL VOLTAGE
AMPLIFICATION AND PHASE SHIFT
vs
FREQUENCY

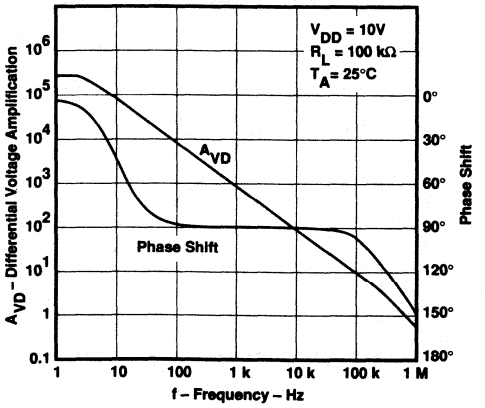


FIGURE 33

TYPICAL CHARACTERISTICS

PHASE MARGIN
vs
SUPPLY VOLTAGE

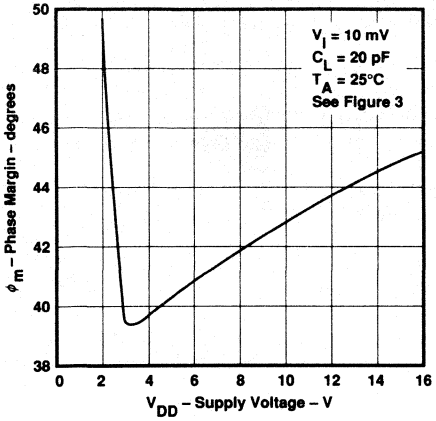


FIGURE 34

PHASE MARGIN
vs
FREE-AIR TEMPERATURE

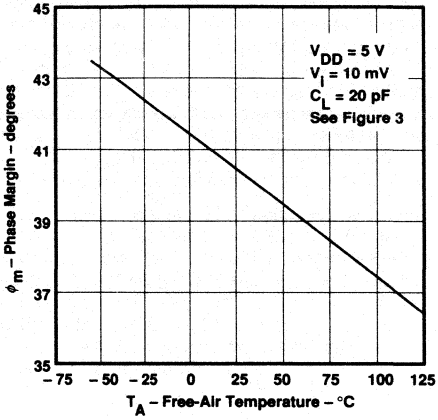


FIGURE 35

PHASE MARGIN
vs
CAPACITIVE LOAD

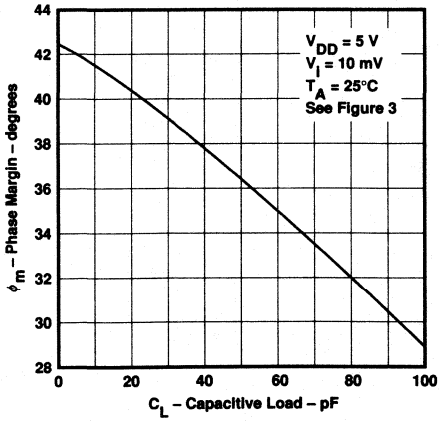


FIGURE 36

EQUIVALENT INPUT NOISE VOLTAGE
vs
FREQUENCY

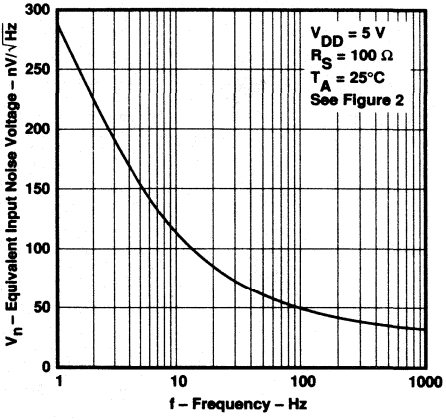


FIGURE 37

TYPICAL APPLICATION DATA

single-supply operation

While the TLC27M2 and TLC27M7 will perform well using dual power supplies (also called balanced or split supplies), the design is optimized for single-supply operation. This includes an input common mode voltage range that encompasses ground as well as an output voltage range that pulls down to ground. The supply voltage range extends down to 3 V (C- suffix types), thus allowing operation with supply levels commonly available for TTL and HCMOS; however, for maximum dynamic range, 16-V single-supply operation is recommended.

Many single-supply applications require that a voltage be applied to one input to establish a reference level that is above ground. A resistive voltage divider is usually sufficient to establish this reference level (see Figure 38). The low input bias current consumption of the TLC27M2 and TLC27M7 permits the use of very large resistive values to implement the voltage divider, thus minimizing power consumption.

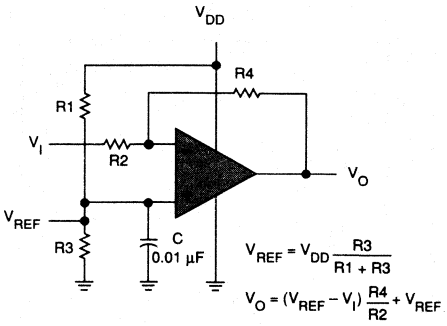
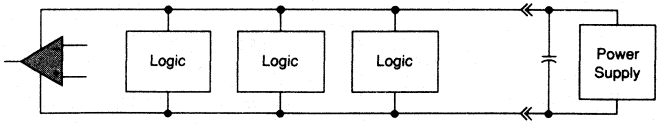


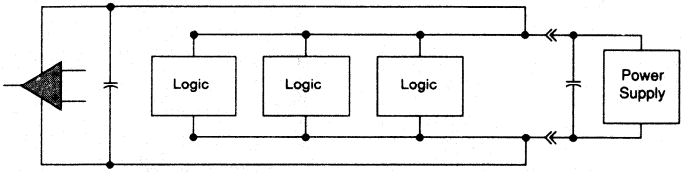
FIGURE 38. INVERTING AMPLIFIER WITH VOLTAGE REFERENCE

The TLC27M2 and TLC27M7 work well in conjunction with digital logic; however, when powering both linear devices and digital logic from the same power supply, the following precautions are recommended:

1. Power the linear devices from separate bypassed supply lines (see Figure 39); otherwise the linear device supply rails can fluctuate due to voltage drops caused by high switching currents in the digital logic.
2. Use proper bypass techniques to reduce the probability of noise-induced errors. Single capacitive decoupling is often adequate; however, RC decoupling may be necessary in high-frequency applications.



(a) Common Supply Rails



(b) Separate Bypassed Supply Rails (preferred)

FIGURE 39. COMMON VERSUS SEPARATE SUPPLY RAILS

TYPICAL APPLICATION DATA

input characteristics

The TLC27M2 and TLC27M7 are specified with a minimum and a maximum input voltage that, if exceeded at either input, could cause the device to malfunction. Exceeding this specified range is a common problem, especially in single-supply operation. Note that the lower range limit includes the negative rail, while the upper range limit is specified at V_{DD} – 1 V at T_A = 25°C and at V_{DD} – 1.5 V at all other temperatures.

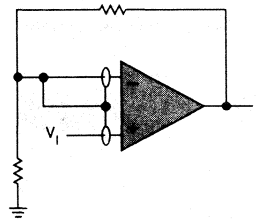
The use of the polysilicon-gate process and the careful input circuit design gives the TLC27M2 and TLC27M7 very good input offset voltage drift characteristics relative to conventional metal-gate processes. Offset voltage drift in CMOS devices is highly influenced by threshold voltage shifts caused by polarization of the phosphorus dopant implanted in the oxide. Placing the phosphorus dopant in a conductor (such as a polysilicon gate) alleviates the polarization problem, thus reducing threshold voltage shifts by more than an order of magnitude. The offset voltage drift with time has been calculated to be typically 0.1 μV/month, including the first month of operation.

Because of the extremely high input impedance and resulting low bias current requirements, the TLC27M2 and TLC27M7 are well suited for low-level signal processing; however, leakage currents on printed circuit boards and sockets can easily exceed bias current requirements and cause a degradation in device performance. It is good practice to include guard rings around inputs (similar to those of Figure 4 in the PARAMETER MEASUREMENT INFORMATION section). These guards should be driven from a low-impedance source at the same voltage level as the common-mode input (see Figure 40).

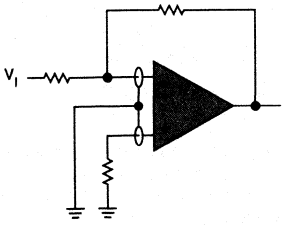
The inputs of any unused amplifiers should be tied to ground to avoid possible oscillation.

noise performance

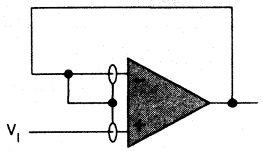
The noise specifications in op amp circuits are greatly dependent on the current in the first-stage differential amplifier. The low input bias current requirements of the TLC27M2 and TLC27M7 result in a very low noise current, which is insignificant in most applications. This feature makes the devices especially favorable over bipolar devices when using values of circuit impedance greater than 50 kΩ, since bipolar devices exhibit greater noise currents.



(a) Noninverting Amplifier



(b) Inverting Amplifier



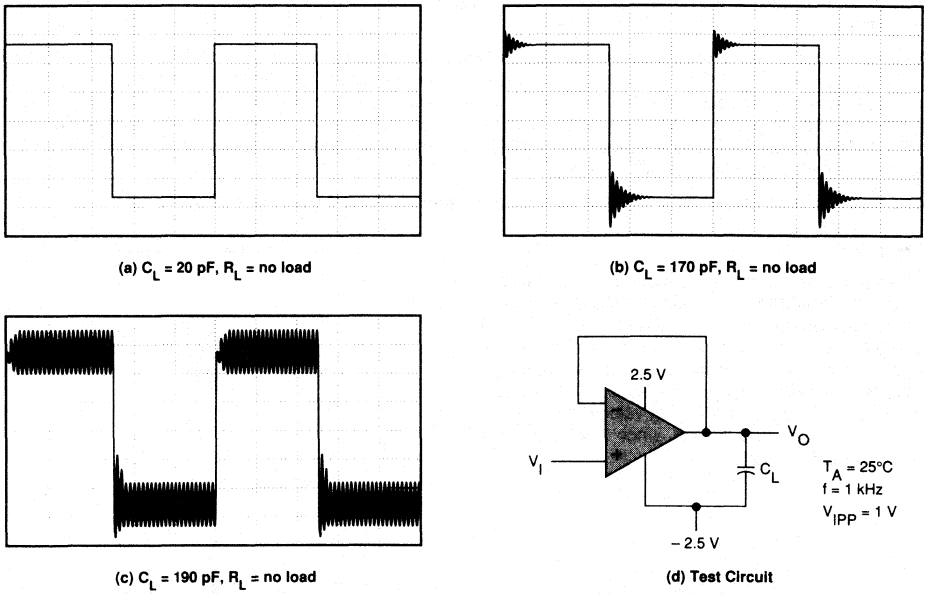
(c) Unity Gain Amplifier

Figure 40. GUARD RING SCHEMES

output characteristics

The output stage of the TLC27M2 and TLC27M7 is designed to sink and source relatively high amounts of current (see typical characteristics). If the output is subjected to a short-circuit condition, this high current capability can cause device damage under certain conditions. Output current capability increases with supply voltage.

All operating characteristics of the TLC27M2 and TLC27M7 were measured using a 20-pF load. The devices will drive higher capacitive loads; however, as output load capacitance increases, the resulting response pole occurs at lower frequencies, thereby causing ringing, peaking, or even oscillation (see Figure 41). In many cases, adding some compensation in the form of a series resistor in the feedback loop will alleviate the problem.



(a) C_L = 20 pF, R_L = no load

(b) C_L = 170 pF, R_L = no load

(c) C_L = 190 pF, R_L = no load

(d) Test Circuit

FIGURE 41. EFFECT OF CAPACITIVE LOADS AND TEST CIRCUIT

Although the TLC27M2 and TLC27M7 possess excellent high-level output voltage and current capability, methods are available for boosting this capability, if needed. The simplest method involves the use of a pull-up resistor (R_P) connected from the output to the positive supply rail. There are two disadvantages to the use of this circuit. First, the NMOS pull-down transistor, N4 (see Figure 42) must sink a comparatively large amount of current. In this circuit, N4 behaves like a linear resistor with an on resistance between approximately 60 Ω and 180 Ω, depending on how hard the op amp input is driven. With very low values of R_P, a voltage offset from 0 V at the output will occur. Secondly, pull-up resistor R_P acts as a drain load to N4 and the gain of the op amp is reduced at output voltage levels where N5 is not supplying the output current.

TYPICAL APPLICATION DATA

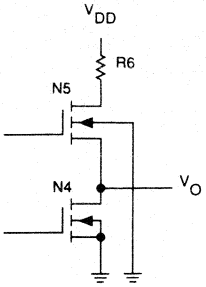


FIGURE 42. TLC27M2 / TLC27M7 OUTPUT STAGE

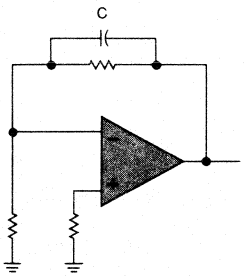


FIGURE 43. COMPENSATION FOR INPUT CAPACITANCE

feedback

Op amp circuits nearly always employ feedback, and since feedback is the first prerequisite for oscillation, a little caution is appropriate. Most oscillation problems result from driving capacitive loads (discussed previously) and ignoring stray input capacitance. A small-value capacitor connected in parallel with the feedback resistor is an effective remedy (see Figure 43). The value of this capacitor is optimized empirically.

electrostatic discharge protection

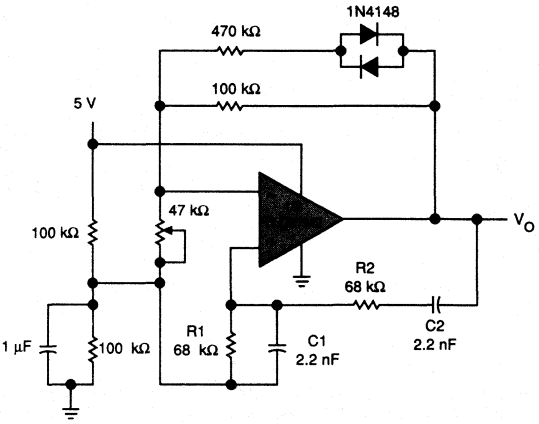
The TLC27M2 and TLC27M7 incorporate an internal electrostatic discharge (ESD) protection circuit that will prevent functional failures at voltages up to 2000 V as tested under MIL-STD-883C, Method 3015.2. Care should be exercised, however, when handling these devices as exposure to ESD may result in the degradation of the device parametric performance. The protect circuit also causes the input bias currents to be temperature dependent and have the characteristics of a reverse-biased diode.

latchup

Because CMOS devices are susceptible to latchup due to their inherent parasitic thyristors, the TLC27M2 and TLC27M7 inputs and outputs were designed to withstand −100-mA surge currents without sustaining latchup; however, techniques should be used to reduce the chance of latchup whenever possible. Internal protection diodes should not by design be forward biased. Applied input and output voltage should not exceed the supply voltage by more than 300 mV. Care should be exercised when using capacitive coupling on pulse generators. Supply transients should be shunted by the use of decoupling capacitors (0.1 μF typical) located across the supply rails as close to the device as possible.

The current path established if latchup occurs is usually between the positive supply rail and ground and can be triggered by surges on the supply lines and / or voltages on either the output or inputs that exceed the supply voltage. Once latchup occurs, the current flow is limited only by the impedance of the power supply and the forward resistance of the parasitic thyristor and usually results in the destruction of the device. The chance of latchup occurring increases with increasing temperature and supply voltages.

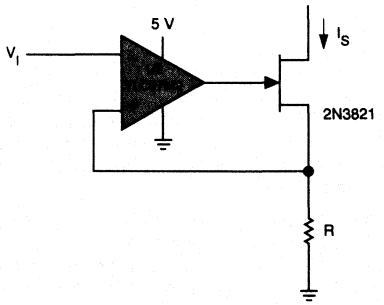
TYPICAL APPLICATION DATA



NOTES: $V_{OPP} \approx 2$ V

$$f_O = \frac{1}{2\pi\sqrt{R1R2C1C2}}$$

FIGURE 44. WIEN OSCILLATOR

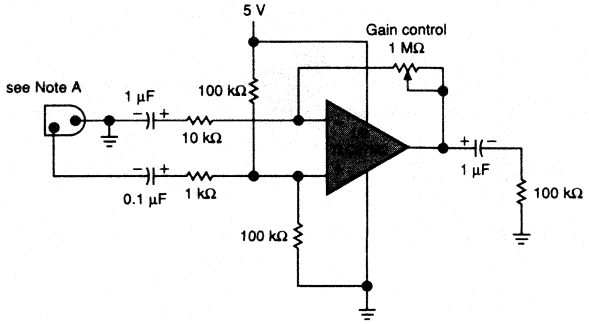


NOTES: $V_I = 0$ V TO 3 V

$$I_S = \frac{V_I}{R}$$

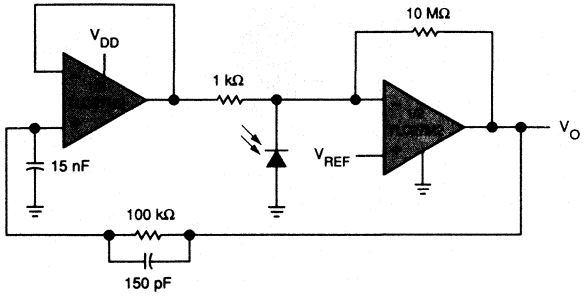
FIGURE 45. PRECISION LOW CURRENT SINK

TYPICAL APPLICATION DATA



NOTE A: Low to medium impedance dynamic mike

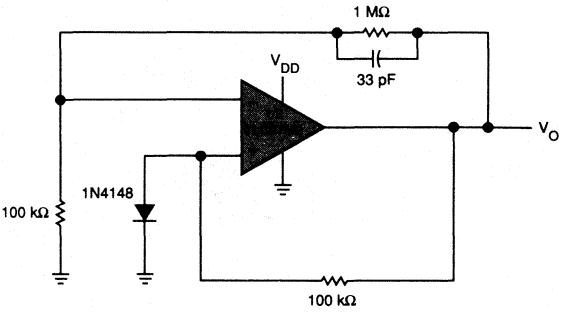
FIGURE 46. MICROPHONE PREAMPLIFIER



NOTES: V_{DD} = 4 V to 15 V
V_{REF} = 0 V to V_{DD} − 2 V

FIGURE 47. PHOTO DIODE AMPLIFIER WITH AMBIENT LIGHT REJECTION

TYPICAL APPLICATION DATA



NOTES: V_{DD} = 8 V to 16 V
V_O = 5 V, 10 mA

FIGURE 48. 5 V LOW POWER VOLTAGE REGULATOR

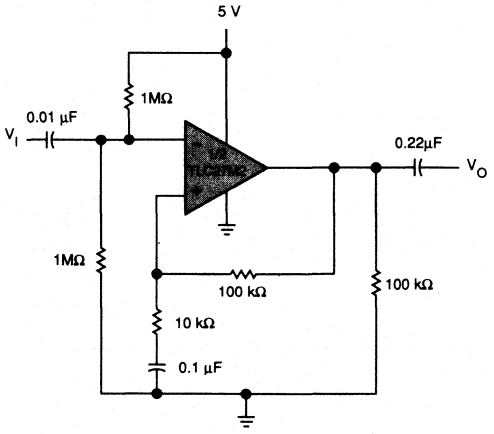


FIGURE 49. SINGLE RAIL A.C. AMPLIFIER

OCTOBER 1987

- **Trimmed Offset Voltage:**
  TLC27L7 . . . 500 μV Max at 25°C, V_{DD} = 5 V
- **Input Offset Voltage Drift Typically**
  0.1 μV / Month, Including the First 30 Days
- **Wide Range of Supply Voltages over Specified Temperature Range:**
  – 55°C to125°C . . . 4 V to 16 V
  – 40°C to 85°C . . . 4 V to 16 V
  0°C to 70°C . . . 3 V to 16 V
- **Single-Supply Operation**
- **Common-Mode Input Voltage Range Extends Below the Negative Rail (C- suffix, I- suffix types)**
- **Ultra-Low Power . . . 95 μW Typically at 25°C, V_{DD} = 5 V**
- **Output Voltage Range Includes Negative Rail**
- **High Input Impedance . . . 10^{12} Ω Typical**
- **ESD Protection Circuitry**
- **Small-Outline Package Option Also Available in Tape-and-Reel**
- **Designed-in Latchup Immunity**

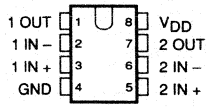
description

The TLC27L2 and TLC27L7 dual operational amplifiers combine a wide range of input offset voltage grades with low offset voltage drift, high input impedance, extremely low power, and high gain.

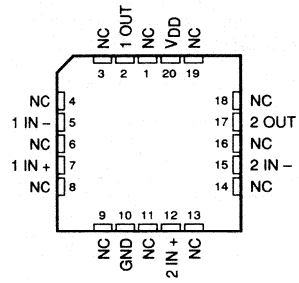
T_A	V_{IO}max at 25°C	PACKAGE			
		Small-Outline (D) See Note 1	Plastic DIP (P)	Ceramic DIP (JG)	Chip Carrier (FK)
0°C to 70°C	500 μV	TLC27L7CD	TLC27L7CP	TLC27L7CJG	—
	2 mV	TLC27L2BCD	TLC27L2BCP	TLC27L2BCJG	—
	5 mV	TLC27L2ACD	TLC27L2ACP	TLC27L2ACJG	—
	10 mV	TLC27L2CD	TLC27L2CP	TLC27L2CJG	—
– 40°C to 85°C	500 μV	TLC27L7ID	TLC27L7IP	TLC27L7IJG	—
	2 mV	TLC27L2BID	TLC27L2BIP	TLC27L2BIJG	—
	5 mV	TLC27L2AID	TLC27L2AIP	TLC27L2AIJG	—
	10 mV	TLC27L2ID	TLC27L2IP	TLC27L2IJG	—
– 55°C to 125°C	500 μV	—	—	TLC27L7MJG	TLC27L7MFK
	10 mV	—	—	TLC27L2MJG	TLC27L2MFK

NOTE 1: Available in tape-and-reel. Add "R" suffix to the device type when ordering (e.g., TLC27L7CDR).

JG AND P DUAL-IN-LINE PACKAGE
D SMALL-OUTLINE PACKAGE
(TOP VIEW)

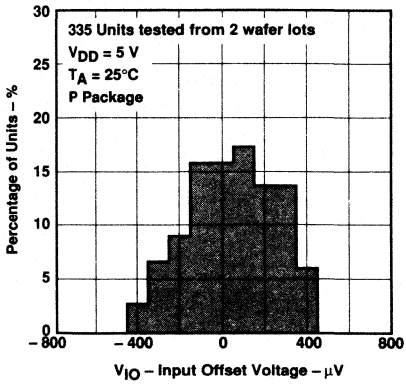


FK CHIP CARRIER PACKAGE
(TOP VIEW)



NC – No internal connection

DISTRIBUTION OF TLC27L7
INPUT OFFSET VOLTAGE



LinCMOS is a trademark of Texas Instruments Incorporated

description (continued)

These devices use Texas Instruments silicon-gate LinCMOS technology, which provides offset voltage stability far exceeding the stability available with conventional metal-gate processes.

The extremely high input impedance, low bias currents, and low power consumption make these cost-effective devices ideal for high gain, low frequency, low power applications . Four offset voltage grades are available (C- suffix and I- suffix types), ranging from the low-cost TLC27L2 (10 mV) to the high-precision TLC27L7 (500 μV). These advantages, in combination with good common-mode rejection and supply voltage rejection, make these devices a good choice for new state-of-the-art designs as well as for upgrading existing designs.

In general, many features associated with bipolar technology are available on LinCMOS operational amplifiers, without the power penalties of bipolar technology. General applications such as transducer interfacing, analog calculations, amplifier blocks, active filters, and signal buffering are all easily designed with the TLC27L2 and TLC27L7. The devices also exhibit low voltage single supply operation and ultra-low power consumption making them ideally suited for remote and inaccessible battery-powered applications. The common-mode input voltage range includes the negative rail.

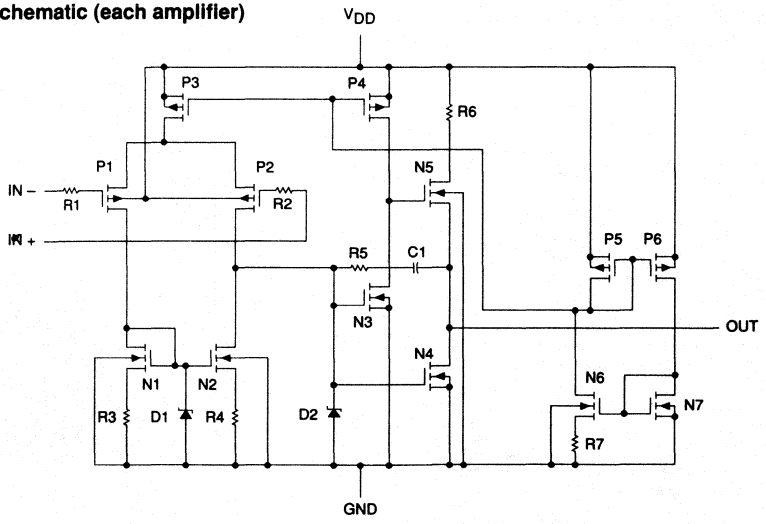
A wide range of packaging options is available, including small outline and chip carrier versions for high-density system applications.

The device inputs and outputs are designed to withstand – 100-mA surge currents without sustaining latchup.

The TLC27L2 and TLC27L7 incorporate internal ESD protection circuits that will prevent functional failures at voltages up to 2000 V as tested under MIL-STD-883C, Method 3015.2; however, care should be exercised in handling these devices as exposure to ESD may result in the degradation of the device parametric performance.

The M- suffix devices are characterized for operation over the full military temperature range of – 55°C to 125°C, the I- suffix devices from – 40°C to 85°C, and the C- suffix devices from 0°C to 70°C.

equivalent schematic (each amplifier)



absolute maximum ratings over operating free-air temperature (unless otherwise noted)

Supply voltage, V_{DD} (see Note 2) . . . . . 18 V
Differential input voltage (see Note 3) . . . . . $\pm V_{DD}$
Input voltage range, V_I (any input) . . . . . -0.3 V to V_{DD}
Input current, I_I . . . . . ± 5 mA
Output current, I_O (each output) . . . . . ± 30 mA
Total current into V_{DD} terminal . . . . . 45 mA
Total current out of ground terminal . . . . . 45 mA
Duration of short-circuit current at (or below) 25°C (see Note 4) . . . . . Unlimited
Continuous total dissipation . . . . . See Dissipation Rating Table
Operating free-air temperature, T_A: C-suffix types . . . . . 0°C to 70°C
I-suffix types . . . . . -40°C to 85°C
M-suffix types . . . . . -55°C to 125°C
Storage temperature range . . . . . -65°C to 150°C
Case temperature for 60 seconds: FK package . . . . . 260°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds: JG package . . . . . 300°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: D and P package . . . . . 260°C

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25$°C POWER RATING	DERATING FACTOR ABOVE $T_A = 25$°C	$T_A = 70$°C POWER RATING	$T_A = 85$°C POWER RATING	$T_A = 125$°C POWER RATING
D	725 mW	5.8 mW/°C	464 mW	377 mW	
FK	1375 mW	11 mW/°C	880 mW	715 mW	275 mW
JG (C-, I- suffix)	825 mW	6.6 mW/°C	528 mW	429 mW	
JG (M- suffix)	1050 mW	8.4 mW/°C	672 mW	546 mW	210 mW
P	1000 mW	8.0 mW/°C	640 mW	520 mW	

recommended operating conditions

		M- SUFFIX TYPES			I- SUFFIX TYPES			C- SUFFIX TYPES			
		MIN	NOM	MAX	MIN	NOM	MAX	MIN	NOM	MAX	UNIT
Supply voltage, V_{DD}		4		16	4		16	3		16	V
Common-mode input voltage, V_{IC}	$V_{DD} = 5$ V	0		3.5	−0.2		3.5	−0.2		3.5	V
	$V_{DD} = 10$ V	0		8.5	−0.2		8.5	−0.2		8.5	V
Input voltage, V_I	$V_{DD} = 5$ V	0		3.5	−0.2		3.5	−0.2		3.5	V
	$V_{DD} = 10$ V	0		8.5	−0.2		8.5	−0.2		8.5	V
Operating free-air temperature, T_A		−55		125	−40		85	0		70	°C

NOTES: 2. All voltage values, except differential voltages, are with respect to network ground.
3. Differential voltages are at the noninverting input with respect to the inverting input.
4. The output may be shorted to either supply. Temperature and/or supply voltages must be limited to ensure that the maximum dissipation rating is not exceeded (see application section).

electrical characteristics at specified free-air temperature, V_{DD} = 5 V (unless otherwise noted)

PARAMETER			TEST CONDITIONS		C- SUFFIX TYPES MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage	TLC27L2C	V_O = 1.4 V, V_{IC} = 0 V, R_S = 50 Ω, R_L = 1 MΩ	25°C		1.1	10	mV
				Full range			12	
		TLC27L2AC	V_O = 1.4 V, V_{IC} = 0 V, R_S = 50 Ω, R_L = 1 MΩ	25°C		0.9	5	
				Full range			6.5	
		TLC27L2BC	V_O = 1.4 V, V_{IC} = 0 V, R_S = 50 Ω, R_L = 1 MΩ	25°C		204	2000	μV
				Full range			3000	
		TLC27L7C	V_O = 1.4 V, V_{IC} = 0 V, R_S = 50 Ω, R_L = 1 MΩ	25°C		170	500	
				Full range			1500	
α_{VIO}	Average temperature coefficient of input offset voltage			25°C to 70°C		1.1		μV/°C
I_{IO}	Input offset current (see Note 5)		V_{IC} = 2.5 V, V_O = 2.5 V	25°C		0.1		pA
				70°C		7	300	
I_{IB}	Input bias current (see Note 5)		V_{IC} = 2.5 V, V_O = 2.5 V	25°C		0.6		pA
				70°C		40	600	
V_{ICR}	Common-mode input voltage range (see Note 6)			25°C	−0.2 to 4	−0.3 to 4.2		V
				Full range	−0.2 to 3.5			V
V_{OH}	High-level output voltage		V_{ID} = 100 mV, R_L = 1 MΩ	25°C	3.2	4.1		V
				70°C	3	4.2		
				0°C	3	4.1		
V_{OL}	Low-level output voltage		V_{ID} = −100 mV, I_{OL} = 0	25°C		0	50	mV
				70°C		0	50	
				0°C		0	50	
A_{VD}	Large-signal differential voltage amplification		V_O = 0.25 V to 2 V, R_L = 1 MΩ	25°C	50	480		V/mV
				70°C	50	380		
				0°C	50	700		
CMRR	Common-mode rejection ratio		V_{IC} = V_{ICR} min	25°C	65	94		dB
				70°C	60	95		
				0°C	60	95		
k_{SVR}	Supply-voltage rejection ratio (ΔV_{DD} / ΔV_{IO})		V_{DD} = 5 V to 10 V, V_O = 1.4 V	25°C	70	97		dB
				70°C	60	98		
				0°C	60	97		
I_{DD}	Supply current (two amplifiers)		No load, V_O = 2.5 V, V_{IC} = 2.5 V	25°C		19	34	μA
				70°C		15	28	
				0°C		24	42	

NOTES: 5. The typical values of input bias current and input offset current below 5 pA were determined mathematically.
6. This range also applies to each input individually.

electrical characteristics at specified free-air temperature, V_{DD} = 10 V (unless otherwise noted)

PARAMETER			TEST CONDITIONS		C- SUFFIX TYPES MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage	TLC27L2C	V_O = 1.4 V, V_{IC} = 0 V, R_S = 50 Ω, R_L = 1 MΩ	25°C		1.1	10	mV
				Full range			12	
		TLC27L2AC	V_O = 1.4 V, V_{IC} = 0 V, R_S = 50 Ω, R_L = 1 MΩ	25°C		0.9	5	
				Full range			6.5	
		TLC27L2BC	V_O = 1.4 V, V_{IC} = 0 V, R_S = 50 Ω, R_L = 1 MΩ	25°C		235	2000	μV
				Full range			3000	
		TLC27L7C	V_O = 1.4 V, V_{IC} = 0 V, R_S = 50 Ω, R_L = 1 MΩ	25°C		190	800	
				Full range			1900	
α_{VIO}	Average temperature coefficient of input offset voltage			25°C to 70°C		1		μV/°C
I_{IO}	Input offset current (see Note 5)		V_{IC} = 5 V, V_O = 5 V	25°C		0.1		pA
				70°C		8	300	
I_{IB}	Input bias current (see Note 5)		V_{IC} = 5 V, V_O = 5 V	25°C		0.7		pA
				70°C		50	600	
V_{ICR}	Common-mode input voltage range (see Note 6)			25°C	−0.2 to 9	−0.3 to 9.2		V
				Full range	−0.2 to 8.5			V
V_{OH}	High-level output voltage		V_{ID} = 100 mV, R_L = 1 MΩ	25°C	8	8.9		V
				70°C	7.8	8.9		
				0°C	7.8	8.9		
V_{OL}	Low-level output voltage		V_{ID} = −100 mV, I_{OL} = 0	25°C		0	50	mV
				70°C		0	50	
				0°C		0	50	
A_{VD}	Large-signal differential voltage amplification		V_O = 1 V to 6 V, R_L = 1 MΩ	25°C	50	800		V/mV
				70°C	50	660		
				0°C	50	1100		
CMRR	Common-mode rejection ratio		V_{IC} = V_{ICR} min	25°C	65	97		dB
				70°C	60	97		
				0°C	60	97		
k_{SVR}	Supply-voltage rejection ratio (ΔV_{DD} / ΔV_{IO})		V_{DD} = 5 V to 10 V, V_O = 1.4 V	25°C	70	97		dB
				70°C	60	98		
				0°C	60	97		
I_{DD}	Supply current (two amplifiers)		No load, V_O = 5 V, V_{IC} = 5 V	25°C		29	46	μA
				70°C		22	40	
				0°C		36	66	

NOTES: 5. The typical values of input bias current and input offset current below 5 pA were determined mathematically.
6. This range also applies to each input individually.

electrical characteristics at specified free-air temperature, V_{DD} = 5 V (unless otherwise noted)

PARAMETER			TEST CONDITIONS		I- SUFFIX TYPES MIN	I- SUFFIX TYPES TYP	I- SUFFIX TYPES MAX	UNIT
V_{IO}	Input offset voltage	TLC27L2I	V_O = 1.4 V, V_{IC} = 0 V, R_S = 50 Ω, R_L = 1 MΩ	25°C		1.1	10	mV
				Full range			13	
		TLC27L2AI	V_O = 1.4 V, V_{IC} = 0 V, R_S = 50 Ω, R_L = 1 MΩ	25°C		0.9	5	
				Full range			7	
		TLC27L2BI	V_O = 1.4 V, V_{IC} = 0 V, R_S = 50 Ω, R_L = 1 MΩ	25°C		204	2000	μV
				Full range			3500	
		TLC27L7I	V_O = 1.4 V, V_{IC} = 0 V, R_S = 50 Ω, R_L = 1 MΩ	25°C		170	500	
				Full range			2000	
α_{VIO}	Average temperature coefficient of input offset voltage			25°C to 85°C		1.1		μV/°C
I_{IO}	Input offset current (see Note 5)		V_{IC} = 2.5 V, V_O = 2.5 V	25°C		0.1		pA
				85°C		24	1000	
I_{IB}	Input bias current (see Note 5)		V_{IC} = 2.5 V, V_O = 2.5 V	25°C		0.6		pA
				85°C		200	2000	
V_{ICR}	Common-mode input voltage range (see Note 6)			25°C	−0.2 to 4	−0.3 to 4.2		V
				Full range	−0.2 to 3.5			V
V_{OH}	High-level output voltage		V_{ID} = 100 mV, R_L = 1 MΩ	25°C	3.2	4.1		V
				85°C	3	4.2		
				−40°C	3	4.1		
V_{OL}	Low-level output voltage		V_{ID} = −100 mV, I_{OL} = 0	25°C		0	50	mV
				85°C		0	50	
				−40°C		0	50	
A_{VD}	Large-signal differential voltage amplification		V_O = 0.25 V to 2 V, R_L = 1 MΩ	25°C	50	480		V/mV
				85°C	50	330		
				−40°C	50	900		
CMRR	Common-mode rejection ratio		V_{IC} = V_{ICR} min	25°C	65	94		dB
				85°C	60	95		
				−40°C	60	95		
k_{SVR}	Supply-voltage rejection ratio (ΔV_{DD} / ΔV_{IO})		V_{DD} = 5 V to 10 V, V_O = 1.4 V	25°C	70	97		dB
				85°C	60	98		
				−40°C	60	97		
I_{DD}	Supply current (two amplifiers)		No load, V_O = 2.5 V, V_{IC} = 2.5 V	25°C		19	34	μA
				85°C		15	26	
				−40°C		31	54	

NOTES: 5. The typical values of input bias current and input offset current below 5 pA were determined mathematically.
6. This range also applies to each input individually.

electrical characteristics at specified free-air temperature, V_{DD} = 10 V (unless otherwise noted)

PARAMETER			TEST CONDITIONS		I- SUFFIX TYPES MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage	TLC27L2I	V_O = 1.4 V, V_{IC} = 0 V, R_S = 50 Ω, R_L = 1 MΩ	25°C		1.1	10	mV
				Full range			13	
		TLC27L2AI	V_O = 1.4 V, V_{IC} = 0 V, R_S = 50 Ω, R_L = 1 MΩ	25°C		0.9	5	
				Full range			7	
		TLC27L2BI	V_O = 1.4 V, V_{IC} = 0 V, R_S = 50 Ω, R_L = 1 MΩ	25°C		235	2000	μV
				Full range			3500	
		TLC27L7I	V_O = 1.4 V, V_{IC} = 0 V, R_S = 50 Ω, R_L = 1 MΩ	25°C		190	800	
				Full range			2900	
α_{VIO}	Average temperature coefficient of input offset voltage			25°C to 85°C		1		μV/°C
I_{IO}	Input offset current (see Note 5)		V_{IC} = 5 V, V_O = 5 V	25°C		0.1		pA
				85°C		26	1000	
I_{IB}	Input bias current (see Note 5)		V_{IC} = 5 V, V_O = 5 V	25°C		0.7		pA
				85°C		220	2000	
V_{ICR}	Common-mode input voltage range (see Note 6)			25°C	−0.2 to 9	−0.3 to 9.2		V
				Full range	−0.2 to 8.5			V
V_{OH}	High-level output voltage		V_{ID} = 100 mV, R_L = 1 MΩ	25°C	8	8.9		V
				85°C	7.8	8.9		
				−40°C	7.8	8.9		
V_{OL}	Low-level output voltage		V_{ID} = −100 mV, I_{OL} = 0	25°C		0	50	mV
				85°C		0	50	
				−40°C		0	50	
A_{VD}	Large-signal differential voltage amplification		V_O = 1 V to 6 V, R_L = 1 MΩ	25°C	50	800		V/mV
				85°C	50	585		
				−40°C	50	1550		
CMRR	Common-mode rejection ratio		V_{IC} = V_{ICR} min	25°C	65	97		dB
				85°C	60	98		
				−40°C	60	97		
k_{SVR}	Supply-voltage rejection ratio (ΔV_{DD} / ΔV_{IO})		V_{DD} = 5 V to 10 V, V_O = 1.4 V	25°C	70	97		dB
				85°C	60	98		
				−40°C	60	97		
I_{DD}	Supply current (two amplifiers)		No load, V_O = 5 V, V_{IC} = 5 V	25°C		29	46	μA
				85°C		20	36	
				−40°C		49	86	

NOTES: 5. The typical values of input bias current and input offset current below 5 pA were determined mathematically.
6. This range also applies to each input individually.

electrical characteristics at specified free-air temperature, V_{DD} = 5 V (unless otherwise noted)

PARAMETER			TEST CONDITIONS		M- SUFFIX TYPES MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage	TLC27L2M	V_O = 1.4 V, V_{IC} = 0 V, R_S = 50 Ω, R_L = 1 MΩ	25°C		1.1	10	mV
				Full range			12	
		TLC27L7M	V_O = 1.4 V, V_{IC} = 0 V, R_S = 50 Ω, R_L = 1 MΩ	25°C		170	500	μV
				Full range			3750	
α_{VIO}	Average temperature coefficient of input offset voltage			25°C to 125°C		1.4		μV/°C
I_{IO}	Input offset current (see Note 5)		V_{IC} = 2.5 V, V_O = 2.5 V	25°C		0.1		pA
				125°C		1.4	15	nA
I_{IB}	Input bias current (see Note 5)		V_{IC} = 2.5 V, V_O = 2.5 V	25°C		0.6		pA
				125°C		9	35	nA
V_{ICR}	Common-mode input voltage range (see Note 6)			25°C	0 to 4	−0.3 to 4.2		V
				Full range	0 to 3.5			V
V_{OH}	High-level output voltage		V_{ID} = 100 mV, R_L = 1 MΩ	25°C	3.2	4.1		V
				125°C	3	4.2		
				−55°C	3	4.1		
V_{OL}	Low-level output voltage		V_{ID} = −100 mV, I_{OL} = 0	25°C		0	50	mV
				125°C		0	50	
				−55°C		0	50	
A_{VD}	Large-signal differential voltage amplification		V_O = 0.25 V to 2 V, R_L = 1 MΩ	25°C	50	480		V/mV
				125°C	25	200		
				−55°C	25	950		
CMRR	Common-mode rejection ratio		V_{IC} = V_{ICR} min	25°C	65	94		dB
				125°C	60	85		
				−55°C	60	95		
k_{SVR}	Supply-voltage rejection ratio (ΔV_{DD} / ΔV_{IO})		V_{DD} = 5 V to 10 V, V_O = 1.4 V	25°C	70	97		dB
				125°C	60	98		
				−55°C	60	97		
I_{DD}	Supply current (two amplifiers)		No load, V_O = 2.5 V, V_{IC} = 2.5 V	25°C		19	34	μA
				125°C		14	24	
				−55°C		35	60	

NOTES: 5. The typical values of input bias current and input offset current below 5 pA were determined mathematically.
6. This range also applies to each input individually.

electrical characteristics at specified free-air temperature, V_{DD} = 10 V (unless otherwise noted)

PARAMETER			TEST CONDITIONS		M- SUFFIX TYPES MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage	TLC27L2M	V_O = 1.4 V, V_{IC} = 0 V, R_S = 50 Ω, R_L = 1 MΩ	25°C		1.1	10	mV
				Full range			12	
		TLC27L7M	V_O = 1.4 V, V_{IC} = 0 V, R_S = 50 Ω, R_L = 1 MΩ	25°C		190	800	μV
				Full range			4300	
α_{VIO}	Average temperature coefficient of input offset voltage			25°C to 125°C		1.4		μV/°C
I_{IO}	Input offset current (see Note 5)		V_{IC} = 5 V, V_O = 5 V	25°C		0.1		pA
				125°C		1.8	15	nA
I_{IB}	Input bias current (see Note 5)		V_{IC} = 5 V, V_O = 5 V	25°C		0.7		pA
				125°C		10	35	nA
V_{ICR}	Common-mode input voltage range (see Note 6)			25°C	0 to 9	−0.3 to 9.2		V
				Full range	0 to 8.5			V
V_{OH}	High-level output voltage		V_{ID} = 100 mV, R_L = 1 MΩ	25°C	8	8.9		V
				125°C	7.8	9		
				−55°C	7.8	8.8		
V_{OL}	Low-level output voltage		V_{ID} = −100 mV, I_{OL} = 0	25°C		0	50	mV
				125°C		0	50	
				−55°C		0	50	
A_{VD}	Large-signal differential voltage amplification		V_O = 1 V to 6 V, R_L = 1 MΩ	25°C	50	800		V/mV
				125°C	25	380		
				−55°C	25	1750		
CMRR	Common-mode rejection ratio		V_{IC} = V_{ICR} min	25°C	65	97		dB
				125°C	60	91		
				−55°C	60	97		
k_{SVR}	Supply-voltage rejection ratio (ΔV_{DD} / ΔV_{IO})		V_{DD} = 5 V to 10 V, V_O = 1.4 V	25°C	70	97		dB
				125°C	60	98		
				−55°C	60	97		
I_{DD}	Supply current (two amplifiers)		No load, V_O = 5 V, V_{IC} = 5 V	25°C		29	46	μA
				125°C		18	30	
				−55°C		56	96	

NOTES: 5. The typical values of input bias current and input offset current below 5 pA were determined mathematically.
6. This range also applies to each input individually.

operating characteristics, V_{DD} = 5 V

PARAMETER		TEST CONDITIONS			C- SUFFIX TYPES MIN	C- SUFFIX TYPES TYP	C- SUFFIX TYPES MAX	UNIT
SR	Slew rate at unity gain	R_L = 1 MΩ, C_L = 20 pF, See Figure 1	V_{IPP} = 1 V	25°C		0.03		V/μs
				70°C		0.03		
				0°C		0.04		
			V_{IPP} = 2.5 V	25°C		0.03		
				70°C		0.02		
				0°C		0.03		
V_n	Equivalent input noise voltage	f = 1 kHz, See Figure 2	R_S = 100 Ω,	25°C		68		nV/√Hz
B_{OM}	Maximum output swing bandwidth	V_O = V_{OH}, R_L = 1 MΩ,	C_L = 20 pF, See Figure 1	25°C		5		kHz
				70°C		4.5		
				0°C		6		
B_1	Unity-gain bandwidth	V_i = 10 mV, C_L = 20 pF,	See Figure 3	25°C		85		kHz
				70°C		65		
				0°C		100		
ϕ_m	Phase margin	f = B_1, V_i = 10 mV, C_L = 20 pF,	See Figure 3	25°C		34°		
				70°C		30°		
				0°C		36°		

operating characteristics, V_{DD} = 10 V

PARAMETER		TEST CONDITIONS			C- SUFFIX TYPES MIN	C- SUFFIX TYPES TYP	C- SUFFIX TYPES MAX	UNIT
SR	Slew rate at unity gain	R_L = 1 MΩ, C_L = 20 pF, See Figure 1	V_{IPP} = 1 V	25°C		0.05		V/μs
				70°C		0.04		
				0°C		0.05		
			V_{IPP} = 5.5 V	25°C		0.04		
				70°C		0.04		
				0°C		0.05		
V_n	Equivalent input noise voltage	f = 1 kHz, See Figure 2	R_S = 100 Ω,	25°C		68		nV/√Hz
B_{OM}	Maximum output swing bandwidth	V_O = V_{OH}, R_L = 1 MΩ,	C_L = 20 pF, See Figure 1	25°C		1		kHz
				70°C		0.9		
				0°C		1.3		
B_1	Unity-gain bandwidth	V_i = 10 mV, C_L = 20 pF,	See Figure 3	25°C		110		kHz
				70°C		90		
				0°C		125		
ϕ_m	Phase margin	f = B_1, V_i = 10 mV, C_L = 20 pF,	See Figure 3	25°C		38°		
				70°C		34°		
				0°C		40°		

operating characteristics, V_{DD} = 5 V

PARAMETER		TEST CONDITIONS			I- SUFFIX TYPES MIN	I- SUFFIX TYPES TYP	I- SUFFIX TYPES MAX	UNIT
SR	Slew rate at unity gain	R_L = 1 MΩ, C_L = 20 pF, See Figure 1	V_{IPP} = 1 V	25°C		0.03		V/μs
				85°C		0.03		
				− 40°C		0.04		
			V_{IPP} = 2.5 V	25°C		0.03		
				85°C		0.02		
				− 40°C		0.04		
V_n	Equivalent input noise voltage	f = 1 kHz, R_S = 100 Ω, See Figure 2		25°C		68		nV/√Hz
B_{OM}	Maximum output swing bandwidth	$V_O = V_{OH}$, C_L = 20 pF, R_L = 1 MΩ, See Figure 1		25°C		5		kHz
				85°C		4		
				− 40°C		7		
B_1	Unity-gain bandwidth	V_i = 10 mV, C_L = 20 pF, See Figure 3		25°C		85		kHz
				85°C		55		
				− 40°C		130		
ϕ_m	Phase margin	f = B_1, V_i = 10 mV, C_L = 20 pF, See Figure 3		25°C		34°		
				85°C		28°		
				− 40°C		38°		

operating characteristics, V_{DD} = 10 V

PARAMETER		TEST CONDITIONS			I- SUFFIX TYPES MIN	I- SUFFIX TYPES TYP	I- SUFFIX TYPES MAX	UNIT
SR	Slew rate at unity gain	R_L = 1 MΩ, C_L = 20 pF, See Figure 1	V_{IPP} = 1 V	25°C		0.05		V/μs
				85°C		0.03		
				− 40°C		0.06		
			V_{IPP} = 5.5 V	25°C		0.04		
				85°C		0.03		
				− 40°C		0.05		
V_n	Equivalent input noise voltage	f = 1 kHz, R_S = 100 Ω, See Figure 2		25°C		68		nV/√Hz
B_{OM}	Maximum output swing bandwidth	$V_O = V_{OH}$, C_L = 20 pF, R_L = 1 MΩ, See Figure 1		25°C		1		kHz
				85°C		0.8		
				− 40°C		1.4		
B_1	Unity-gain bandwidth	V_i = 10 mV, C_L = 20 pF, See Figure 3		25°C		110		kHz
				85°C		80		
				− 40°C		155		
ϕ_m	Phase margin	f = B_1, V_i = 10 mV, C_L = 20 pF, See Figure 3		25°C		38°		
				85°C		32°		
				− 40°C		42°		

operating characteristics, V_{DD} = 5 V

PARAMETER		TEST CONDITIONS			M- SUFFIX TYPES MIN	M- SUFFIX TYPES TYP	M- SUFFIX TYPES MAX	UNIT
SR	Slew rate at unity gain	R_L = 1 MΩ, C_L = 20 pF, See Figure 1	V_{IPP} = 1 V	25°C		0.03		V/μs
				125°C		0.02		
				– 55°C		0.04		
			V_{IPP} = 2.5 V	25°C		0.03		
				125°C		0.02		
				– 55°C		0.04		
V_n	Equivalent input noise voltage	f = 1 kHz, See Figure 2	R_S = 100 Ω,	25°C		68		nV/√Hz
B_{OM}	Maximum output swing bandwidth	$V_O = V_{OH}$, R_L = 1 MΩ,	C_L = 20 pF, See Figure 1	25°C		5		kHz
				125°C		3		
				– 55°C		8		
B_1	Unity-gain bandwidth	V_i = 10 mV, C_L = 20 pF,	See Figure 3	25°C		85		kHz
				125°C		45		
				– 55°C		140		
ϕ_m	Phase margin	f = B_1, V_i = 10 mV, C_L = 20 pF,	See Figure 3	25°C		34°		
				125°C		25°		
				– 55°C		39°		

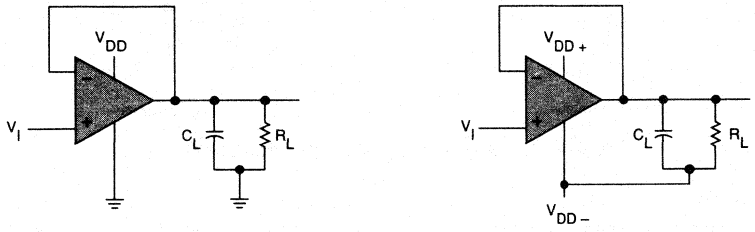
operating characteristics, V_{DD} = 10 V

PARAMETER		TEST CONDITIONS			M- SUFFIX TYPES MIN	M- SUFFIX TYPES TYP	M- SUFFIX TYPES MAX	UNIT
SR	Slew rate at unity gain	R_L = 1 MΩ, C_L = 20 pF, See Figure 1	V_{IPP} = 1 V	25°C		0.05		V/μs
				125°C		0.03		
				– 55°C		0.06		
			V_{IPP} = 5.5 V	25°C		0.04		
				125°C		0.03		
				– 55°C		0.06		
V_n	Equivalent input noise voltage	f = 1 kHz, See Figure 2	R_S = 100 Ω,	25°C		68		nV/√Hz
B_{OM}	Maximum output swing bandwidth	$V_O = V_{OH}$, R_L = 1 MΩ,	C_L = 20 pF, See Figure 1	25°C		1		kHz
				125°C		0.7		
				– 55°C		1.5		
B_1	Unity-gain bandwidth	V_i = 10 mV, C_L = 20 pF,	See Figure 3	25°C		110		kHz
				125°C		70		
				– 55°C		165		
ϕ_m	Phase margin	f = B_1, V_i = 10 mV, C_L = 20 pF,	See Figure 3	25°C		38°		
				125°C		29°		
				– 55°C		43°		

PARAMETER MEASUREMENT INFORMATION

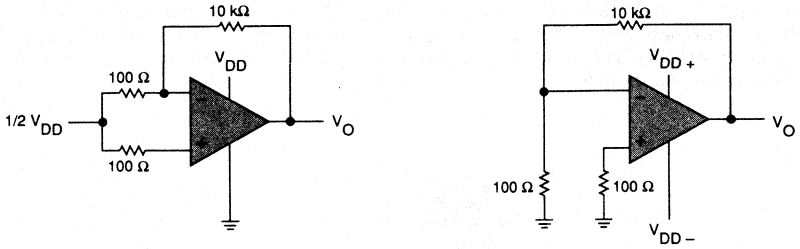
single-supply versus split-supply test circuits

Because the TLC27L2 and TLC27L7 are optimized for single-supply operation, circuit configurations used for the various tests often present some inconvenience since the input signal, in many cases, must be offset from ground. This inconvenience can be avoided by testing the device with split supplies and the output load tied to the negative rail. A comparison of single-supply versus split-supply test circuits is shown below. The use of either circuit will give the same result.



(a) Single-Supply (b) Split-Supply

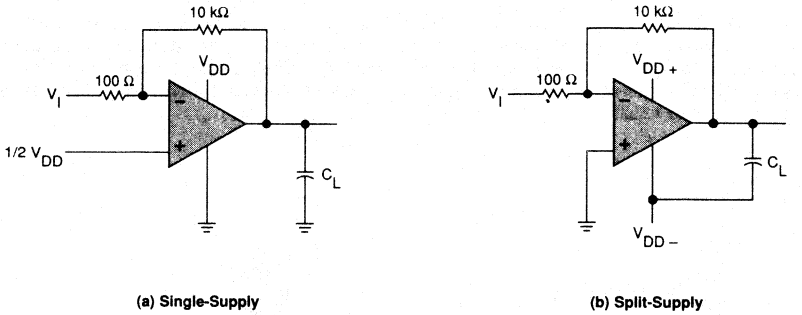
FIGURE 1. UNITY-GAIN AMPLIFIER



(a) Single-Supply (b) Split-Supply

FIGURE 2. NOISE TEST CIRCUIT

PARAMETER MEASUREMENT INFORMATION



(a) Single-Supply (b) Split-Supply

FIGURE 3. GAIN-OF-100 INVERTING AMPLIFIER

input bias current

Because of the high input impedance of the TLC27L2 and TLC27L7 op amps, attempts to measure the input bias current can result in erroneous readings. The bias current at normal room ambient temperature is typically less than 1 pA, a value that is easily exceeded by leakages on the test socket. Two suggestions are offered to avoid erroneous measurements:

1 Isolate the device from other potential leakage sources. Use a grounded shield around and between the device inputs (see Figure 4). Leakages that would otherwise flow to the inputs will be shunted away.

2 Compensate for the leakage of the test socket by actually performing an input bias current test (using a picoammeter) with no device in the test socket. The actual input bias current can then be calculated by subtracting the "open-socket" leakage readings from the readings obtained with a device in the test socket.

One word of caution . . . many automatic testers as well as some bench-top op amp testers use the servo-loop technique with a resistor in series with the device input to measure the input bias current (the voltage drop across the series resistor is measured and the bias current is calculated). This method requires that a device be inserted into the test socket to obtain a correct reading; therefore, an "open-socket" reading is not feasible using this method.

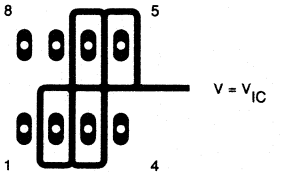


FIGURE 4. ISOLATION METAL AROUND DEVICE INPUTS
(JG AND P DUAL-IN-LINE PACKAGE)

PARAMETER MEASUREMENT INFORMATION

low-level output voltage

To obtain low-supply-voltage operation, some compromise was necessary in the input stage. This compromise results in the device low-level output being dependent on both the common-mode input voltage level as well as the differential input voltage level. When attempting to correlate low-level output readings with those quoted in the electrical specifications, these two conditions should be observed. If conditions other than these are to be used, please refer to Figures 14 thru 19 in the Typical Characteristics section of this data sheet.

input offset voltage temperature coefficient

Erroneous readings often result from attempts to measure temperature coefficient of input offset voltage. This parameter is actually a calculation using input offset voltage measurements obtained at two different temperatures. When one (or both) of the temperatures is below freezing, moisture can collect on both the device and the test socket. This moisture will result in leakage and contact resistance which can cause erroneous input offset voltage readings. The isolation techniques previously mentioned have no affect on the leakage since the moisture also covers the isolation metal itself, thereby rendering it useless. It is suggested that these measurements be performed at temperatures above freezing to minimize error.

full power response

Full power response, the frequency above which the op amp slew rate limits the output voltage swing, is often specified two ways . . . full-linear response and full-peak response. The full-linear response is generally measured by monitoring the distortion level of the output while increasing the frequency of a sinusoidal input signal until the maximum frequency is found above which the output contains significant distortion. The full-peak response is defined as the maximum output frequency, without regard to distortion, above which full peak-to-peak output swing cannot be maintained.

Because there is no industry-wide accepted value for "significant" distortion, the full-peak response is specified in this data sheet and is measured using the circuit of Figure 1. The initial setup involves the use of a sinusoidal input to determine the maximum peak-to-peak output of the device (the amplitude of the sinusoidal wave is increased until clipping occurs). The sinusoidal wave is then replaced with a square wave of the same amplitude. The frequency is then increased until the maximum peak-to-peak output can no longer be maintained (Figure 5). A square wave is used to allow a more accurate determination of the point at which the maximum peak-to-peak output is reached.

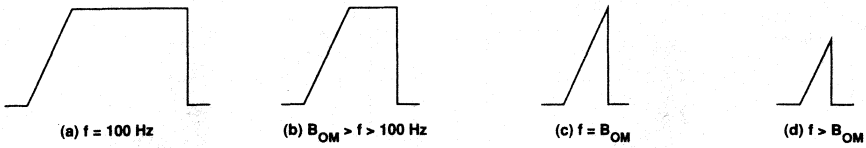


FIGURE 5. FULL-POWER-RESPONSE OUTPUT SIGNAL

test time

Inadequate test time is a frequent problem, especially when testing CMOS devices in a high-volume, short-test-time environment. Internal capacitances are inherently higher in CMOS than in bipolar and BiFET devices, and require longer test times than their bipolar and BiFET counterparts. The problem becomes more pronounced with reduced supply levels and lower temperatures.

TYPICAL CHARACTERISTICS

DISTRIBUTION OF TLC27L2
INPUT OFFSET VOLTAGE

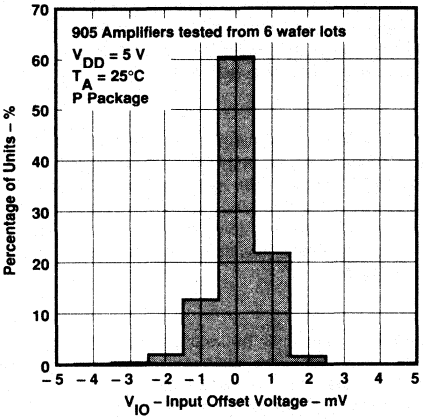


FIGURE 6

DISTRIBUTION OF TLC27L2
INPUT OFFSET VOLTAGE

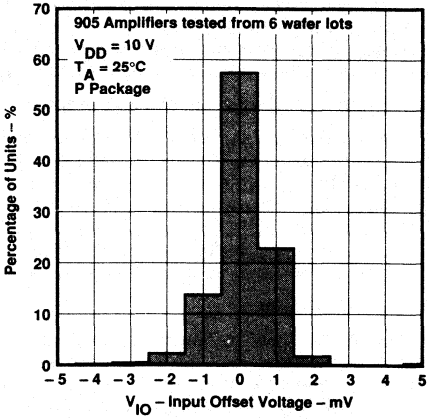


FIGURE 7

DISTRIBUTION OF TLC27L2 AND TLC27L7
INPUT OFFSET VOLTAGE
TEMPERATURE COEFFICIENT

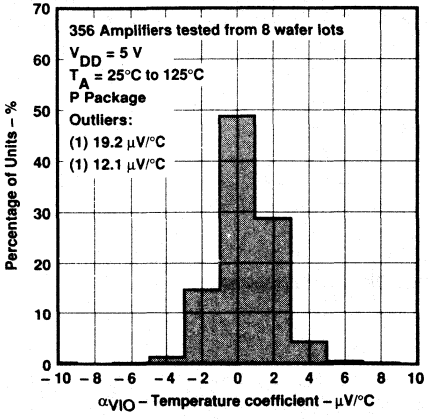


FIGURE 8

DISTRIBUTION OF TLC27L2 AND TLC27L7
INPUT OFFSET VOLTAGE
TEMPERATURE COEFFICIENT

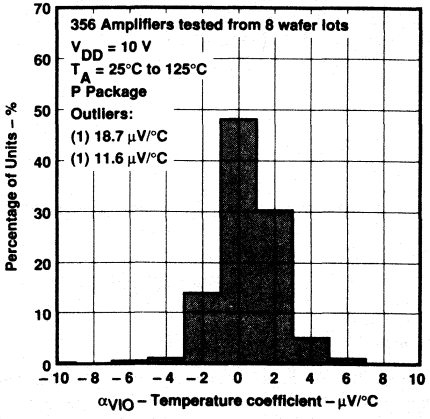


FIGURE 9

TYPICAL CHARACTERISTICS

HIGH-LEVEL OUTPUT VOLTAGE
vs
HIGH-LEVEL OUTPUT CURRENT

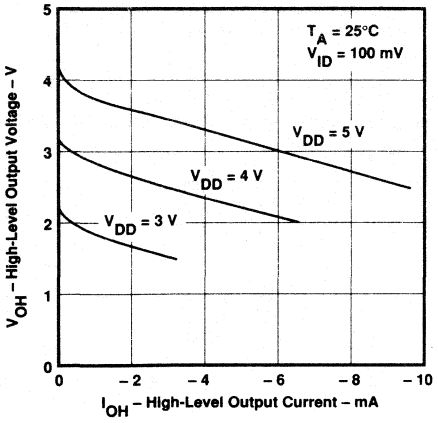


FIGURE 10

HIGH-LEVEL OUTPUT VOLTAGE
vs
HIGH-LEVEL OUTPUT CURRENT

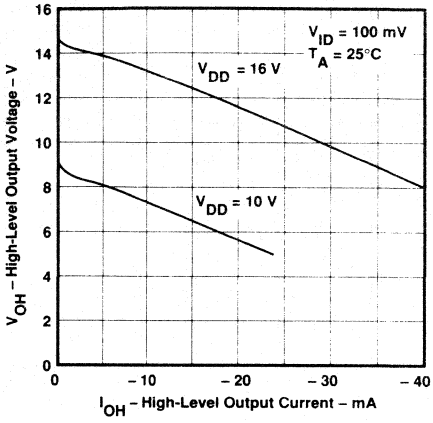


FIGURE 11

HIGH-LEVEL OUTPUT VOLTAGE
vs
SUPPLY VOLTAGE

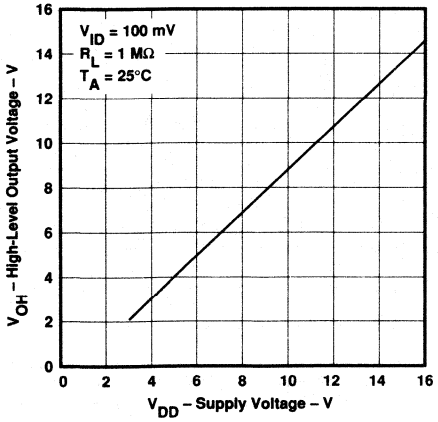


FIGURE 12

HIGH-LEVEL OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE

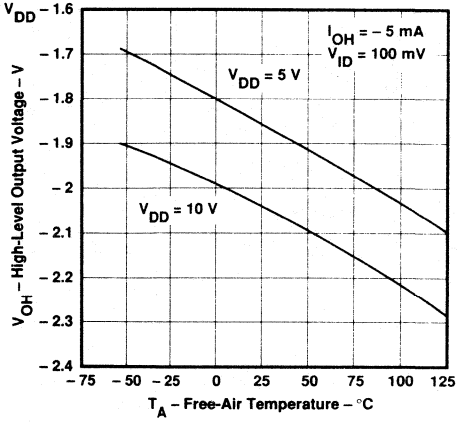


FIGURE 13

TYPICAL CHARACTERISTICS

LOW-LEVEL OUTPUT VOLTAGE
vs
COMMON-MODE INPUT VOLTAGE

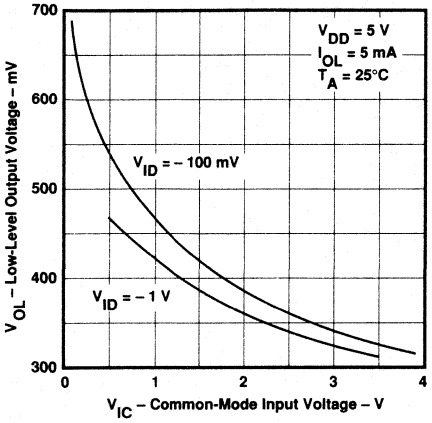


FIGURE 14

LOW-LEVEL OUTPUT VOLTAGE
vs
COMMON-MODE INPUT VOLTAGE

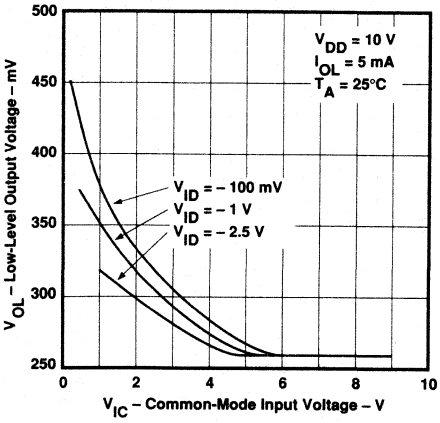


FIGURE 15

LOW-LEVEL OUTPUT VOLTAGE
vs
DIFFERENTIAL INPUT VOLTAGE

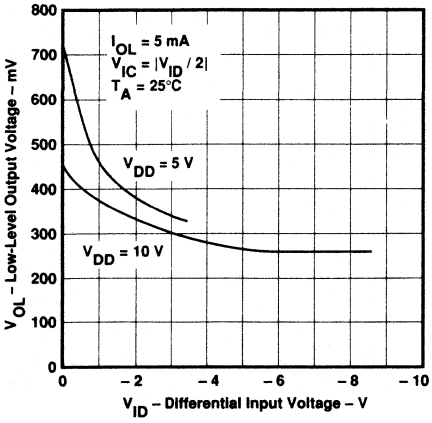


FIGURE 16

LOW-LEVEL OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE

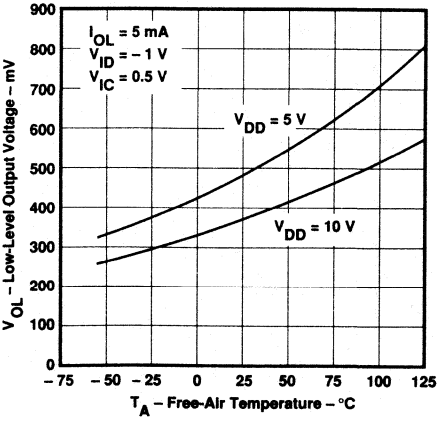


FIGURE 17

TYPICAL CHARACTERISTICS

LOW-LEVEL OUTPUT VOLTAGE
vs
LOW-LEVEL OUTPUT CURRENT

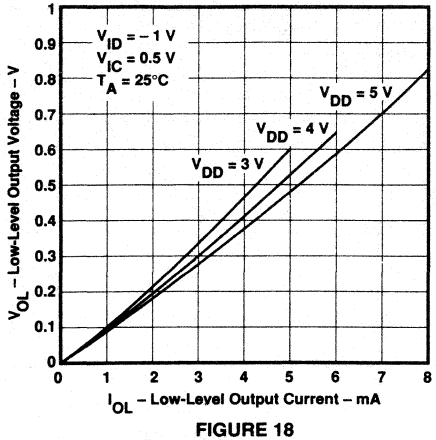


FIGURE 18

LOW-LEVEL OUTPUT VOLTAGE
vs
LOW-LEVEL OUTPUT CURRENT

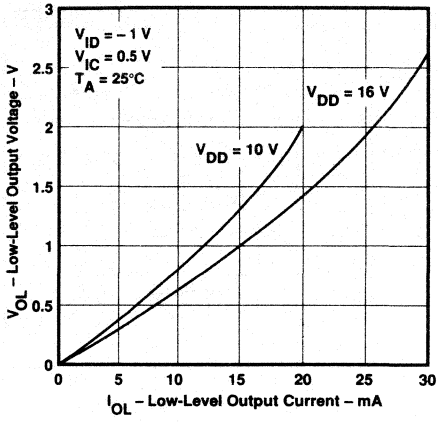


FIGURE 19

LARGE-SIGNAL
DIFFERENTIAL VOLTAGE AMPLIFICATION
vs
SUPPLY VOLTAGE

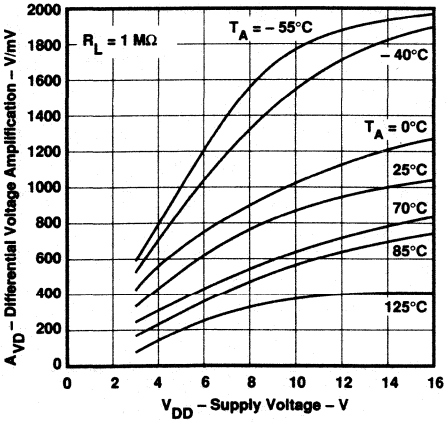


FIGURE 20

LARGE-SIGNAL
DIFFERENTIAL VOLTAGE AMPLIFICATION
vs
FREE-AIR TEMPERATURE

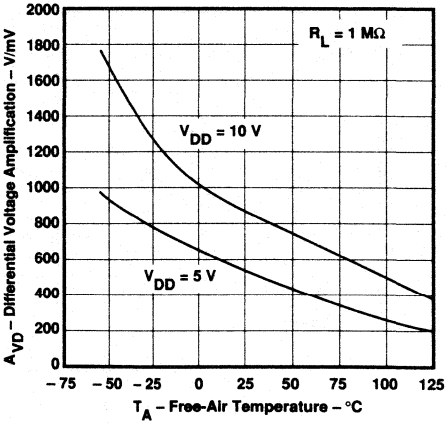


FIGURE 21

TYPICAL CHARACTERISTICS

INPUT BIAS CURRENT AND INPUT OFFSET CURRENT
vs
FREE-AIR TEMPERATURE

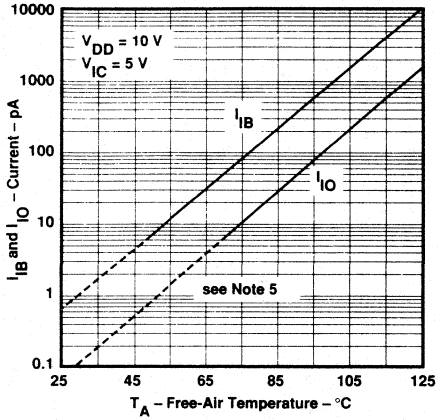


FIGURE 22

MAXIMUM INPUT VOLTAGE
vs
SUPPLY VOLTAGE

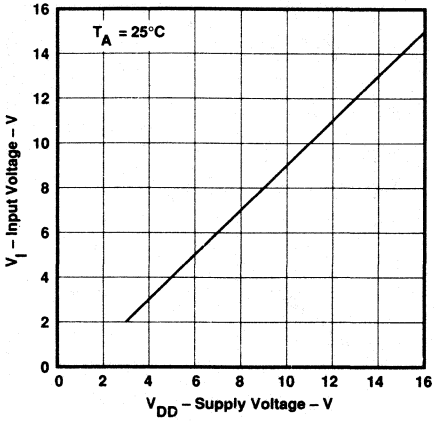


FIGURE 23

SUPPLY CURRENT
vs
SUPPLY VOLTAGE

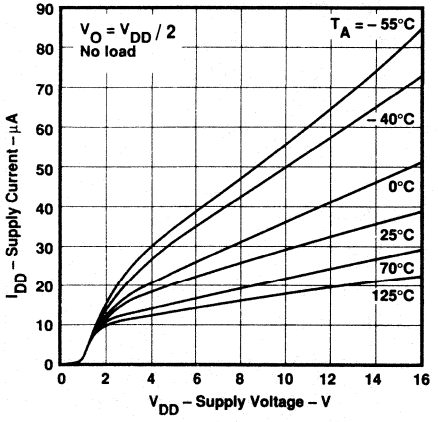


FIGURE 24

SUPPLY CURRENT
vs
FREE-AIR TEMPERATURE

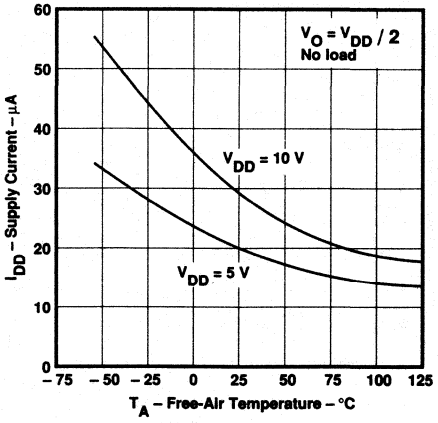


FIGURE 25

NOTE 5: The typical values of input bias current and input offset current below 5 pA were determined mathematically.

TYPICAL CHARACTERISTICS

SLEW RATE
vs
SUPPLY VOLTAGE

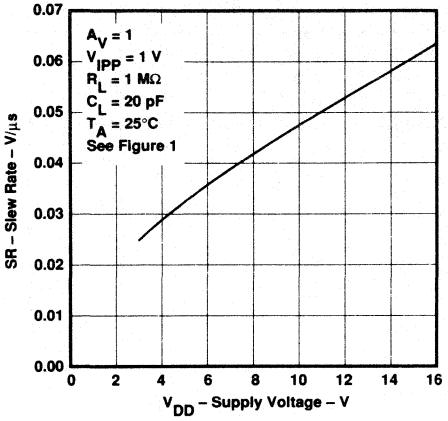


FIGURE 26

SLEW RATE
vs
FREE-AIR TEMPERATURE

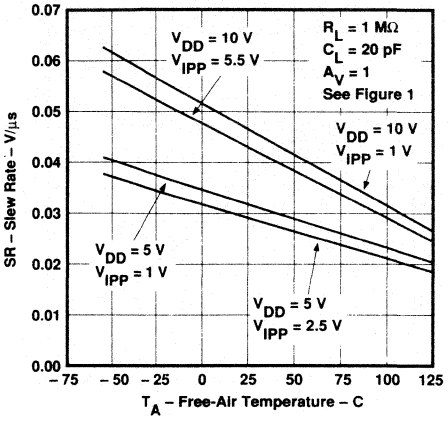


FIGURE 27

NORMALIZED SLEW RATE
vs
FREE-AIR TEMPERATURE

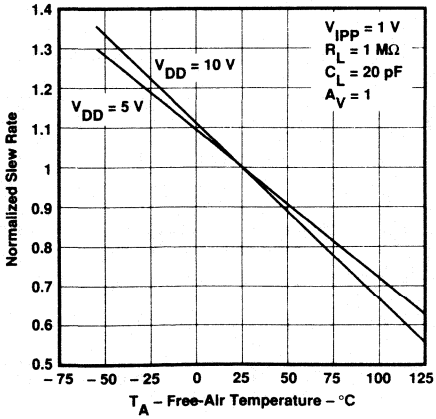


FIGURE 28

MAXIMUM PEAK-TO-PEAK OUTPUT VOLTAGE
vs
FREQUENCY

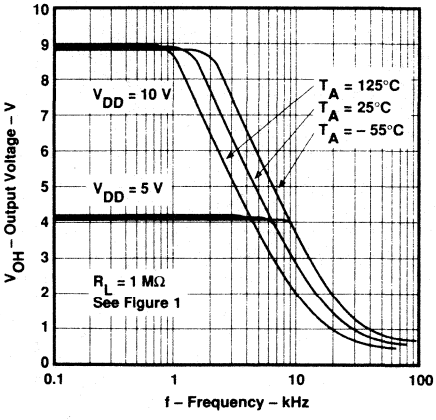


FIGURE 29

TYPICAL CHARACTERISTICS

UNITY-GAIN BANDWIDTH
vs
FREE-AIR TEMPERATURE

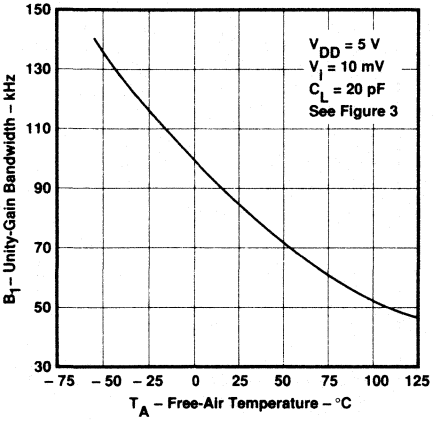


FIGURE 30

UNITY-GAIN BANDWIDTH
vs
SUPPLY VOLTAGE

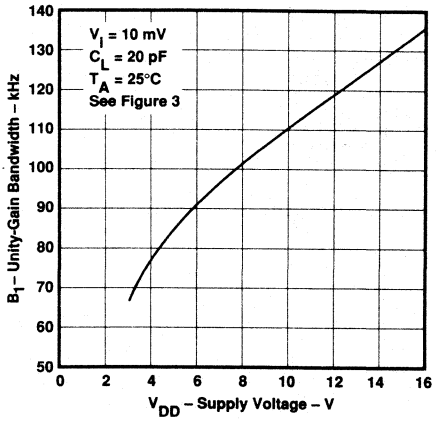


FIGURE 31

LARGE-SIGNAL DIFFERENTIAL VOLTAGE
AMPLIFICATION AND PHASE SHIFT
vs
FREQUENCY

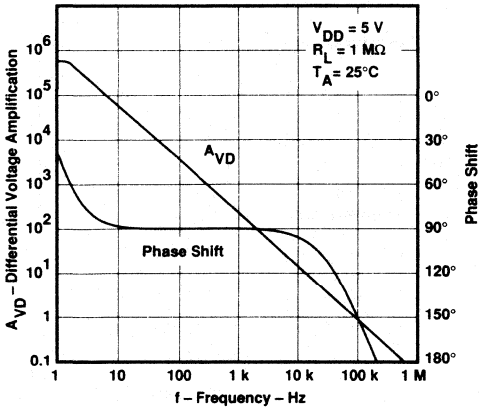


FIGURE 32

LARGE-SIGNAL DIFFERENTIAL VOLTAGE
AMPLIFICATION AND PHASE SHIFT
vs
FREQUENCY

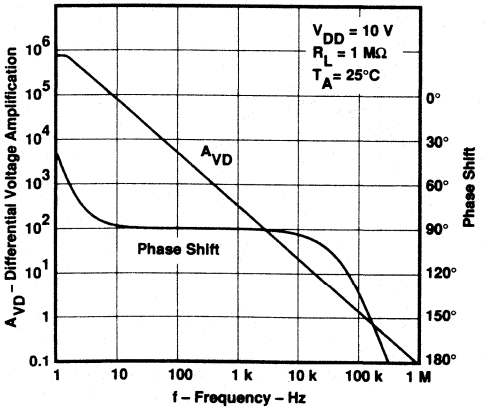


FIGURE 33

TYPICAL CHARACTERISTICS

PHASE MARGIN
vs
SUPPLY VOLTAGE

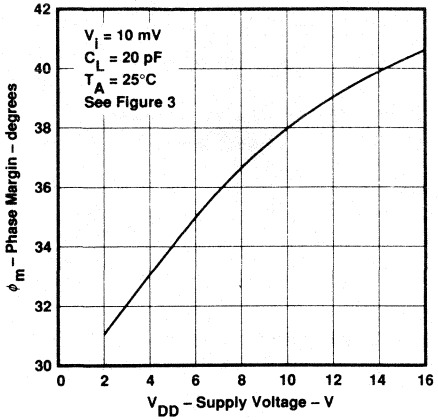


FIGURE 34

PHASE MARGIN
vs
FREE-AIR TEMPERATURE

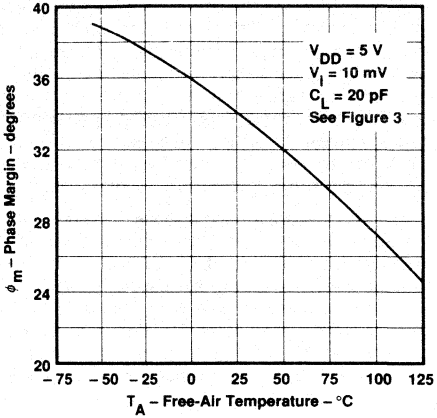


FIGURE 35

PHASE MARGIN
vs
CAPACITIVE LOAD

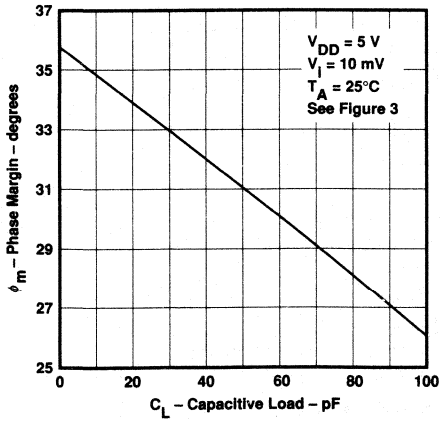


FIGURE 36

EQUIVALENT INPUT NOISE VOLTAGE
vs
FREQUENCY

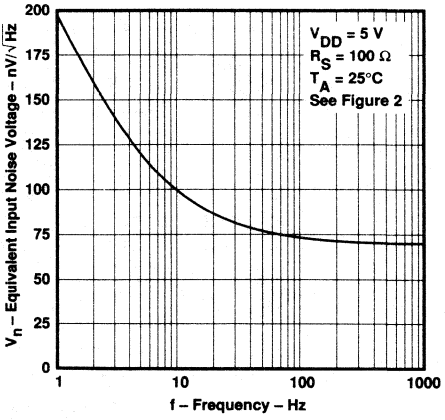


FIGURE 37

single-supply operation

While the TLC27L2 and TLC27L7 will perform well using dual power supplies (also called balanced or split supplies), the design is optimized for single-supply operation. This includes an input common mode voltage range that encompasses ground as well as an output voltage range that pulls down to ground. The supply voltage range extends down to 3 V (C- suffix types), thus allowing operation with supply levels commonly available for TTL and HCMOS; however, for maximum dynamic range, 16-V single-supply operation is recommended.

Many single-supply applications require that a voltage be applied to one input to establish a reference level that is above ground. A resistive voltage divider is usually sufficient to establish this reference level (see Figure 38). The low input bias current consumption of the TLC27L2 and TLC27L7 permits the use of very large resistive values to implement the voltage divider, thus minimizing power consumption.

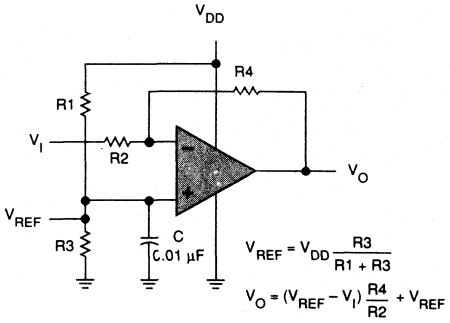
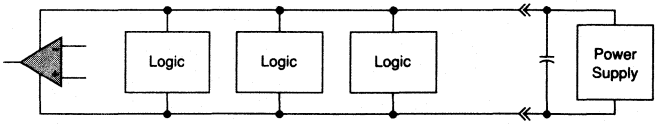


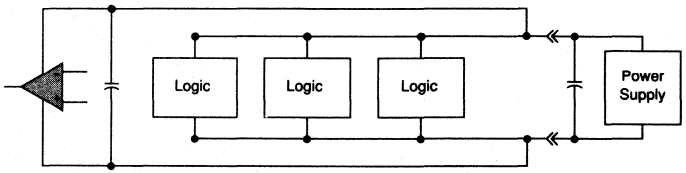
FIGURE 38. INVERTING AMPLIFIER WITH VOLTAGE REFERENCE

The TLC27L2 and TLC27L7 work well in conjunction with digital logic; however, when powering both linear devices and digital logic from the same power supply, the following precautions are recommended:

1. Power the linear devices from separate bypassed supply lines (see Figure 39); otherwise the linear device supply rails can fluctuate due to voltage drops caused by high switching currents in the digital logic.
2. Use proper bypass techniques to reduce the probability of noise-induced errors. Single capacitive decoupling is often adequate; however, RC decoupling may be necessary in high-frequency applications.



(a) Common Supply Rails



(b) Separate Bypassed Supply Rails (preferred)

FIGURE 39. COMMON VERSUS SEPARATE SUPPLY RAILS

TYPICAL APPLICATION DATA

input characteristics

The TLC27L2 and TLC27L7 are specified with a minimum and a maximum input voltage that, if exceeded at either input, could cause the device to malfunction. Exceeding this specified range is a common problem, especially in single-supply operation. Note that the lower range limit includes the negative rail, while the upper range limit is specified at V_{DD} – 1 V at T_A = 25°C and at V_{DD} – 1.5 V at all other temperatures.

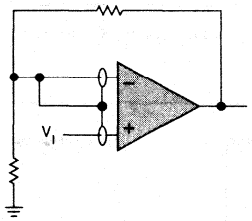
The use of the polysilicon-gate process and the careful input circuit design gives the TLC27L2 and TLC27L7 very good input offset voltage drift characteristics relative to conventional metal-gate processes. Offset voltage drift in CMOS devices is highly influenced by threshold voltage shifts caused by polarization of the phosphorus dopant implanted in the oxide. Placing the phosphorus dopant in a conductor (such as a polysilicon gate) alleviates the polarization problem, thus reducing threshold voltage shifts by more than an order of magnitude. The offset voltage drift with time has been calculated to be typically 0.1 μV/month, including the first month of operation.

Because of the extremely high input impedance and resulting low bias current requirements, the TLC27L2 and TLC27L7 are well suited for low-level signal processing; however, leakage currents on printed circuit boards and sockets can easily exceed bias current requirements and cause a degradation in device performance. It is good practice to include guard rings around inputs (similar to those of Figure 4 in the PARAMETER MEASUREMENT INFORMATION section). These guards should be driven from a low-impedance source at the same voltage level as the common-mode input (see Figure 40).

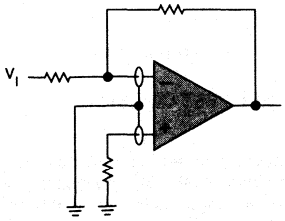
The inputs of any unused amplifiers should be tied to ground to avoid possible oscillation.

noise performance

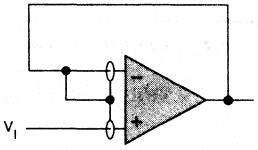
The noise specifications in op amp circuits are greatly dependent on the current in the first-stage differential amplifier. The low input bias current requirements of the TLC27L2 and TLC27L7 result in a very low noise current, which is insignificant in most applications. This feature makes the devices especially favorable over bipolar devices when using values of circuit impedance greater than 50 kΩ, since bipolar devices exhibit greater noise currents.



(a) Noninverting Amplifier



(b) Inverting Amplifier



(c) Unity Gain Amplifier

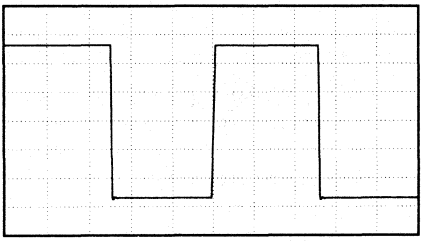
Figure 40. GUARD RING SCHEMES

TYPICAL APPLICATION DATA

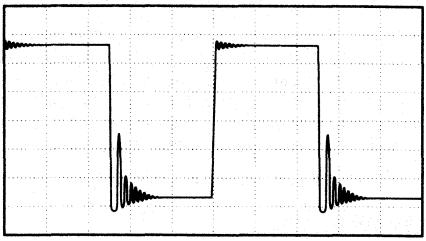
output characteristics

The output stage of the TLC27L2 and TLC27L7 is designed to sink and source relatively high amounts of current (see typical characteristics). If the output is subjected to a short-circuit condition, this high current capability can cause device damage under certain conditions. Output current capability increases with supply voltage.

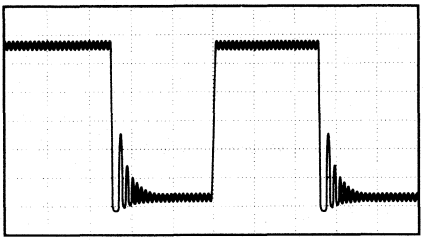
All operating characteristics of the TLC27L2 and TLC27L7 were measured using a 20-pF load. The devices will drive higher capacitive loads; however, as output load capacitance increases, the resulting response pole occurs at lower frequencies, thereby causing ringing, peaking, or even oscillation (see Figure 41). In many cases, adding some compensation in the form of a series resistor in the feedback loop will alleviate the problem.



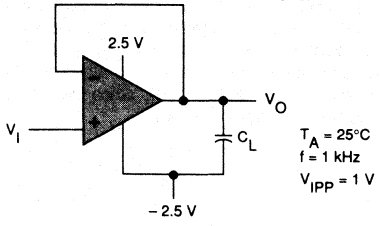
(a) C_L = 20 pF, R_L = no load



(b) C_L = 260 pF, R_L = no load



(c) C_L = 310 pF, R_L = no load



(d) Test Circuit

FIGURE 41. EFFECT OF CAPACITIVE LOADS AND TEST CIRCUIT

Although the TLC27L2 and TLC27L7 possess excellent high-level output voltage and current capability, methods are available for boosting this capability, if needed. The simplest method involves the use of a pull-up resistor (R_P) connected from the output to the positive supply rail. There are two disadvantages to the use of this circuit. First, the NMOS pull-down transistor, N4 (see Figure 42) must sink a comparatively large amount of current. In this circuit, N4 behaves like a linear resistor with an on resistance between approximately 60 Ω and 180 Ω, depending on how hard the op amp input is driven. With very low values of R_P, a voltage offset from 0 V at the output will occur. Secondly, pull-up resistor R_P acts as a drain load to N4 and the gain of the op amp is reduced at output voltage levels where N5 is not supplying the output current.

TYPICAL APPLICATION DATA

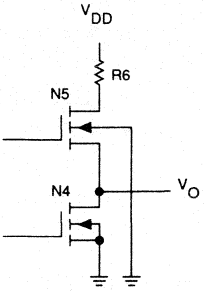


FIGURE 42. TLC27L2 / TLC27L7 OUTPUT STAGE

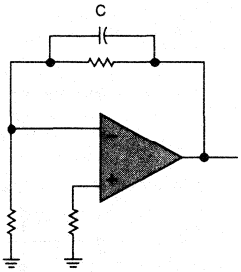


FIGURE 43. COMPENSATION FOR INPUT CAPACITANCE

feedback

Op amp circuits nearly always employ feedback, and since feedback is the first prerequisite for oscillation, a little caution is appropriate. Most oscillation problems result from driving capacitive loads (discussed previously) and ignoring stray input capacitance. A small-value capacitor connected in parallel with the feedback resistor is an effective remedy (see Figure 43). The value of this capacitor is optimized empirically.

electrostatic discharge protection

The TLC27L2 and TLC27L7 incorporate an internal electrostatic discharge (ESD) protection circuit that will prevent functional failures at voltages up to 2000 V as tested under MIL-STD-883C, Method 3015.2. Care should be exercised, however, when handling these devices as exposure to ESD may result in the degradation of the device parametric performance. The protection circuit also causes the input bias currents to be temperature dependent and have the characteristics of a reverse-biased diode.

latchup

Because CMOS devices are susceptible to latchup due to their inherent parasitic thyristors, the TLC27L2 and TLC27L7 inputs and outputs were designed to withstand −100-mA surge currents without sustaining latchup; however, techniques should be used to reduce the chance of latchup whenever possible. Internal protection diodes should not by design be forward biased. Applied input and output voltage should not exceed the supply voltage by more than 300 mV. Care should be exercised when using capacitive coupling on pulse generators. Supply transients should be shunted by the use of decoupling capacitors (0.1 μF typical) located across the supply rails as close to the device as possible.

The current path established if latchup occurs is usually between the positive supply rail and ground and can be triggered by surges on the supply lines and / or voltages on either the output or inputs that exceed the supply voltage. Once latchup occurs, the current flow is limited only by the impedance of the power supply and the forward resistance of the parasitic thyristor and usually results in the destruction of the device. The chance of latchup occuring increases with increasing temperature and supply voltages.

TYPICAL APPLICATION DATA

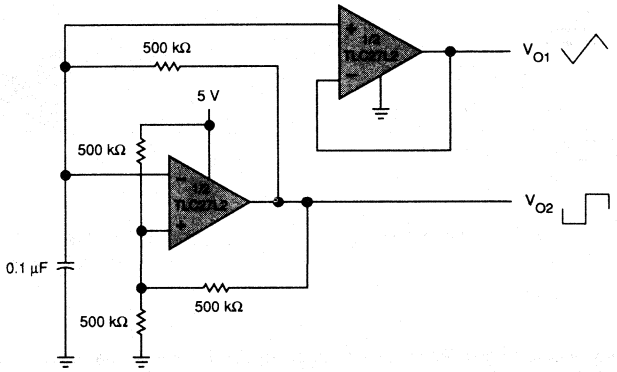
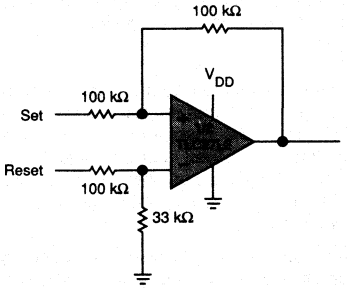


FIGURE 44. MULTIVIBRATOR

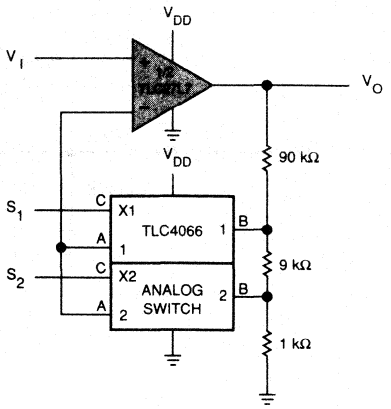


NOTES: V_{DD} = 5 V to 16V

FIGURE 45. SET / RESET FLIP-FLOP

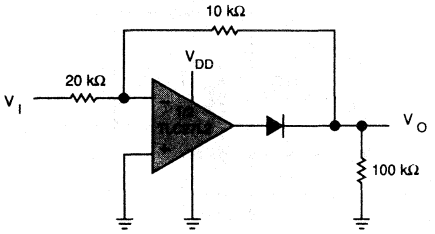
TYPICAL APPLICATION DATA

Select:	S_1	S_2
A_V	10	100



NOTES: V_{DD} = 5 V to 12V

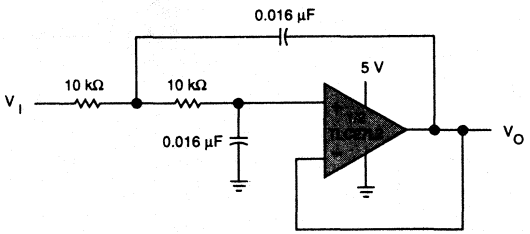
FIGURE 46. AMPLIFIER WITH DIGITAL GAIN SELECTION



NOTES: V_{DD} = 5 V to 16V

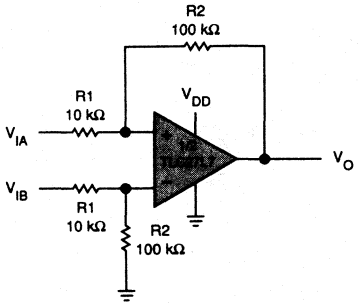
FIGURE 47. FULL WAVE RECTIFIER

TYPICAL APPLICATION DATA



NOTE: Normalized to F_C = 1 kHz and R_L = 10 kΩ

FIGURE 48. TWO-POLE LOW-PASS BUTTERWORTH FILTER



NOTES: V_{DD} = 5 V to 16 V

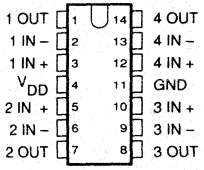
$$V_O = \frac{R2}{R1}(V_{IB} - V_{IA})$$

FIGURE 49. DIFFERENCE AMPLIFIER

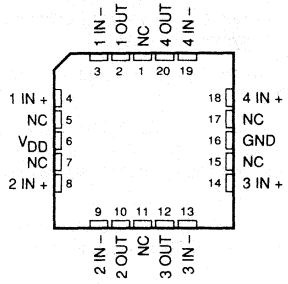
SEPTEMBER 1987

- **Trimmed Offset Voltage:**
  TLC279 ... 900 μV Max at 25°C, V_{DD} = 5 V
- **Input Offset Voltage Drift Typically**
  0.1 μV / Month, Including the First 30 Days
- **Wide Range of Supply Voltages Over Specified Temperature Range:**
  – 55°C to125°C ... 4 V to 16 V
  – 40°C to 85°C ... 4 V to 16 V
  0°C to 70°C ... 3 V to 16 V
- **Single-Supply Operation**
- **Common-Mode Input Voltage Range Extends Below the Negative Rail (C- suffix, I- suffix types)**
- **Low Noise ... 25 nV/√Hz Typically at f = 1 kHz**
- **Output Voltage Range Includes Negative Rail**
- **High Input Impedance ... 10^{12} Ω Typical**
- **ESD Protection Circuitry**
- **Small-Outline Package Option Also Available in Tape-and-Reel**
- **Designed-in Latchup Immunity**

N AND J DUAL-IN-LINE PACKAGE
D SMALL-OUTLINE PACKAGE
(TOP VIEW)



FK CHIP CARRIER PACKAGE
(TOP VIEW)



NC – No internal connection

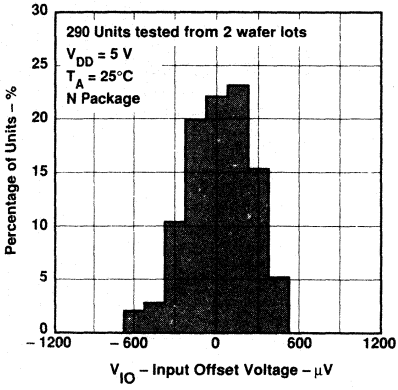
description

The TLC274 and TLC279 quad operational amplifiers combine a wide range of input offset voltage grades with low offset voltage drift, high input impedance, low noise, and speeds approaching that of general-purpose BiFET devices.

T_A	V_{IO}max at 25°C	PACKAGE			
		Small-Outline (D) See Note 1	Plastic DIP (N)	Ceramic DIP (J)	Chip Carrier (FK)
0°C to 70°C	900 μV	TLC279CD	TLC279CN	TLC279CJ	—
	2 mV	TLC274BCD	TLC274BCN	TLC274BCJ	—
	5 mV	TLC274ACD	TLC274ACN	TLC274ACJ	—
	10 mV	TLC274CD	TLC274CN	TLC274CJ	—
– 40°C to 85°C	900 μV	TLC279ID	TLC279IN	TLC279IJ	—
	2 mV	TLC274BID	TLC274BIN	TLC274BIJ	—
	5 mV	TLC274AID	TLC274AIN	TLC274AIJ	—
	10 mV	TLC274ID	TLC274IN	TLC274IJ	—
– 55°C to 125°C	900 μV	—	—	TLC279MJ	TLC279MFK
	10 mV	—	—	TLC274MJ	TLC274MFK

NOTE 1: Available in tape-and-reel. Add "R" suffix to the device type when ordering (e.g., TLC279CDR).

DISTRIBUTION OF TLC279
INPUT OFFSET VOLTAGE



LinCMOS is a trademark of Texas Instruments Incorporated

description (continued)

These devices use Texas Instruments silicon-gate LinCMOS technology, which provides offset voltage stability far exceeding the stability available with conventional metal-gate processes.

The extremely high input impedance, low bias currents, and high slew rates make these cost-effective devices ideal for applications which have previously been reserved for BiFET and NFET products. Four offset voltage grades are available (C- suffix and I- suffix types), ranging from the low-cost TLC274 (10 mV) to the high-precision TLC279 (900 μV). These advantages, in combination with good common-mode rejection and supply voltage rejection, make these devices a good choice for new state-of-the-art designs as well as for upgrading existing designs.

In general, many features associated with bipolar technology are avaliable on LinCMOS operational amplifiers, without the power penalities of bipolar technology. General applications such as transducer interfacing, analog calculations, amplifier blocks, active filters, and signal buffering are all easily designed with the TLC274 and TLC279. The devices also exhibit low voltage single supply operation making them ideally suited for remote and inaccessable battery-powered applications. The common-mode input voltage range includes the negative rail.

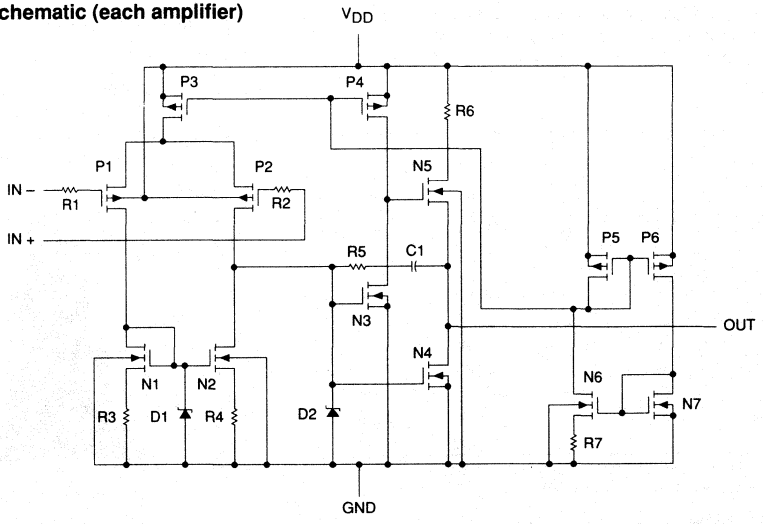
A wide range of packaging options is available, including small outline and chip carrier versions for high-density system applications.

The device inputs and outputs are designed to withstand – 100-mA surge currents without sustaining latchup.

The TLC274 and TLC279 incorporate internal ESD protection circuits that will prevent functional failures at voltages up to 2000 V as tested under MIL-STD-883C, Method 3015.2; however, care should be exercised in handling these devices as exposure to ESD may result in the degradation of the device parametric performance.

The M- suffix devices are characterized for operation over the full military temperature range of – 55°C to 125°C, the I- suffix devices from – 40°C to 85°C, and the C- suffix devices from 0°C to 70°C.

equivalent schematic (each amplifier)



absolute maximum ratings over operating free-air temperature (unless otherwise noted)

Supply voltage, V_{DD} (see Note 2) . . . . . 18 V
Differential input voltage (see Note 3) . . . . . $\pm V_{DD}$
Input voltage range, V_I (any input) . . . . . -0.3 V to V_{DD}
Input current, I_I . . . . . ± 5 mA
Output current, I_O (each output) . . . . . ± 30 mA
Total current into V_{DD} terminal . . . . . 45 mA
Total current out of ground terminal . . . . . 45 mA
Duration of short-circuit current at (or below) 25°C (see Note 4) . . . . . Unlimited
Continuous total dissipation . . . . . See Dissipation Rating Table
Operating free-air temperature, T_A: C-suffix types . . . . . 0°C to 70°C
I-suffix types . . . . . -40°C to 85°C
M-suffix types . . . . . -55°C to 125°C
Storage temperature range . . . . . -65°C to 150°C
Case temperature for 60 seconds: FK package . . . . . 260°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds: J package . . . . . 300°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: D and N package . . . . . 260°C

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25$°C POWER RATING	DERATING FACTOR ABOVE $T_A = 25$°C	$T_A = 70$°C POWER RATING	$T_A = 85$°C POWER RATING	$T_A = 125$°C POWER RATING
D	950 mW	7.6 mW/°C	608 mW	494 mW	
FK	1375 mW	11 mW/°C	880 mW	715 mW	275 mW
J (C-, I- suffix)	1025 mW	8.2 mW/°C	656 mW	533 mW	
J (M- suffix)	1375 mW	11 mW/°C	880 mW	715 mW	275 mW
N	1575 mW	12.6 mW/°C	1008 mW	819 mW	

recommended operating conditions

		M- SUFFIX TYPES			I- SUFFIX TYPES			C- SUFFIX TYPES			
		MIN	NOM	MAX	MIN	NOM	MAX	MIN	NOM	MAX	UNIT
Supply voltage, V_{DD}		4		16	4		16	3		16	V
Common-mode input voltage, V_{IC}	$V_{DD} = 5$ V	0		3.5	-0.2		3.5	-0.2		3.5	V
	$V_{DD} = 10$ V	0		8.5	-0.2		8.5	-0.2		8.5	V
Input voltage, V_I	$V_{DD} = 5$ V	0		3.5	-0.2		3.5	-0.2		3.5	V
	$V_{DD} = 10$ V	0		8.5	-0.2		8.5	-0.2		8.5	V
Operating free-air temperature, T_A		-55		125	-40		85	0		70	°C

NOTES: 2. All voltage values, except differential voltages, are with respect to network ground.
3. Differential voltages are at the noninverting input with respect to the inverting input.
4. The output may be shorted to either supply. Temperature and/or supply voltages must be limited to ensure that the maximum dissipation rating is not exceeded (see application section).

electrical characteristics at specified free-air temperature, V_{DD} = 5 V (unless otherwise noted)

PARAMETER			TEST CONDTIONS		C- SUFFIX TYPES MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage	TLC274C	V_O = 1.4 V, V_{IC} = 0 V, R_S = 50 Ω, R_L = 10 kΩ	25°C		1.1	10	mV
				Full range			12	
		TLC274AC	V_O = 1.4 V, V_{IC} = 0 V, R_S = 50 Ω, R_L = 10 kΩ	25°C		0.9	5	
				Full range			6.5	
		TLC274BC	V_O = 1.4 V, V_{IC} = 0 V, R_S = 50 Ω, R_L = 10 kΩ	25°C		340	2000	µV
				Full range			3000	
		TLC279C	V_O = 1.4 V, V_{IC} = 0 V, R_S = 50 Ω, R_L = 10 kΩ	25°C		320	900	
				Full range			1500	
α_{VIO}	Average temperature coefficient of input offset voltage			25°C to 70°C		1.8		µV/°C
I_{IO}	Input offset current (see Note 5)		V_{IC} = 2.5 V, V_O = 2.5 V	25°C		0.1		pA
				70°C		7	300	
I_{IB}	Input bias current (see Note 5)		V_{IC} = 2.5 V, V_O = 2.5 V	25°C		0.6		pA
				70°C		40	600	
V_{ICR}	Common-mode input voltage range (see Note 6)			25°C	−0.2 to 4	−0.3 to 4.2		V
				Full range	−0.2 to 3.5			V
V_{OH}	High-level output voltage		V_{ID} = 100 mV, R_L = 10 kΩ	25°C	3.2	3.8		V
				70°C	3	3.8		
				0°C	3	3.8		
V_{OL}	Low-level output voltage		V_{ID} = − 100 mV, I_{OL} = 0	25°C		0	50	mV
				70°C		0	50	
				0°C		0	50	
A_{VD}	Large-signal differential voltage amplification		V_O = 0.25 V to 2 V, R_L = 10 kΩ	25°C	5	23		V/mV
				70°C	4	20		
				0°C	4	27		
CMRR	Common-mode rejection ratio		V_{IC} = V_{ICR} min	25°C	65	80		dB
				70°C	60	85		
				0°C	60	84		
k_{SVR}	Supply-voltage rejection ratio (ΔV_{DD} / ΔV_{IO})		V_{DD} = 5 V to 10 V, V_O = 1.4 V	25°C	65	95		dB
				70°C	60	96		
				0°C	60	94		
I_{DD}	Supply current (four amplifiers)		No load, V_O = 2.5 V, V_{IC} = 2.5 V	25°C		2.7	6.4	mA
				70°C		2.3	5.2	
				0°C		3.1	7.2	

NOTES: 5. The typical values of input bias current and input offset current below 5 pA were determined mathematically.
6. This range also applies to each input individually.

electrical characteristics at specified free-air temperature, V_{DD} = 10 V (unless otherwise noted)

PARAMETER			TEST CONDTIONS		C- SUFFIX TYPES MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage	TLC274C	V_O = 1.4 V, V_{IC} = 0 V, R_S = 50 Ω, R_L = 10 kΩ	25°C		1.1	10	mV
				Full range			12	
		TLC274AC	V_O = 1.4 V, V_{IC} = 0 V, R_S = 50 Ω, R_L = 10 kΩ	25°C		0.9	5	
				Full range			6.5	
		TLC274BC	V_O = 1.4 V, V_{IC} = 0 V, R_S = 50 Ω, R_L = 10 kΩ	25°C		390	2000	μV
				Full range			3000	
		TLC279C	V_O = 1.4 V, V_{IC} = 0 V, R_S = 50 Ω, R_L = 10 kΩ	25°C		370	1200	
				Full range			1900	
α_{VIO}	Average temperature coefficient of input offset voltage			25°C to 70°C		2		μV/°C
I_{IO}	Input offset current (see Note 5)		V_{IC} = 5 V, V_O = 5 V	25°C		0.1		pA
				70°C		8	300	
I_{IB}	Input bias current (see Note 5)		V_{IC} = 5 V, V_O = 5 V	25°C		0.7		pA
				70°C		50	600	
V_{ICR}	Common-mode input voltage range (see Note 6)			25°C	−0.2 to 9	−0.3 to 9.2		V
				Full range	−0.2 to 8.5			V
V_{OH}	High-level output voltage		V_{ID} = 100 mV, R_L = 10 kΩ	25°C	8	8.5		V
				70°C	7.8	8.4		
				0°C	7.8	8.5		
V_{OL}	Low-level output voltage		V_{ID} = −100 mV, I_{OL} = 0	25°C		0	50	mV
				70°C		0	50	
				0°C		0	50	
A_{VD}	Large-signal differential voltage amplification		V_O = 1 V to 6 V, R_L = 10 kΩ	25°C	10	36		V/mV
				70°C	7.5	32		
				0°C	7.5	42		
CMRR	Common-mode rejection ratio		V_{IC} = V_{ICR} min	25°C	65	85		dB
				70°C	60	88		
				0°C	60	88		
k_{SVR}	Supply-voltage rejection ratio (ΔV_{DD} / ΔV_{IO})		V_{DD} = 5 V to 10 V, V_O = 1.4 V	25°C	65	95		dB
				70°C	60	96		
				0°C	60	94		
I_{DD}	Supply current (four amplifiers)		No load, V_O = 5 V, V_{IC} = 5 V	25°C		3.8	8	mA
				70°C		3	6.8	
				0°C		4.5	8.8	

NOTES: 5. The typical values of input bias current and input offset current below 5 pA were determined mathematically.
6. This range also applies to each input individually.

electrical characteristics at specified free-air temperature, V_{DD} = 5 V (unless otherwise noted)

PARAMETER			TEST CONDTIONS		I- SUFFIX TYPES MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage	TLC274I	V_O = 1.4 V, V_{IC} = 0 V, R_S = 50 Ω, R_L = 10 kΩ	25°C		1.1	10	mV
				Full range			13	
		TLC274AI	V_O = 1.4 V, V_{IC} = 0 V, R_S = 50 Ω, R_L = 10 kΩ	25°C		0.9	5	
				Full range			7	
		TLC274BI	V_O = 1.4 V, V_{IC} = 0 V, R_S = 50 Ω, R_L = 10 kΩ	25°C		340	2000	μV
				Full range			3500	
		TLC279I	V_O = 1.4 V, V_{IC} = 0 V, R_S = 50 Ω, R_L = 10 kΩ	25°C		320	900	
				Full range			2000	
α_{VIO}	Average temperature coefficient of input offset voltage			25°C to 85°C		1.8		μV/°C
I_{IO}	Input offset current (see Note 5)		V_{IC} = 2.5 V, V_O = 2.5 V	25°C		0.1		pA
				85°C		24	1000	
I_{IB}	Input bias current (see Note 5)		V_{IC} = 2.5 V, V_O = 2.5 V	25°C		0.6		pA
				85°C		200	2000	
V_{ICR}	Common-mode input voltage range (see Note 6)			25°C	−0.2 to 4	−0.3 to 4.2		V
				Full range	−0.2 to 3.5			V
V_{OH}	High-level output voltage		V_{ID} = 100 mV, R_L = 10 kΩ	25°C	3.2	3.8		V
				85°C	3	3.8		
				−40°C	3	3.8		
V_{OL}	Low-level output voltage		V_{ID} = −100 mV, I_{OL} = 0	25°C		0	50	mV
				85°C		0	50	
				−40°C		0	50	
A_{VD}	Large-signal differential voltage amplification		V_O = 0.25 V to 2 V, R_L = 10 kΩ	25°C	5	23		V/mV
				85°C	3.5	19		
				−40°C	3.5	32		
CMRR	Common-mode rejection ratio		V_{IC} = V_{ICR} min	25°C	65	80		dB
				85°C	60	86		
				−40°C	60	81		
k_{SVR}	Supply-voltage rejection ratio (ΔV_{DD} / ΔV_{IO})		V_{DD} = 5 V to 10 V, V_O = 1.4 V	25°C	65	95		dB
				85°C	60	96		
				−40°C	60	92		
I_{DD}	Supply current (four amplifiers)		No load, V_O = 2.5 V, V_{IC} = 2.5 V	25°C		2.7	6.4	mA
				85°C		2.1	4.8	
				−40°C		3.8	8.8	

NOTES: 5. The typical values of input bias current and input offset current below 5 pA were determined mathematically.
6. This range also applies to each input individually.

electrical characteristics at specified free-air temperature, V_{DD} = 10 V (unless otherwise noted)

PARAMETER			TEST CONDTIONS		I- SUFFIX TYPES MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage	TLC274I	V_O = 1.4 V, V_{IC} = 0 V, R_S = 50 Ω, R_L = 10 kΩ	25°C		1.1	10	mV
				Full range			13	
		TLC274AI	V_O = 1.4 V, V_{IC} = 0 V, R_S = 50 Ω, R_L = 10 kΩ	25°C		0.9	5	
				Full range			7	
		TLC274BI	V_O = 1.4 V, V_{IC} = 0 V, R_S = 50 Ω, R_L = 10 kΩ	25°C		390	2000	μV
				Full range			3500	
		TLC279I	V_O = 1.4 V, V_{IC} = 0 V, R_S = 50 Ω, R_L = 10 kΩ	25°C		370	1200	
				Full range			2900	
α_{VIO}	Average temperature coefficient of input offset voltage			25°C to 85°C		2		μV/°C
I_{IO}	Input offset current (see Note 5)		V_{IC} = 5 V, V_O = 5 V	25°C		0.1		pA
				85°C		26	1000	
I_{IB}	Input bias current (see Note 5)		V_{IC} = 5 V, V_O = 5 V	25°C		0.7		pA
				85°C		220	2000	
V_{ICR}	Common-mode input voltage range (see Note 6)			25°C	−0.2 to 9	−0.3 to 9.2		V
				Full range	−0.2 to 8.5			V
V_{OH}	High-level output voltage		V_{ID} = 100 mV, R_L = 10 kΩ	25°C	8	8.5		V
				85°C	7.8	8.5		
				−40°C	7.8	8.5		
V_{OL}	Low-level output voltage		V_{ID} = −100 mV, I_{OL} = 0	25°C		0	50	mV
				85°C		0	50	
				−40°C		0	50	
A_{VD}	Large-signal differential voltage amplification		V_O = 1 V to 6 V, R_L = 10 kΩ	25°C	10	36		V/mV
				85°C	7	31		
				−40°C	7	46		
CMRR	Common-mode rejection ratio		V_{IC} = V_{ICR} min	25°C	65	85		dB
				85°C	60	88		
				−40°C	60	87		
k_{SVR}	Supply-voltage rejection ratio (ΔV_{DD} / ΔV_{IO})		V_{DD} = 5 V to 10 V, V_O = 1.4 V	25°C	65	95		dB
				85°C	60	96		
				−40°C	60	92		
I_{DD}	Supply current (four amplifiers)		No load, V_O = 5 V, V_{IC} = 5 V	25°C		3.8	8	mA
				85°C		2.9	6.4	
				−40°C		5.5	10	

NOTES: 5. The typical values of input bias current and input offset current below 5 pA were determined mathematically.
6. This range also applies to each input individually.

electrical characteristics at specified free-air temperature, V_{DD} = 5 V (unless otherwise noted)

PARAMETER			TEST CONDTIONS		M- SUFFIX TYPES MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage	TLC274M	V_O = 1.4 V, V_{IC} = 0 V, R_S = 50 Ω, R_L = 10 kΩ	25°C		1.1	10	mV
				Full range			12	
		TLC279M	V_O = 1.4 V, V_{IC} = 0 V, R_S = 50 Ω, R_L = 10 kΩ	25°C		320	900	μV
				Full range			3750	
α_{VIO}	Average temperature coefficient of input offset voltage			25°C to 125°C		2.1		μV/°C
I_{IO}	Input offset current (see Note 5)		V_{IC} = 2.5 V, V_O = 2.5 V	25°C		0.1		pA
				125°C		1.4	15	nA
I_{IB}	Input bias current (see Note 5)		V_{IC} = 2.5 V, V_O = 2.5 V	25°C		0.6		pA
				125°C		9	35	nA
V_{ICR}	Common-mode input voltage range (see Note 6)			25°C	0.0 to 4	− 0.3 to 4.2		V
				Full range	0.0 to 3.5			V
V_{OH}	High-level output voltage		V_{ID} = 100 mV, R_L = 10 kΩ	25°C	3.2	3.8		V
				125°C	3	3.8		
				− 55°C	3	3.8		
V_{OL}	Low-level output voltage		V_{ID} = − 100 mV, I_{OL} = 0	25°C		0	50	mV
				125°C		0	50	
				− 55°C		0	50	
A_{VD}	Large-signal differential voltage amplification		V_O = 0.25 V to 2 V, R_L = 10 kΩ	25°C	5	23		V/mV
				125°C	3.5	16		
				− 55°C	3.5	35		
CMRR	Common-mode rejection ratio		V_{IC} = V_{ICR} min	25°C	65	80		dB
				125°C	60	84		
				− 55°C	60	81		
k_{SVR}	Supply-voltage rejection ratio (ΔV_{DD} / ΔV_{IO})		V_{DD} = 5 V to 10 V, V_O = 1.4 V	25°C	65	95		dB
				125°C	60	97		
				− 55°C	60	90		
I_{DD}	Supply current (four amplifiers)		No load, V_O = 2.5 V, V_{IC} = 2.5 V	25°C		2.7	6.4	mA
				125°C		1.9	4.4	
				− 55°C		4	10	

NOTES: 5. The typical values of input bias current and input offset current below 5 pA were determined mathematically.
6. This range also applies to each input individually.

electrical characteristics at specified free-air temperature, V_{DD} = 10 V (unless otherwise noted)

PARAMETER			TEST CONDTIONS		M- SUFFIX TYPES MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage	TLC274M	V_O = 1.4 V, V_{IC} = 0 V, R_S = 50 Ω, R_L = 10 kΩ	25°C		1.1	10	mV
				Full range			12	
		TLC279M	V_O = 1.4 V, V_{IC} = 0 V, R_S = 50 Ω, R_L = 10 kΩ	25°C		370	1200	μV
				Full range			4300	
α_{VIO}	Average temperature coefficient of input offset voltage			25°C to 125°C		2.2		μV/°C
I_{IO}	Input offset current (see Note 5)		V_{IC} = 5 V, V_O = 5 V	25°C		0.1		pA
				125°C		1.8	15	nA
I_{IB}	Input bias current (see Note 5)		V_{IC} = 5 V, V_O = 5 V	25°C		0.7		pA
				125°C		10	35	nA
V_{ICR}	Common-mode input voltage range (see Note 6)			25°C	0.0 to 9	−0.3 to 9.2		V
				Full range	0.0 to 8.5			V
V_{OH}	High-level output voltage		V_{ID} = 100 mV, R_L = 10 kΩ	25°C	8	8.5		V
				125°C	7.8	8.4		
				−55°C	7.8	8.5		
V_{OL}	Low-level output voltage		V_{ID} = −100 mV, I_{OL} = 0	25°C		0	50	mV
				125°C		0	50	
				−55°C		0	50	
A_{VD}	Large-signal differential voltage amplification		V_O = 1 V to 6 V, R_L = 10 kΩ	25°C	10	36		V/mV
				125°C	7	27		
				−55°C	7	50		
CMRR	Common-mode rejection ratio		V_{IC} = V_{ICR} min	25°C	65	85		dB
				125°C	60	86		
				−55°C	60	87		
k_{SVR}	Supply-voltage rejection ratio (ΔV_{DD} / ΔV_{IO})		V_{DD} = 5 V to 10 V, V_O = 1.4 V	25°C	65	95		dB
				125°C	60	97		
				−55°C	60	90		
I_{DD}	Supply current (four amplifiers)		No load, V_O = 5 V, V_{IC} = 5 V	25°C		3.8	8	mA
				125°C		2.5	5.6	
				−55°C		5.9	12	

NOTES: 5. The typical values of input bias current and input offset current below 5 pA were determined mathematically.
6. This range also applies to each input individually.

operating characteristics, V_{DD} = 5 V

PARAMETER		TEST CONDTIONS			C- SUFFIX TYPES MIN	C- SUFFIX TYPES TYP	C- SUFFIX TYPES MAX	UNIT
SR	Slew rate at unity gain	R_L = 10 kΩ, C_L = 20 pF, See Figure 1	V_{IPP} = 1 V	25°C		3.6		V/μs
				70°C		3		
				0°C		3.9		
			V_{IPP} = 2.5 V	25°C		2.9		
				70°C		2.5		
				0°C		3.1		
V_n	Equivalent input noise voltage	f = 1 kHz, R_S = 100 Ω, See Figure 2		25°C		25		nV/√Hz
B_{OM}	Maximum output swing bandwidth	V_O = V_{OH}, C_L = 20 pF, R_L = 10 kΩ, See Figure 1		25°C		320		kHz
				70°C		260		
				0°C		340		
B_1	Unity-gain bandwidth	V_i = 10 mV, C_L = 20 pF, See Figure 3		25°C		1.7		MHz
				70°C		1.3		
				0°C		2		
ϕ_m	Phase margin	f = B_1, V_i = 10 mV, C_L = 20 pF, See Figure 3		25°C		46°		
				70°C		43°		
				0°C		47°		

operating characteristics, V_{DD} = 10 V

PARAMETER		TEST CONDTIONS			C- SUFFIX TYPES MIN	C- SUFFIX TYPES TYP	C- SUFFIX TYPES MAX	UNIT
SR	Slew rate at unity gain	R_L = 10 kΩ, C_L = 20 pF, See Figure 1	V_{IPP} = 1 V	25°C		5.3		V/μs
				70°C		4.3		
				0°C		5.9		
			V_{IPP} = 5.5 V	25°C		4.6		
				70°C		3.8		
				0°C		5.1		
V_n	Equivalent input noise voltage	f = 1 kHz, R_S = 100 Ω, See Figure 2		25°C		25		nV/√Hz
B_{OM}	Maximum output swing bandwidth	V_O = V_{OH}, C_L = 20 pF, R_L = 10 kΩ, See Figure 1		25°C		200		kHz
				70°C		140		
				0°C		220		
B_1	Unity-gain bandwidth	V_i = 10 mV, C_L = 20 pF, See Figure 3		25°C		2.2		MHz
				70°C		1.8		
				0°C		2.5		
ϕ_m	Phase margin	f = B_1, V_i = 10 mV, C_L = 20 pF, See Figure 3		25°C		49°		
				70°C		46°		
				0°C		50°		

operating characteristics, V_{DD} = 5 V

PARAMETER		TEST CONDTIONS			I- SUFFIX TYPES MIN	TYP	MAX	UNIT
SR	Slew rate at unity gain	R_L = 10 kΩ, C_L = 20 pF, See Figure 1	V_{IPP} = 1 V	25°C		3.6		V/μs
				85°C		2.8		
				– 40°C		4.5		
			V_{IPP} = 2.5 V	25°C		2.9		
				85°C		2.3		
				– 40°C		3.5		
V_n	Equivalent input noise voltage	f = 1 kHz, R_S = 100 Ω, See Figure 2		25°C		25		nV/√Hz
B_{OM}	Maximum output swing bandwidth	V_O = V_{OH}, C_L = 20 pF, R_L = 10 kΩ, See Figure 1		25°C		320		kHz
				85°C		250		
				– 40°C		380		
B_1	Unity-gain bandwidth	V_i = 10 mV, C_L = 20 pF, See Figure 3		25°C		1.7		MHz
				85°C		1.2		
				– 40°C		2.6		
ϕ_m	Phase margin	f = B_1, V_i = 10 mV, C_L = 20 pF, See Figure 3		25°C		46°		
				85°C		43°		
				– 40°C		49°		

operating characteristics, V_{DD} = 10 V

PARAMETER		TEST CONDTIONS			I- SUFFIX TYPES MIN	TYP	MAX	UNIT
SR	Slew rate at unity gain	R_L = 10 kΩ, C_L = 20 pF, See Figure 1	V_{IPP} = 1 V	25°C		5.3		V/μs
				85°C		4		
				– 40°C		6.7		
			V_{IPP} = 5.5 V	25°C		4.6		
				85°C		3.5		
				– 40°C		5.8		
V_n	Equivalent input noise voltage	f = 1 kHz, R_S = 100 Ω, See Figure 2		25°C		25		nV/√Hz
B_{OM}	Maximum output swing bandwidth	V_O = V_{OH}, C_L = 20 pF, R_L = 10 kΩ, See Figure 1		25°C		200		kHz
				85°C		130		
				– 40°C		260		
B_1	Unity-gain bandwidth	V_i = 10 mV, C_L = 20 pF, See Figure 3		25°C		2.2		MHz
				85°C		1.7		
				– 40°C		3.1		
ϕ_m	Phase margin	f = B_1, V_i = 10 mV, C_L = 20 pF, See Figure 3		25°C		49°		
				85°C		46°		
				– 40°C		52°		

operating characteristics, V_{DD} = 5 V

PARAMETER		TEST CONDTIONS			M- SUFFIX TYPES MIN	TYP	MAX	UNIT
SR	Slew rate at unity gain	R_L = 10 kΩ, C_L = 20 pF, See Figure 1	V_{IPP} = 1 V	25°C		3.6		V/μs
				125°C		2.3		
				– 55°C		4.7		
			V_{IPP} = 2.5 V	25°C		2.9		
				125°C		2		
				– 55°C		3.7		
V_n	Equivalent input noise voltage	f = 1 kHz, R_S = 100 Ω, See Figure 2		25°C		25		nV/√Hz
B_{OM}	Maximum output swing bandwidth	$V_O = V_{OH}$, C_L = 20 pF, R_L = 10 kΩ, See Figure 1		25°C		320		kHz
				125°C		230		
				– 55°C		400		
B_1	Unity-gain bandwidth	V_i = 10 mV, C_L = 20 pF, See Figure 3		25°C		1.7		MHz
				125°C		1.1		
				– 55°C		2.9		
ϕ_m	Phase margin	f = B_1, V_i = 10 mV, C_L = 20 pF, See Figure 3		25°C		46°		
				125°C		41°		
				– 55°C		49°		

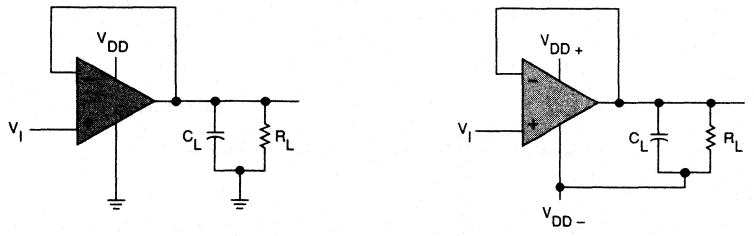
operating characteristics, V_{DD} = 10 V

PARAMETER		TEST CONDTIONS			M- SUFFIX TYPES MIN	TYP	MAX	UNIT
SR	Slew rate at unity gain	R_L = 10 kΩ, C_L = 20 pF, See Figure 1	V_{IPP} = 1 V	25°C		5.3		V/μs
				125°C		3.1		
				– 55°C		7.1		
			V_{IPP} = 5.5 V	25°C		4.6		
				125°C		2.7		
				– 55°C		6.1		
V_n	Equivalent input noise voltage	f = 1 kHz, R_S = 100 Ω, See Figure 2		25°C		25		nV/√Hz
B_{OM}	Maximum output swing bandwidth	$V_O = V_{OH}$, C_L = 20 pF, R_L = 10 kΩ, See Figure 1		25°C		200		kHz
				125°C		110		
				– 55°C		280		
B_1	Unity-gain bandwidth	V_i = 10 mV, C_L = 20 pF, See Figure 3		25°C		2.2		MHz
				125°C		1.6		
				– 55°C		3.4		
ϕ_m	Phase margin	f = B_1, V_i = 10 mV, C_L = 20 pF, See Figure 3		25°C		49°		
				125°C		44°		
				– 55°C		52°		

PARAMETER MEASUREMENT INFORMATION

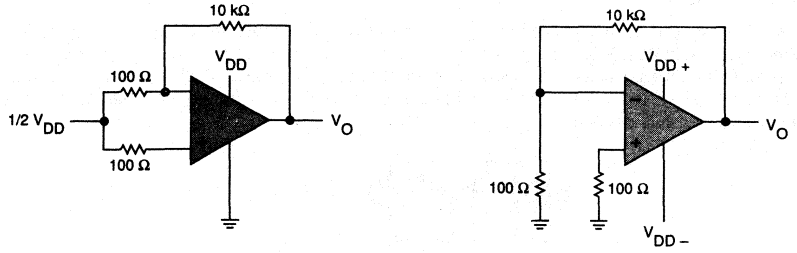
single-supply versus split-supply test circuits

Because the TLC274 and TLC279 are optimized for single-supply operation, circuit configurations used for the various tests often present some inconvenience since the input signal, in many cases, must be offset from ground. This inconvenience can be avoided by testing the device with split supplies and the output load tied to the negative rail. A comparison of single-supply versus split-supply test circuits is shown below. The use of either circuit will give the same result.



(a) Single-Supply (b) Split-Supply

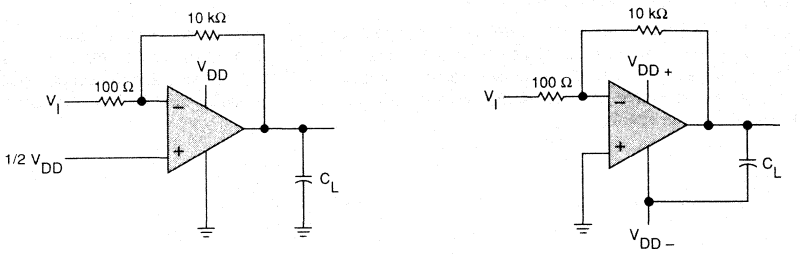
FIGURE 1. UNITY-GAIN AMPLIFIER



(a) Single-Supply (b) Split-Supply

FIGURE 2. NOISE TEST CIRCUIT

PARAMETER MEASUREMENT INFORMATION



(a) Single-Supply (b) Split-Supply

FIGURE 3. GAIN-OF-100 INVERTING AMPLIFIER

input bias current

Because of the high input impedance of the TLC274 and TLC279 op amps, attempts to measure the input bias current can result in erroneous readings. The typical bias current at normal room ambient temperature is typically less than 1 pA, a value that is easily exceeded by leakages on the test socket. Two suggestions are offered to avoid erroneous measurements:

1 Isolate the device from other potential leakage sources. This can be achieved by using a grounded shield around and between the device inputs (see Figure 4). Leakages that would otherwise flow to the inputs will be shunted away.

2 Compensate for the leakage of the test socket. This can be achieved by actually performing an input bias current test (using a picoammeter) with no device in the test socket. The actual input bias current can then be calculated by subtracting the "open-socket" leakage readings from the readings obtained with a device in the test socket.

One word of caution . . . many automatic testers as well as some bench-top op amp testers use the servo-loop technique with a resistor in series with the device input to measure the input bias current (the voltage drop across the series resistor is measured and the bias current is calculated). This method requires that a device be inserted into the test socket to obtain a correct reading; therefore, an "open-socket" reading is not feasible using this method.

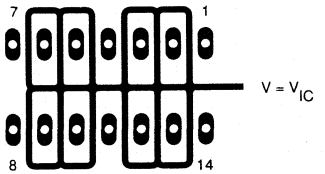


FIGURE 4. ISOLATION METAL AROUND DEVICE INPUTS
(N AND J DUAL-IN-LINE PACKAGE)

low-level output voltage

To obtain low-supply-voltage operation, some compromise was necessary in the input stage. This compromise results in the device low-level output being dependent on both the common-mode input voltage level as well as the differential input voltage level. When attempting to correlate low-level output readings with those quoted in the electrical specifications, these two conditions should be observed. If conditions other than these are to be used, please refer to Figures 14 thru 19 in the Typical Characteristics section of this data sheet.

input offset voltage temperature coefficient

Erroneous readings often result from attempts to measure temperature coefficient of input offset voltage. This parameter is actually a calculation using input offset voltage measurements obtained at two different temperatures. When one (or both) of the temperatures is below freezing, moisture can collect on both the device and the test socket. This moisture will result in leakage and contact resistance which can cause erroneous input offset voltage readings. The isolation techniques previously mentioned have no affect on the leakage since the moisture also covers the isolation metal itself, thereby rendering it useless. It is suggested that these measurements be performed at temperatures above freezing to minimize error.

full power response

Full power response, the frequency above which the op amp slew rate limits the output voltage swing, is often specified two ways . . . full-linear response and full-peak response. The full-linear response is generally measured by monitoring the distortion level of the output while increasing the frequency of a sinusoidal input signal until the maximum frequency is found above which the output contains significant distortion. The full-peak response is defined as the maximum output frequency, without regard to distortion, above which full peak-to-peak output swing cannot be maintained.

Because there is no industry-wide accepted value for "significant" distortion, the full peak response is specified in this data sheet and is measured using the circuit of Figure 1. The initial setup involves the use of a sinusoidal input to determine the maximum peak-to-peak output of the device (the amplitude of the sinusoidal wave is increased until clipping occurs). The sinusoidal wave is then replaced with a square wave of the same amplitude. The frequency is then increased until the maximum peak-to-peak output can no longer be maintained (Figure 5). A square wave is used to allow a more accurate determination of the point at which the maximum peak-to-peak output is reached.

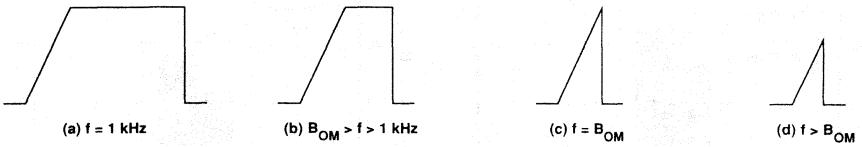


FIGURE 5. FULL-POWER-RESPONSE OUTPUT SIGNAL

test time

Inadequate test time is a frequent problem, especially when testing CMOS devices in a high-volume, short-test-time environment. Internal capacitances are inherently higher in CMOS than in bipolar and BiFET devices, and require longer test times than their bipolar and BiFET counterparts. The problem becomes more pronounced with reduced supply levels and lower temperatures.

TYPICAL CHARACTERISTICS

DISTRIBUTION OF TLC274
INPUT OFFSET VOLTAGE

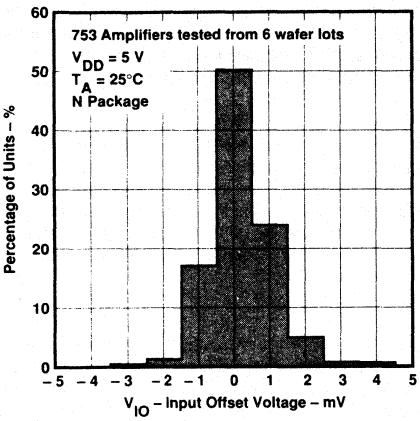


FIGURE 6

DISTRIBUTION OF TLC274
INPUT OFFSET VOLTAGE

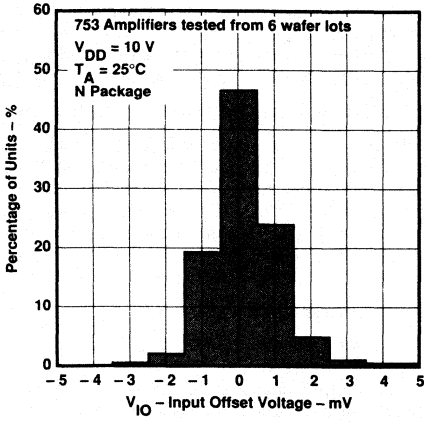


FIGURE 7

DISTRIBUTION OF TLC274 AND TLC279
INPUT OFFSET VOLTAGE
TEMPERATURE COEFFICIENT

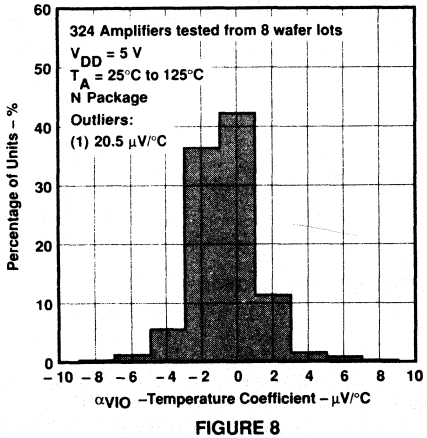


FIGURE 8

DISTRIBUTION OF TLC274 AND TLC279
INPUT OFFSET VOLTAGE
TEMPERATURE COEFFICIENT

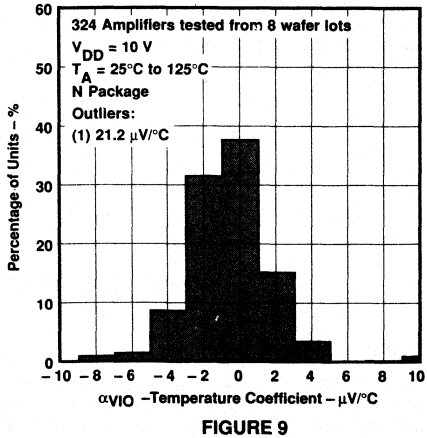


FIGURE 9

TYPICAL CHARACTERISTICS

HIGH-LEVEL OUTPUT VOLTAGE
vs
HIGH-LEVEL OUTPUT CURRENT

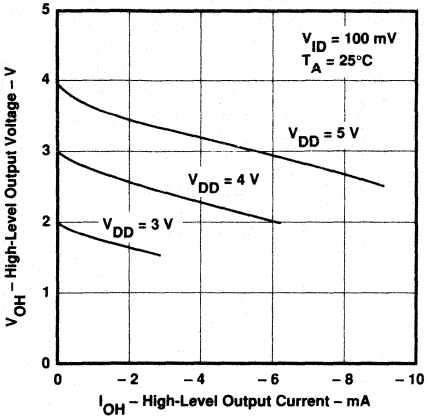


FIGURE 10

HIGH-LEVEL OUTPUT VOLTAGE
vs
HIGH-LEVEL OUTPUT CURRENT

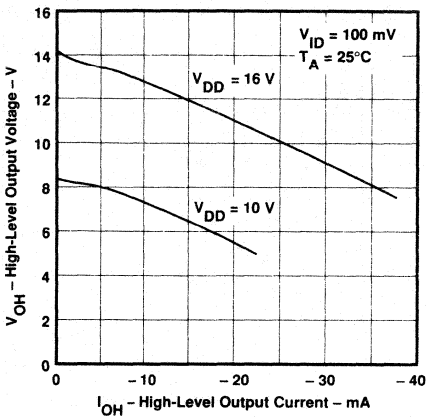


FIGURE 11

HIGH-LEVEL OUTPUT VOLTAGE
vs
SUPPLY VOLTAGE

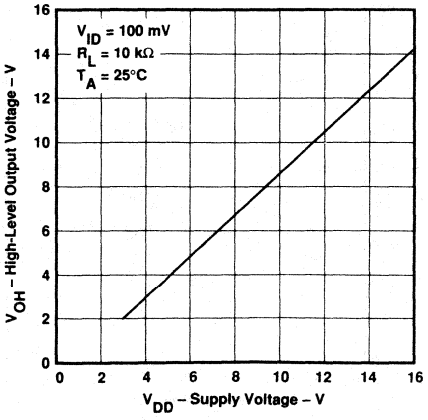


FIGURE 12

HIGH-LEVEL OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE

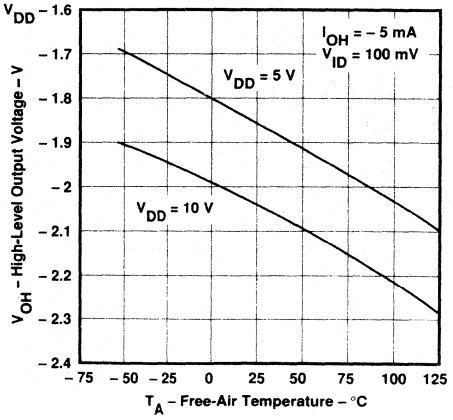


FIGURE 13

TYPICAL CHARACTERISTICS

LOW-LEVEL OUTPUT VOLTAGE
vs
COMMON-MODE INPUT VOLTAGE

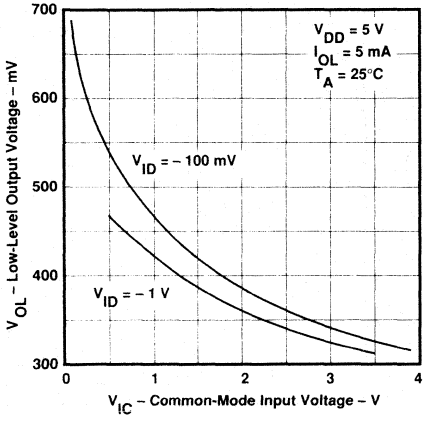


FIGURE 14

LOW-LEVEL OUTPUT VOLTAGE
vs
COMMON-MODE INPUT VOLTAGE

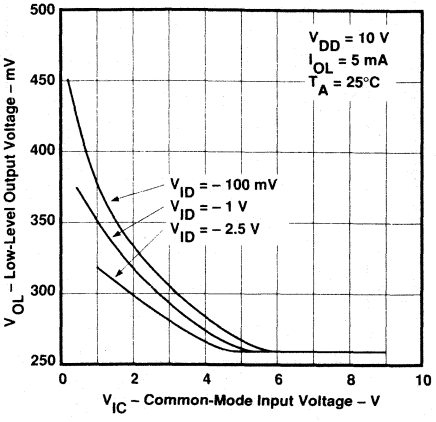


FIGURE 15

LOW-LEVEL OUTPUT VOLTAGE
vs
DIFFERENTIAL INPUT VOLTAGE

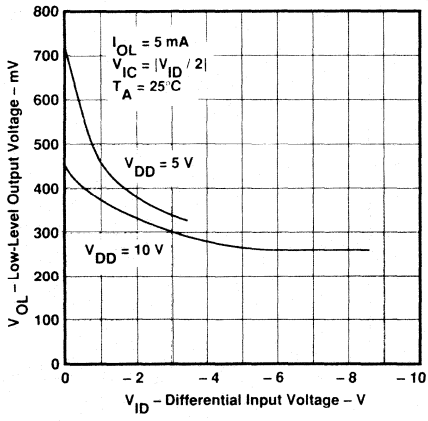


FIGURE 16

LOW-LEVEL OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE

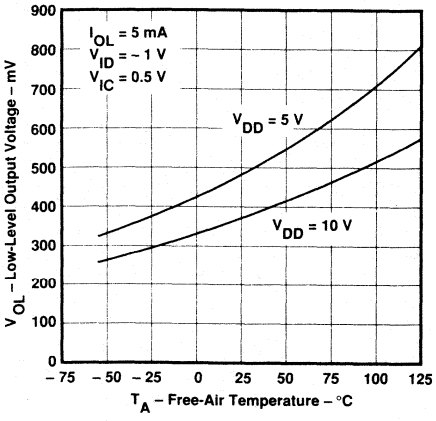


FIGURE 17

TYPICAL CHARACTERISTICS

LOW-LEVEL OUTPUT VOLTAGE
vs
LOW-LEVEL OUTPUT CURRENT

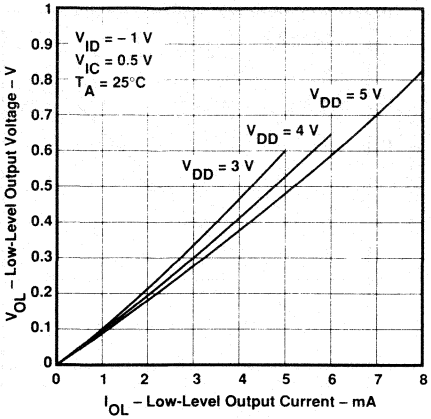


FIGURE 18

LOW-LEVEL OUTPUT VOLTAGE
vs
LOW-LEVEL OUTPUT CURRENT

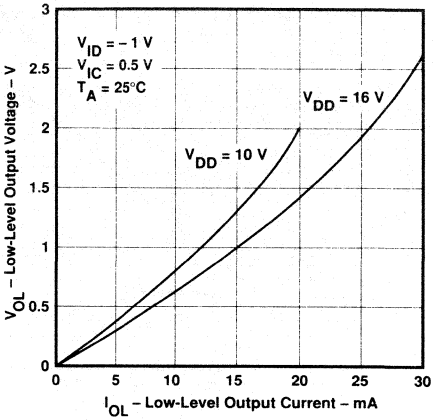


FIGURE 19

LARGE-SIGNAL
DIFFERENTIAL VOLTAGE AMPLIFICATION
vs
SUPPLY VOLTAGE

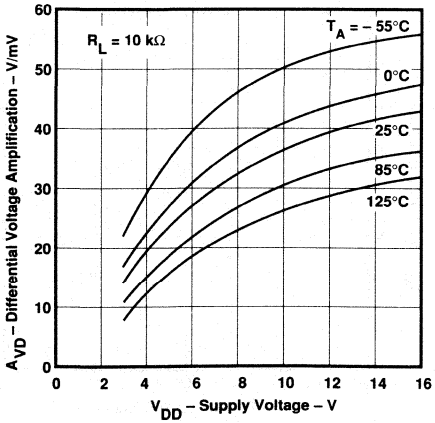


FIGURE 20

LARGE-SIGNAL
DIFFERENTIAL VOLTAGE AMPLIFICATION
vs
FREE-AIR TEMPERATURE

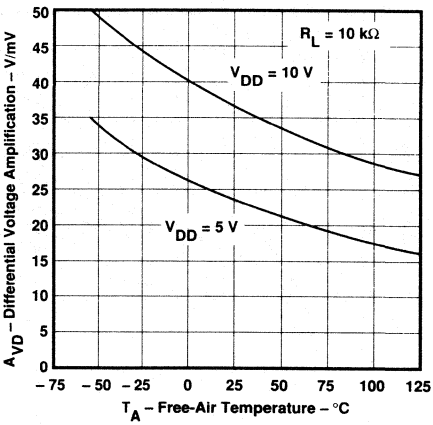


FIGURE 21

TYPICAL CHARACTERISTICS

INPUT BIAS CURRENT AND INPUT OFFSET CURRENT
vs
FREE-AIR TEMPERATURE

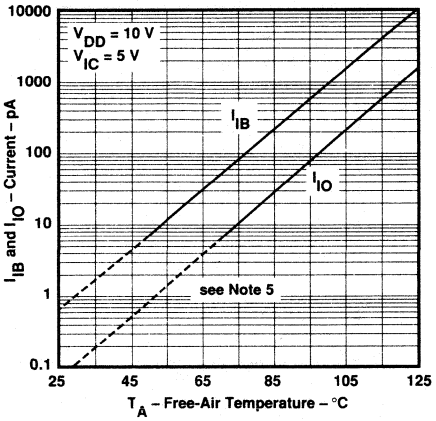


FIGURE 22

MAXIMUM INPUT VOLTAGE
vs
SUPPLY VOLTAGE

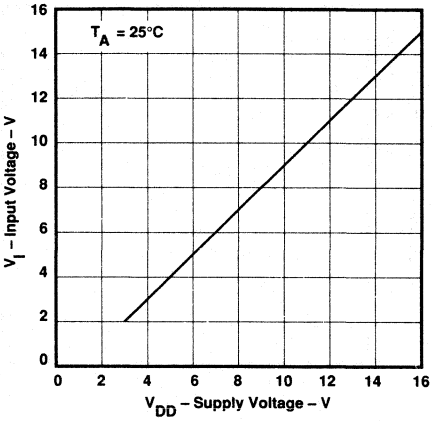


FIGURE 23

SUPPLY CURRENT
vs
SUPPLY VOLTAGE

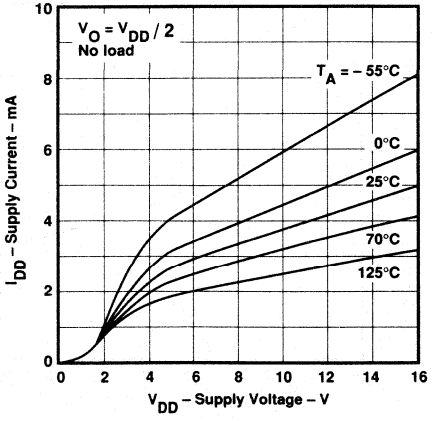


FIGURE 24

SUPPLY CURRENT
vs
FREE-AIR TEMPERATURE

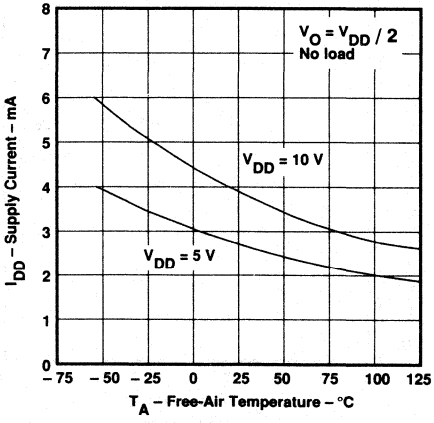


FIGURE 25

NOTE 5: The typical values of input bias current and input offset current below 5 pA were determined mathematically.

TYPICAL CHARACTERISTICS

SLEW RATE
vs
SUPPLY VOLTAGE

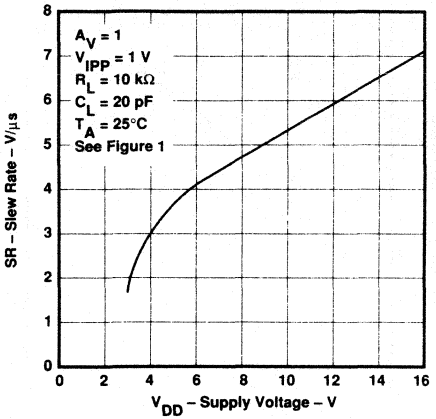


FIGURE 26

SLEW RATE
vs
FREE-AIR TEMPERATURE

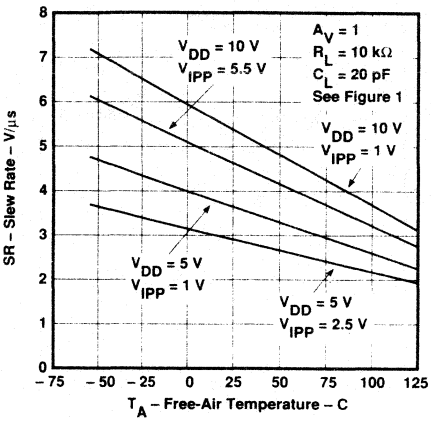


FIGURE 27

NORMALIZED SLEW RATE
vs
FREE-AIR TEMPERATURE

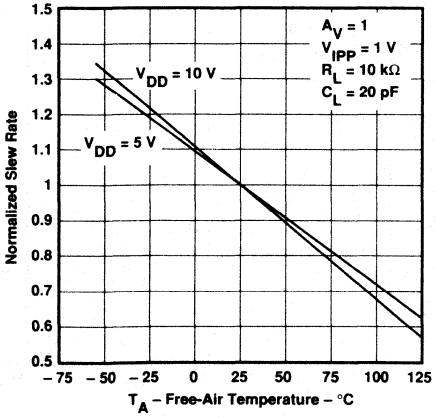


FIGURE 28

MAXIMUM PEAK-TO-PEAK OUTPUT VOLTAGE
vs
FREQUENCY

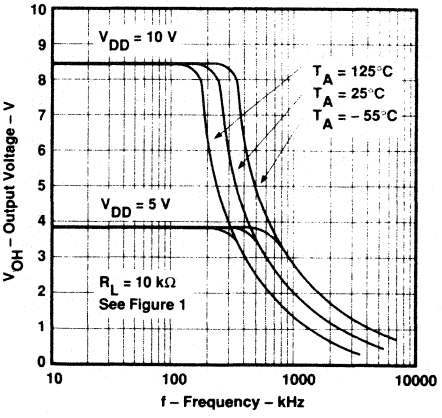


FIGURE 29

TYPICAL CHARACTERISTICS

UNITY-GAIN BANDWIDTH
vs
FREE-AIR TEMPERATURE

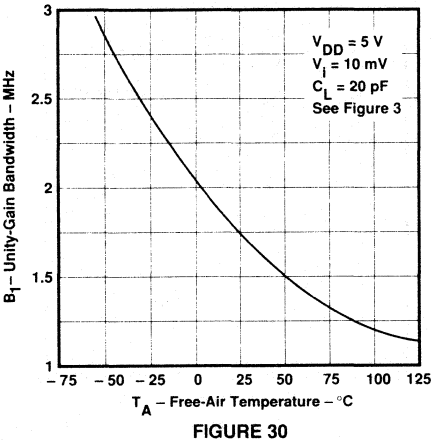


FIGURE 30

UNITY-GAIN BANDWIDTH
vs
SUPPLY VOLTAGE

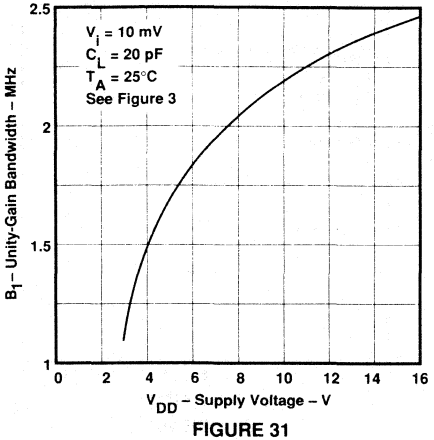


FIGURE 31

LARGE-SIGNAL DIFFERENTIAL VOLTAGE
AMPLIFICATION AND PHASE SHIFT
vs
FREQUENCY

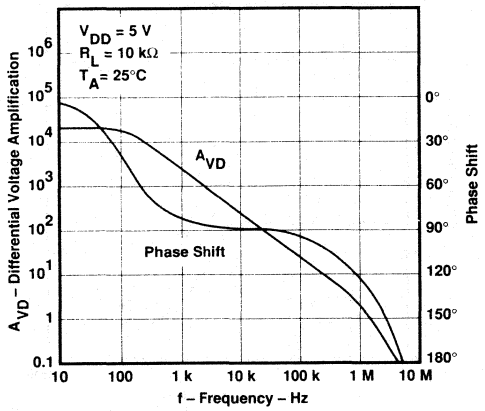


FIGURE 32

LARGE-SIGNAL DIFFERENTIAL VOLTAGE
AMPLIFICATION AND PHASE SHIFT
vs
FREQUENCY

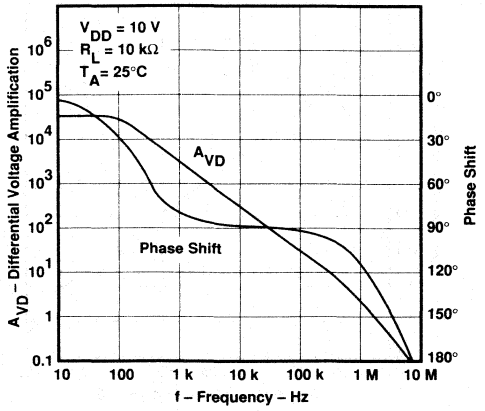


FIGURE 33

TYPICAL CHARACTERISTICS

PHASE MARGIN
vs
SUPPLY VOLTAGE

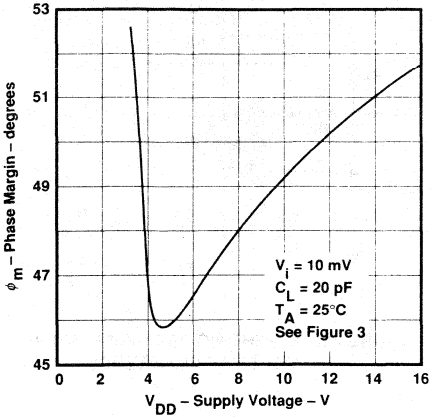


FIGURE 34

PHASE MARGIN
vs
FREE-AIR TEMPERATURE

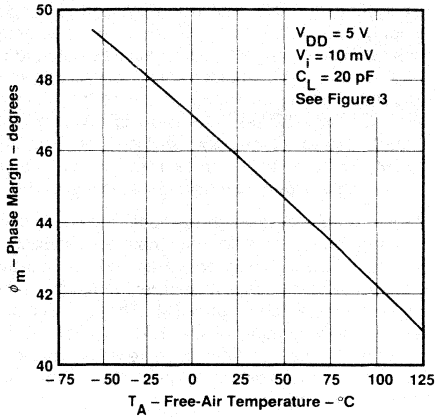


FIGURE 35

PHASE MARGIN
vs
CAPACITIVE LOAD

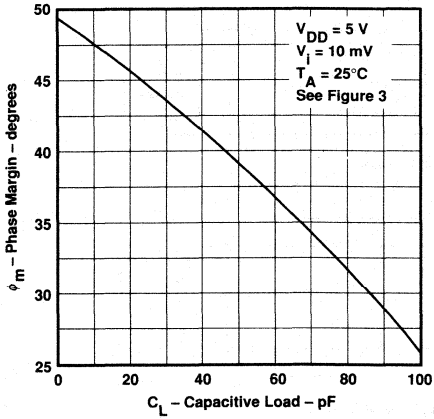


FIGURE 36

EQUIVALENT INPUT NOISE VOLTAGE
vs
FREQUENCY

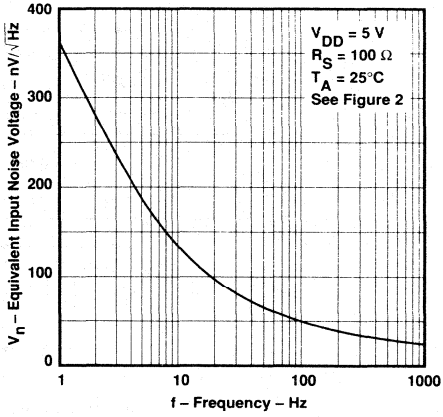


FIGURE 37

TYPICAL APPLICATION DATA

single-supply operation

While the TLC274 and TLC279 will perform well using dual power supplies (also called balanced or split supplies), the design is optimized for single-supply operation. This includes an input common mode voltage range that encompasses ground as well as an output voltage range that pulls down to ground. The supply voltage range extends down to 3 V (C- suffix types), thus allowing operation with supply levels commonly available for TTL and HCMOS; however, for maximum dynamic range, 16-V single-supply operation is recommended.

Many single-supply applications require that a voltage be applied to one input to establish a reference level that is above ground. A resistive voltage divider is usually sufficient to establish this reference level (see Figure 38). The low input bias current consumption of the TLC274 and TLC279 permits the use of very large resistive values to implement the voltage divider, thus minimizing power consumption.

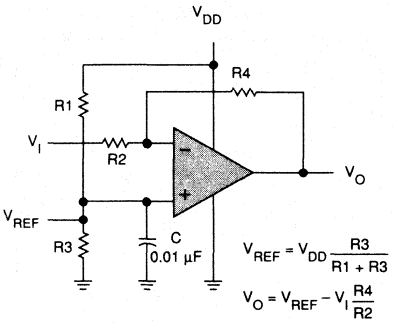
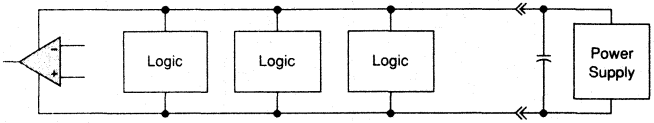


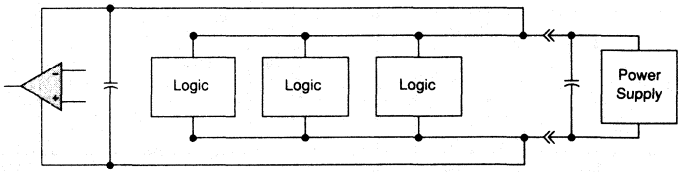
FIGURE 38. INVERTING AMPLIFIER WITH VOLTAGE REFERENCE

The TLC274 and TLC279 work well in conjunction with digital logic; however, when powering both linear devices and digital logic from the same power supply, the following precautions are recommended:

1. Power the linear devices from separate bypassed supply lines (see Figure 39); otherwise the linear device supply rails can fluctuate due to voltage drops caused by high switching currents in the digital logic.
2. Use proper bypass techniques to reduce the probability of noise-induced errors. Single capacitive decoupling is often adequate; however, RC decoupling may be necessary in high-frequency applications.



(a) Common Supply Rails



(b) Separate Bypassed Supply Rails (preferred)

FIGURE 39. COMMON VERSUS SEPARATE SUPPLY RAILS

TYPICAL APPLICATION DATA

input characteristics

The TLC274 and TLC279 are specified with a minimum and a maximum input voltage that, if exceeded at either input, could cause the device to malfunction. Exceeding this specified range is a common problem, especially in single-supply operation. Note that the lower range limit includes the negative rail, while the upper range limit is specified at V_{DD}– 1 V at T_A = 25°C and at V_{DD}– 1.5 V at all other temperatures.

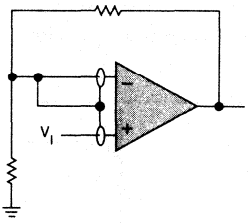
The use of the polysilicon-gate process and the careful input circuit design gives the TLC274 and TLC279 very good input offset voltage drift characteristics relative to conventional metal-gate processes. Offset voltage drift in CMOS devices is highly influenced by threshold voltage shifts caused by polarization of the phosphorus dopant implanted in the oxide. Placing the phosphorus dopant in a conductor (such as a polysilicon gate) alleviates the polarization problem, thus reducing threshold voltage shifts by more than an order of magnitude. The offset voltage drift with time has been calculated to be typically 0.1 μV/month, including the first month of operation.

Because of the extremely high input impedance and resulting low bias current requirements, the TLC274 and TLC279 are well suited for low-level signal processing; however, leakage currents on printed circuit boards and sockets can easily exceed bias current requirements and cause a degradation in device performance. It is good practice to include guard rings around inputs (similar to those of Figure 4 in the PARAMETER MEASUREMENT INFORMATION section). These guards should be driven from a low-impedance source at the same voltage level as the common-mode input (see Figure 40).

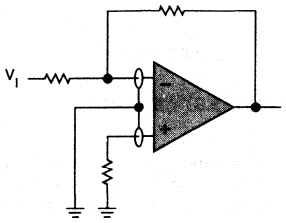
The inputs of any unused amplifiers should be tied to ground to avoid possible oscillation.

noise performance

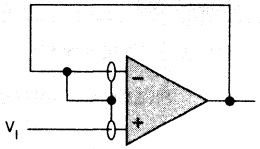
The noise specifications in op amp circuits are greatly dependent on the current in the first-stage differential amplifier. The low input bias current requirements of the TLC274 and TLC279 result in a very low noise current, which is insignificant in most applications. This feature makes the devices especially favorable over bipolar devices when using values of circuit impedance greater than 50 kΩ, since bipolar devices exhibit greater noise currents.



(a) Noninverting Ampilfier



(b) Inverting Amplifier



(c) Unity Gain Ampilfier

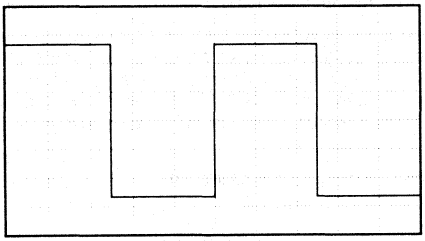
Figure 40. GUARD RING SCHEMES

TYPICAL APPLICATION DATA

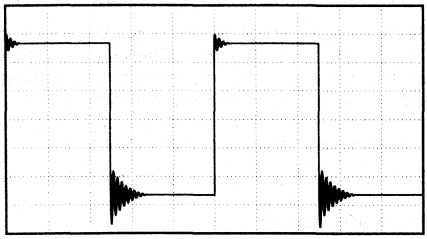
output characteristics

The output stage of the TLC274 and TLC279 is designed to sink and source relatively high amounts of current (see typical characteristics). If the output is subjected to a short-circuit condition, this high current capability can cause device damage under certain conditions. Output current capability increases with supply voltage.

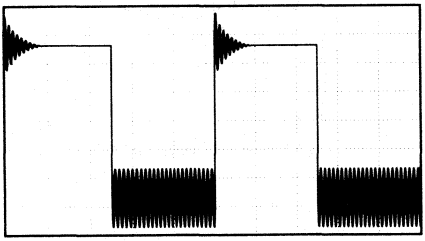
All operating characteristics of the TLC274 and TLC279 were measured using a 20-pF load. The devices will drive higher capacitive loads; however, as output load capacitance increases, the resulting response pole occurs at lower frequencies, thereby causing ringing, peaking, or even oscillation (see Figure 41). In many cases, adding some compensation in the form of a series resistor in the feedback loop will alleviate the problem.



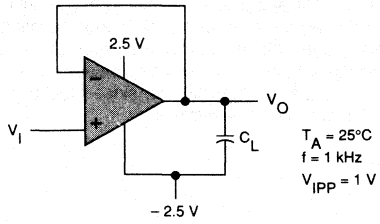
(a) C_L = 20 pF, R_L = no load



(b) C_L = 130 pF, R_L = no load



(c) C_L = 150 pF, R_L = no load



(d) Test Circuit

FIGURE 41. EFFECT OF CAPACITIVE LOADS AND TEST CIRCUIT

Although the TLC274 and TLC279 possess excellent high-level output voltage and current capability, methods are available for boosting this capability, if needed. The simplest method involves the use of a pullup resistor connected from the output to the positive supply rail. There are two disadvantages to the use of this circuit. First, the NMOS pull-down transistor, N4 (see Figure 42) must sink a comparatively large amount of current. In this circuit, N4 behaves like a linear resistor with an on resistance between approximately 60 Ω and 180 Ω, depending on how hard the op amp input is driven. With very low values of R6, a voltage offset from 0 V at the output will occur. Secondly, pullup resistor R6 acts as a drain load to N4 and the gain of the opamp is reduced at output voltage levels where N5 is not supplying the output current.

TYPICAL APPLICATION DATA

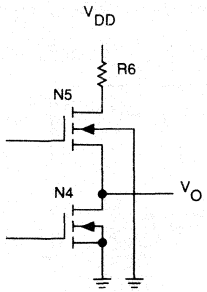


FIGURE 42. TLC274 / TLC279 OUTPUT STAGE

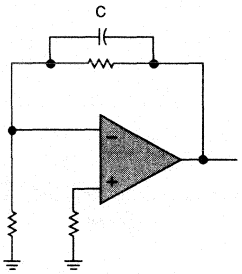


FIGURE 43. COMPENSATION FOR INPUT CAPACITANCE

feedback

Op amp circuits nearly always employ feedback, and since feedback is the first prerequsite for oscillation, a little caution is appropriate. Most oscillation problems result from driving capactive loads (discussed previously) and ignoring stray input capacitance. A small-value capacitor connected in parallel with the feedback resistor is an effective remedy (see Figure 43). The value of this capacitor is optimized empirically.

electrostatic discharge protection

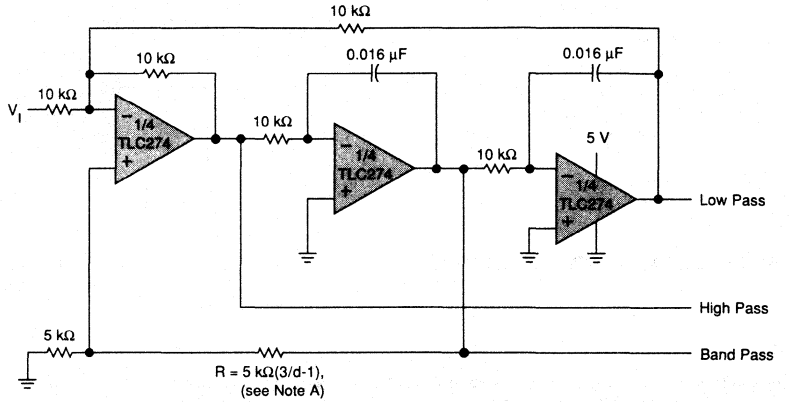
The TLC274 and TLC279 incorporate an internal electrostatic discharge (ESD) protection circuit that will prevent functional failures at voltages at or below 2000 V as tested under MIL-STD-883C, Method 3015.2. Care should be exercised, however, when handling these devices as exposure to ESD may result in the degradation of the device parametric performance. The protect circuit also causes the input bias currents to be temperature dependent and have the characteristics of a reverse-biased diode.

latchup

Because CMOS devices are susceptible to latchup due to their inherent parasitic thyristors, the TLC274 and TLC279 inputs and outputs were designed to withstand −100-mA surge currents without sustaining latchup; however, techniques should be used to reduce the chance of latchup whenever possible. Internal protection diodes should not by design be forward biased. Applied input and output voltage should not exceed the supply voltage by more than 300 mV. Care should be exercised when using capacitive coupling on pulse generators. Supply transients should be shunted by the use of decoupling capacitors (0.1 μF typical) located across the supply rails as close to the device as is possible.

The current path established if latchup occurs is usually between the positive supply rail and ground and can be triggered by surges on the supply lines and / or voltages on either the output or inputs that exceed the supply voltage. Once latchup occurs, the current flow is limited only by the impedance of the power supply and the forward resistance of the parasitic thyristor and usually results in the destruction of the device. The chance of latchup occuring increases with increasing temperature and supply voltages.

TYPICAL APPLICATION DATA



NOTES: A. d = damping factor, 1/Q
B. Normalized to 10 kΩ and f_C = 1 kHz

FIGURE 44. STATE VARIABLE FILTER

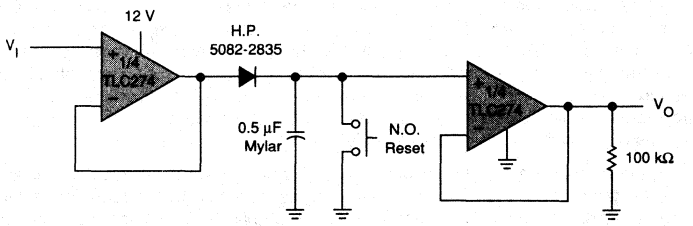
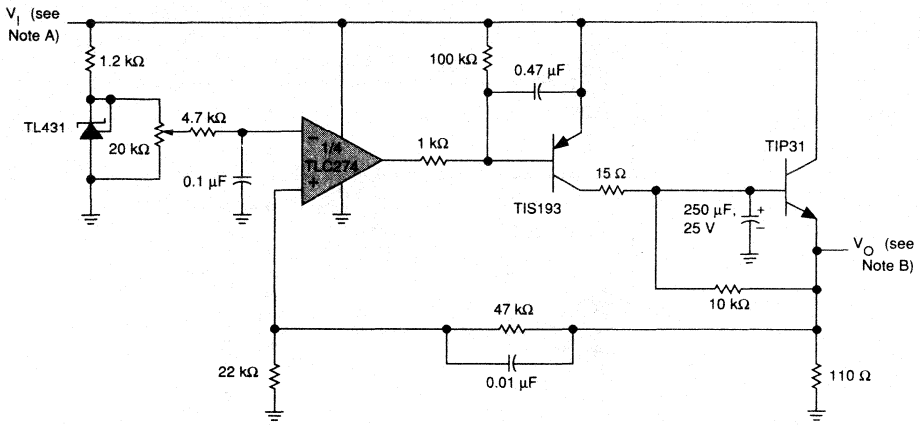


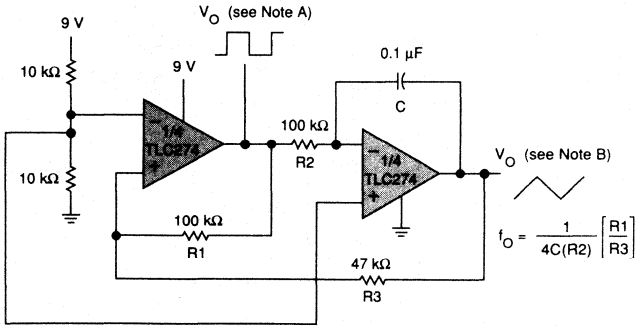
FIGURE 45. POSITIVE-PEAK DETECTOR

TYPICAL APPLICATION DATA



NOTES: A. V_I = 3.5 to 15 V
B. V_O = 2.0 V, 0 to 1 A

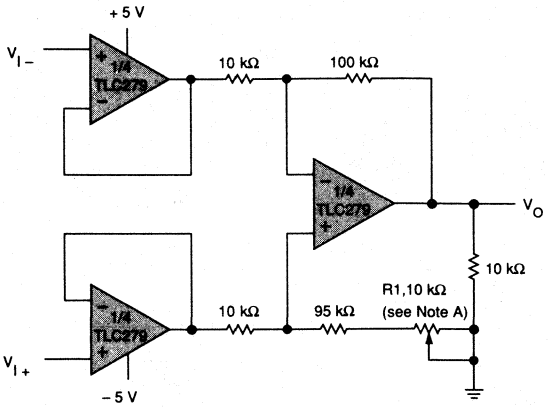
FIGURE 46. LOGIC ARRAY POWER SUPPLY



NOTES: A. V_{OPP} = 8 V
B. V_{OPP} = 4 V

FIGURE 47. SINGLE-SUPPLY FUNCTION GENERATOR

TYPICAL APPLICATION DATA



NOTE A: CMRR Adjustment (must be noninductive).

FIGURE 48. LOW-POWER INSTRUMENTATION AMPLIFIER

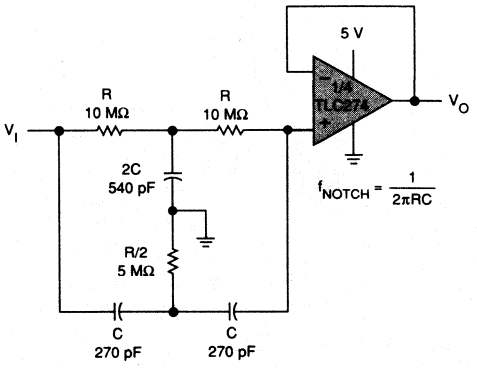
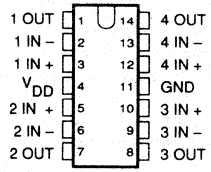


FIGURE 49. SINGLE-SUPPLY TWIN-T NOTCH FILTER

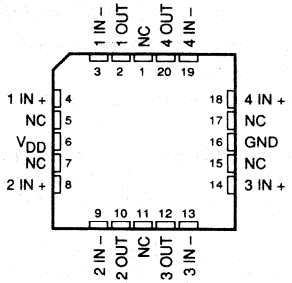
OCTOBER 1987

- **Trimmed Offset Voltage:**
  TLC27M9 . . . 900 μV Max at 25°C, V_{DD} = 5 V
- **Input Offset Voltage Drift Typically 0.1 μV / Month, Including the First 30 Days**
- **Wide Range of Supply Voltages Over Specified Temperature Range:**
  – 55°C to125°C . . . 4 V to 16 V
  – 40°C to 85°C . . . 4 V to 16 V
  0°C to 70°C . . . 3 V to 16 V
- **Single-Supply Operation**
- **Common-Mode Input Voltage Range Extends Below the Negative Rail (C- suffix, I- suffix types)**
- **Low Noise . . . 32 nV/√Hz Typically at f = 1 kHz**
- **Low Power . . . 2.1 mW Typically at 25°C, V_{DD} = 5 V**
- **Output Voltage Range Includes Negative Rail**
- **High Input Impedance . . . 10^{12} Ω Typical**
- **ESD Protection Circuitry**
- **Small-Outline Package Option Also Available in Tape-and-Reel**
- **Designed-in Latchup Immunity**

N AND J DUAL-IN-LINE PACKAGE
D SMALL-OUTLINE PACKAGE
(TOP VIEW)



FK CHIP CARRIER PACKAGE
(TOP VIEW)



NC – No internal connection

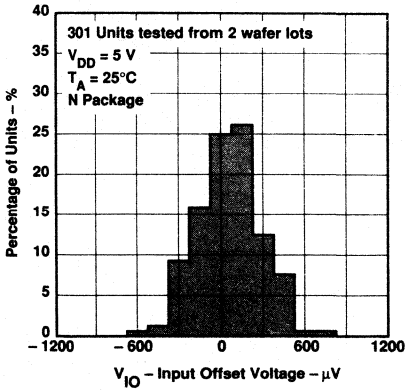
description

The TLC27M4 and TLC27M9 quad operational amplifiers combine a wide range of input offset voltage grades with low offset voltage drift, high input impedance, low noise, and speeds

T_A	V_{IO}max at 25°C	PACKAGE			
		Small-Outline (D) See Note 1	Plastic DIP (N)	Ceramic DIP (J)	Chip Carrier (FK)
0°C to 70°C	900 μV	TLC27M9CD	TLC27M9CN	TLC27M9CJ	—
	2 mV	TLC27M4BCD	TLC27M4BCN	TLC27M4BCJ	—
	5 mV	TLC27M4ACD	TLC27M4ACN	TLC27M4ACJ	—
	10 mV	TLC27M4CD	TLC27M4CN	TLC27M4CJ	—
– 40°C to 85°C	900 μV	TLC27M9ID	TLC27M9IN	TLC27M9IJ	—
	2 mV	TLC27M4BID	TLC27M4BIN	TLC27M4BIJ	—
	5 mV	TLC27M4AID	TLC27M4AIN	TLC27M4AIJ	—
	10 mV	TLC27M4ID	TLC27M4IN	TLC27M4IJ	—
– 55°C to 125°C	900 μV	—	—	TLC27M9MJ	TLC27M9MFK
	10 mV	—	—	TLC27M4MJ	TLC27M4MFK

NOTE 1: Available in tape-and-reel. Add "R" suffix to the device type when ordering (e.g., TLC27M9CDR).

DISTRIBUTION OF TLC27M9 INPUT OFFSET VOLTAGE



LinCMOS is a trademark of Texas Instruments Incorporated

description (continued)

comparable to that of general-purpose bipolar devices. These devices use Texas Instruments silicon-gate LinCMOS technology, which provides offset voltage stability far exceeding the stability available with conventional metal-gate processes.

The extremely high input impedance and low bias currents make these cost-effective devices ideal for applications which have previously been reserved for general-purpose bipolar products, but with only a fraction of the power consumption. Four offset voltage grades are available (C- suffix and I- suffix types), ranging from the low-cost TLC27M4 (10 mV) to the high-precision TLC27M9 (900 μV). These advantages, in combination with good common-mode rejection and supply voltage rejection, make these devices a good choice for new state-of-the-art designs as well as for upgrading existing designs.

In general, many features associated with bipolar technology are avaliable on LinCMOS operational amplifiers, without the power penalities of bipolar technology. General applications such as transducer interfacing, analog calculations, amplifier blocks, active filters, and signal buffering are all easily designed with the TLC27M4 and TLC27M9. The devices also exhibit low voltage single supply operation and low power consumption making them ideally suited for remote and inaccessible battery-powered applications. The common-mode input voltage range includes the negative rail.

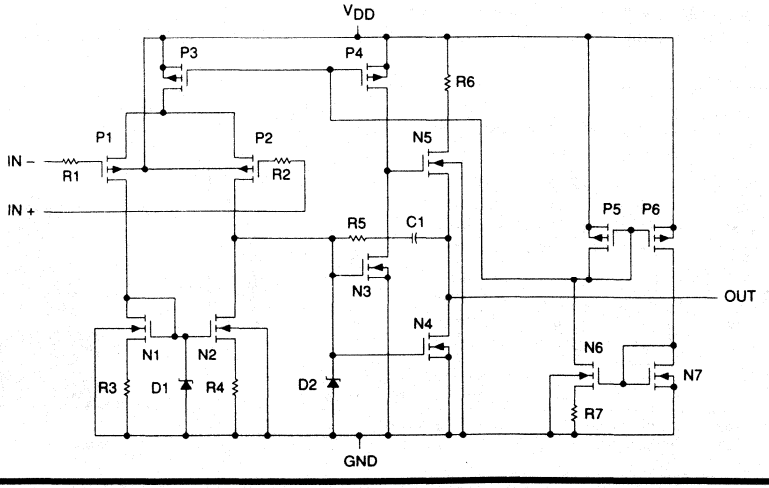
A wide range of packaging options is available, including small outline and chip carrier versions for high-density system applications.

The device inputs and outputs are designed to withstand – 100-mA surge currents without sustaining latchup.

The TLC27M4 and TLC27M9 incorporate internal ESD protection circuits that will prevent functional failures at voltages up to 2000 V as tested under MIL-STD-883C, Method 3015.2; however, care should be exercised in handling these devices as exposure to ESD may result in the degradation of the device parametric performance.

The M- suffix devices are characterized for operation over the full military temperature range of – 55°C to 125°C, the I- suffix devices from – 40°C to 85°C, and the C- suffix devices from 0°C to 70°C.

equivalent schematic (each amplifier)



absolute maximum ratings over operating free-air temperature (unless otherwise noted)

Supply voltage, V_{DD} (see Note 2) . . . . . 18 V
Differential input voltage (see Note 3) . . . . . $\pm V_{DD}$
Input voltage range, V_I (any input) . . . . . -0.3 V to V_{DD}
Input current, I_I . . . . . ± 5 mA
Output current, I_O (each output) . . . . . ± 30 mA
Total current into V_{DD} terminal . . . . . 45 mA
Total current out of ground terminal . . . . . 45 mA
Duration of short-circuit current at (or below) 25°C (see Note 4) . . . . . Unlimited
Continuous total dissipation . . . . . See Dissipation Rating Table
Operating free-air temperature, T_A: C-suffix types . . . . . 0°C to 70°C
I-suffix types . . . . . -40°C to 85°C
M-suffix types . . . . . -55°C to 125°C
Storage temperature range . . . . . -65°C to 150°C
Case temperature for 60 seconds: FK package . . . . . 260°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds: J package . . . . . 300°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: D and N package . . . . . 260°C

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25$°C POWER RATING	DERATING FACTOR ABOVE $T_A = 25$°C	$T_A = 70$°C POWER RATING	$T_A = 85$°C POWER RATING	$T_A = 125$°C POWER RATING
D	950 mW	7.6 mW/°C	608 mW	494 mW	
FK	1375 mW	11 mW/°C	880 mW	715 mW	275 mW
J (C-, I- suffix)	1025 mW	8.2 mW/°C	656 mW	533 mW	
J (M- suffix)	1375 mW	11 mW/°C	880 mW	715 mW	275 mW
N	1575 mW	12.6 mW/°C	1008 mW	819 mW	

recommended operating conditions

		M- SUFFIX TYPES			I- SUFFIX TYPES			C- SUFFIX TYPES			
		MIN	NOM	MAX	MIN	NOM	MAX	MIN	NOM	MAX	UNIT
Supply voltage, V_{DD}		4		16	4		16	3		16	V
Common-mode input voltage, V_{IC}	$V_{DD} = 5$ V	0		3.5	-0.2		3.5	-0.2		3.5	V
	$V_{DD} = 10$ V	0		8.5	-0.2		8.5	-0.2		8.5	V
Input voltage, V_I	$V_{DD} = 5$ V	0		3.5	-0.2		3.5	-0.2		3.5	V
	$V_{DD} = 10$ V	0		8.5	-0.2		8.5	-0.2		8.5	V
Operating free-air temperature, T_A		-55		125	-40		85	0		70	°C

NOTES: 2. All voltage values, except differential voltages, are with respect to network ground.
3. Differential voltages are at the noninverting input with respect to the inverting input.
4. The output may be shorted to either supply. Temperature and/or supply voltages must be limited to ensure that the maximum dissipation rating is not exceeded (see application section).

electrical characteristics at specified free-air temperature, V_{DD} = 5 V (unless otherwise noted)

PARAMETER			TEST CONDTIONS		C- SUFFIX TYPES MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage	TLC27M4C	V_O = 1.4 V, V_{IC} = 0 V, R_S = 50 Ω, R_L = 100 kΩ	25°C		1.1	10	mV
				Full range			12	
		TLC27M4AC	V_O = 1.4 V, V_{IC} = 0 V, R_S = 50 Ω, R_L = 100 kΩ	25°C		0.9	5	
				Full range			6.5	
		TLC27M4BC	V_O = 1.4 V, V_{IC} = 0 V, R_S = 50 Ω, R_L = 100 kΩ	25°C		250	2000	μV
				Full range			3000	
		TLC27M9C	V_O = 1.4 V, V_{IC} = 0 V, R_S = 50 Ω, R_L = 100 kΩ	25°C		210	900	
				Full range			1500	
α_{VIO}	Average temperature coefficient of input offset voltage			25°C to 70°C		1.7		μV/°C
I_{IO}	Input offset current (see Note 5)		V_{IC} = 2.5 V, V_O = 2.5 V	25°C		0.1		pA
				70°C		7	300	
I_{IB}	Input bias current (see Note 5)		V_{IC} = 2.5 V, V_O = 2.5 V	25°C		0.6		pA
				70°C		40	600	
V_{ICR}	Common-mode input voltage range (see Note 6)			25°C	−0.2 to 4	−0.3 to 4.2		V
				Full range	−0.2 to 3.5			V
V_{OH}	High-level output voltage		V_{ID} = 100 mV, R_L = 100 kΩ	25°C	3.2	3.9		V
				70°C	3	4		
				0°C	3	3.9		
V_{OL}	Low-level output voltage		V_{ID} = −100 mV, I_{OL} = 0	25°C		0	50	mV
				70°C		0	50	
				0°C		0	50	
A_{VD}	Large-signal differential voltage amplification		V_O = 0.25 V to 2 V, R_L = 100 kΩ	25°C	25	170		V/mV
				70°C	15	140		
				0°C	15	200		
CMRR	Common-mode rejection ratio		V_{IC} = V_{ICR} min	25°C	65	91		dB
				70°C	60	92		
				0°C	60	91		
k_{SVR}	Supply-voltage rejection ratio (ΔV_{DD} / ΔV_{IO})		V_{DD} = 5 V to 10 V, V_O = 1.4 V	25°C	70	93		dB
				70°C	60	94		
				0°C	60	92		
I_{DD}	Supply current (four amplifiers)		No load, V_O = 2.5 V, V_{IC} = 2.5 V	25°C		420	1120	μA
				70°C		340	880	
				0°C		500	1280	

NOTES: 5. The typical values of input bias current and input offset current below 5 pA were determined mathematically.
6. This range also applies to each input individually.

electrical characteristics at specified free-air temperature, V_{DD} = 10 V (unless otherwise noted)

PARAMETER			TEST CONDTIONS		C- SUFFIX TYPES			UNIT
					MIN	TYP	MAX	
V_{IO}	Input offset voltage	TLC27M4C	V_O = 1.4 V, V_{IC} = 0 V, R_S = 50 Ω, R_L = 100 kΩ	25°C		1.1	10	mV
				Full range			12	
		TLC27M4AC	V_O = 1.4 V, V_{IC} = 0 V, R_S = 50 Ω, R_L = 100 kΩ	25°C		0.9	5	
				Full range			6.5	
		TLC27M4BC	V_O = 1.4 V, V_{IC} = 0 V, R_S = 50 Ω, R_L = 100 kΩ	25°C		260	2000	μV
				Full range			3000	
		TLC27M9C	V_O = 1.4 V, V_{IC} = 0 V, R_S = 50 Ω, R_L = 100 kΩ	25°C		220	1200	
				Full range			1900	
α_{VIO}	Average temperature coefficient of input offset voltage			25°C to 70°C		2.1		μV/°C
I_{IO}	Input offset current (see Note 5)		V_{IC} = 5 V, V_O = 5 V	25°C		0.1		pA
				70°C		8	300	
I_{IB}	Input bias current (see Note 5)		V_{IC} = 5 V, V_O = 5 V	25°C		0.7		pA
				70°C		50	600	
V_{ICR}	Common-mode input voltage range (see Note 6)			25°C	−0.2 to 9	−0.3 to 9.2		V
				Full range	−0.2 to 8.5			V
V_{OH}	High-level output voltage		V_{ID} = 100 mV, R_L = 100 kΩ	25°C	8	8.7		V
				70°C	7.8	8.7		
				0°C	7.8	8.7		
V_{OL}	Low-level output voltage		V_{ID} = −100 mV, I_{OL} = 0	25°C		0	50	mV
				70°C		0	50	
				0°C		0	50	
A_{VD}	Large-signal differential voltage amplification		V_O = 1 V to 6 V, R_L = 100 kΩ	25°C	25	275		V/mV
				70°C	15	230		
				0°C	15	320		
CMRR	Common-mode rejection ratio		V_{IC} = V_{ICR} min	25°C	65	94		dB
				70°C	60	94		
				0°C	60	94		
k_{SVR}	Supply-voltage rejection ratio (ΔV_{DD} / ΔV_{IO})		V_{DD} = 5 V to 10 V, V_O = 1.4 V	25°C	70	93		dB
				70°C	60	94		
				0°C	60	92		
I_{DD}	Supply current (four amplifiers)		No load, V_O = 5 V, V_{IC} = 5 V	25°C		570	1200	μA
				70°C		440	1120	
				0°C		690	1600	

NOTES: 5. The typical values of input bias current and input offset current below 5 pA were determined mathematically.
6. This range also applies to each input individually.

electrical characteristics at specified free-air temperature, V_{DD} = 5 V (unless otherwise noted)

PARAMETER			TEST CONDTIONS		I- SUFFIX TYPES			UNIT
					MIN	TYP	MAX	
V_{IO}	Input offset voltage	TLC27M4I	V_O = 1.4 V, V_{IC} = 0 V, R_S = 50 Ω, R_L = 100 kΩ	25°C		1.1	10	mV
				Full range			13	
		TLC27M4AI	V_O = 1.4 V, V_{IC} = 0 V, R_S = 50 Ω, R_L = 100 kΩ	25°C		0.9	5	
				Full range			7	
		TLC27M4BI	V_O = 1.4 V, V_{IC} = 0 V, R_S = 50 Ω, R_L = 100 kΩ	25°C		250	2000	µV
				Full range			3500	
		TLC27M9I	V_O = 1.4 V, V_{IC} = 0 V, R_S = 50 Ω, R_L = 100 kΩ	25°C		210	900	
				Full range			2000	
α_{VIO}	Average temperature coefficient of input offset voltage			25°C to 85°C		1.7		µV/°C
I_{IO}	Input offset current (see Note 5)		V_{IC} = 2.5 V, V_O = 2.5 V	25°C		0.1		pA
				85°C		24	1000	
I_{IB}	Input bias current (see Note 5)		V_{IC} = 2.5 V, V_O = 2.5 V	25°C		0.6		pA
				85°C		200	2000	
V_{ICR}	Common-mode input voltage range (see Note 6)			25°C	−0.2 to 4	−0.3 to 4.2		V
				Full range	−0.2 to 3.5			V
V_{OH}	High-level output voltage		V_{ID} = 100 mV, R_L = 100 kΩ	25°C	3.2	3.9		V
				85°C	3	4		
				−40°C	3	3.9		
V_{OL}	Low-level output voltage		V_{ID} = −100 mV, I_{OL} = 0	25°C		0	50	mV
				85°C		0	50	
				−40°C		0	50	
A_{VD}	Large-signal differential voltage amplification		V_O = 0.25 V to 2 V, R_L = 100 kΩ	25°C	25	170		V/mV
				85°C	15	130		
				−40°C	15	270		
CMRR	Common-mode rejection ratio		V_{IC} = V_{ICR} min	25°C	65	91		dB
				85°C	60	90		
				−40°C	60	90		
k_{SVR}	Supply-voltage rejection ratio (ΔV_{DD} / ΔV_{IO})		V_{DD} = 5 V to 10 V, V_O = 1.4 V	25°C	70	93		dB
				85°C	60	94		
				−40°C	60	91		
I_{DD}	Supply current (four amplifiers)		No load, V_O = 2.5 V, V_{IC} = 2.5 V	25°C		420	1120	µA
				85°C		320	800	
				−40°C		630	1600	

NOTES: 5. The typical values of input bias current and input offset current below 5 pA were determined mathematically.
6. This range also applies to each input individually.

electrical characteristics at specified free-air temperature, V_{DD} = 10 V (unless otherwise noted)

PARAMETER			TEST CONDTIONS		I- SUFFIX TYPES			UNIT
					MIN	TYP	MAX	
V_{IO}	Input offset voltage	TLC27M4I	V_O = 1.4 V, V_{IC} = 0 V, R_S = 50 Ω, R_L = 100 kΩ	25°C		1.1	10	mV
				Full range			13	
		TLC27M4AI	V_O = 1.4 V, V_{IC} = 0 V, R_S = 50 Ω, R_L = 100 kΩ	25°C		0.9	5	
				Full range			7	
		TLC27M4BI	V_O = 1.4 V, V_{IC} = 0 V, R_S = 50 Ω, R_L = 100 kΩ	25°C		260	2000	μV
				Full range			3500	
		TLC27M9I	V_O = 1.4 V, V_{IC} = 0 V, R_S = 50 Ω, R_L = 100 kΩ	25°C		220	1200	
				Full range			2900	
α_{VIO}	Average temperature coefficient of input offset voltage			25°C to 85°C		2.1		μV/°C
I_{IO}	Input offset current (see Note 5)		V_{IC} = 5 V, V_O = 5 V	25°C		0.1		pA
				85°C		26	1000	
I_{IB}	Input bias current (see Note 5)		V_{IC} = 5 V, V_O = 5 V	25°C		0.7		pA
				85°C		220	2000	
V_{ICR}	Common-mode input voltage range (see Note 6)			25°C	−0.2 to 9	−0.3 to 9.2		V
				Full range	−0.2 to 8.5			V
V_{OH}	High-level output voltage		V_{ID} = 100 mV, R_L = 100 kΩ	25°C	8	8.7		V
				85°C	7.8	8.7		
				−40°C	7.8	8.7		
V_{OL}	Low-level output voltage		V_{ID} = −100 mV, I_{OL} = 0	25°C		0	50	mV
				85°C		0	50	
				−40°C		0	50	
A_{VD}	Large-signal differential voltage amplification		V_O = 1 V to 6 V, R_L = 100 kΩ	25°C	25	275		V/mV
				85°C	15	220		
				−40°C	15	390		
CMRR	Common-mode rejection ratio		V_{IC} = V_{ICR} min	25°C	65	94		dB
				85°C	60	94		
				−40°C	60	93		
k_{SVR}	Supply-voltage rejection ratio (ΔV_{DD} / ΔV_{IO})		V_{DD} = 5 V to 10 V, V_O = 1.4 V	25°C	70	93		dB
				85°C	60	94		
				−40°C	60	91		
I_{DD}	Supply current (four amplifiers)		No load, V_O = 5 V, V_{IC} = 5 V	25°C		570	1200	μA
				85°C		410	1040	
				−40°C		900	1800	

NOTES: 5. The typical values of input bias current and input offset current below 5 pA were determined mathematically.
6. This range also applies to each input individually.

electrical characteristics at specified free-air temperature, V_{DD} = 5 V (unless otherwise noted)

PARAMETER			TEST CONDTIONS		M- SUFFIX TYPES MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage	TLC27M4M	V_O = 1.4 V, V_{IC} = 0 V, R_S = 50 Ω, R_L = 100 kΩ	25°C		1.1	10	mV
				Full range			12	
		TLC27M9M	V_O = 1.4 V, V_{IC} = 0 V, R_S = 50 Ω, R_L = 100 kΩ	25°C		210	900	µV
				Full range			3750	
α_{VIO}	Average temperature coefficient of input offset voltage			25°C to 125°C		1.7		µV/°C
I_{IO}	Input offset current (see Note 5)		V_{IC} = 2.5 V, V_O = 2.5 V	25°C		0.1		pA
				125°C		1.4	15	nA
I_{IB}	Input bias current (see Note 5)		V_{IC} = 2.5 V, V_O = 2.5 V	25°C		0.6		pA
				125°C		9	35	nA
V_{ICR}	Common-mode input voltage range (see Note 6)			25°C	0.0 to 4	− 0.3 to 4.2		V
				Full range	0.0 to 3.5			V
V_{OH}	High-level output voltage		V_{ID} = 100 mV, R_L = 100 kΩ	25°C	3.2	3.9		V
				125°C	3	4		
				− 55°C	3	3.9		
V_{OL}	Low-level output voltage		V_{ID} = − 100 mV, I_{OL} = 0	25°C		0	50	mV
				125°C		0	50	
				− 55°C		0	50	
A_{VD}	Large-signal differential voltage amplification		V_O = 0.25 V to 2 V, R_L = 100 kΩ	25°C	25	170		V/mV
				125°C	15	120		
				− 55°C	15	290		
CMRR	Common-mode rejection ratio		V_{IC} = V_{ICR} min	25°C	65	91		dB
				125°C	60	91		
				− 55°C	60	89		
k_{SVR}	Supply-voltage rejection ratio (ΔV_{DD} / ΔV_{IO})		V_{DD} = 5 V to 10 V, V_O = 1.4 V	25°C	70	93		dB
				125°C	60	94		
				− 55°C	60	91		
I_{DD}	Supply current (four amplifiers)		No load, V_O = 2.5 V, V_{IC} = 2.5 V	25°C		420	1120	µA
				125°C		280	720	
				− 55°C		680	1760	

NOTES: 5. The typical values of input bias current and input offset current below 5 pA were determined mathematically.
6. This range also applies to each input individually.

electrical characteristics at specified free-air temperature, V_{DD} = 10 V (unless otherwise noted)

PARAMETER			TEST CONDTIONS		M- SUFFIX TYPES MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage	TLC27M4M	V_O = 1.4 V, V_{IC} = 0 V, R_S = 50 Ω, R_L = 100 kΩ	25°C		1.1	10	mV
				Full range			12	
		TLC27M9M	V_O = 1.4 V, V_{IC} = 0 V, R_S = 50 Ω, R_L = 100 kΩ	25°C		220	1200	μV
				Full range			4300	
α_{VIO}	Average temperature coefficient of input offset voltage			25°C to 125°C		2.1		μV/°C
I_{IO}	Input offset current (see Note 5)		V_{IC} = 5 V, V_O = 5 V	25°C		0.1		pA
				125°C		1.8	15	nA
I_{IB}	Input bias current (see Note 5)		V_{IC} = 5 V, V_O = 5 V	25°C		0.7		pA
				125°C		10	35	nA
V_{ICR}	Common-mode input voltage range (see Note 6)			25°C	0.0 to 9	− 0.3 to 9.2		V
				Full range	0.0 to 8.5			V
V_{OH}	High-level output voltage		V_{ID} = 100 mV, R_L = 100 kΩ	25°C	8	8.7		V
				125°C	7.8	8.8		
				− 55°C	7.8	8.6		
V_{OL}	Low-level output voltage		V_{ID} = − 100 mV, I_{OL} = 0	25°C		0	50	mV
				125°C		0	50	
				− 55°C		0	50	
A_{VD}	Large-signal differential voltage amplification		V_O = 1 V to 6 V, R_L = 100 kΩ	25°C	25	275		V/mV
				125°C	15	190		
				− 55°C	15	420		
CMRR	Common-mode rejection ratio		V_{IC} = V_{ICR} min	25°C	65	94		dB
				125°C	60	93		
				− 55°C	60	93		
k_{SVR}	Supply-voltage rejection ratio (ΔV_{DD} / ΔV_{IO})		V_{DD} = 5 V to 10 V, V_O = 1.4 V	25°C	70	93		dB
				125°C	60	94		
				− 55°C	60	91		
I_{DD}	Supply current (four amplifiers)		No load, V_O = 5 V, V_{IC} = 5 V	25°C		570	1200	μA
				125°C		360	960	
				− 55°C		980	2000	

NOTES: 5. The typical values of input bias current and input offset current below 5 pA were determined mathematically.
6. This range also applies to each input individually.

operating characteristics, V_{DD} = 5 V

PARAMETER		TEST CONDTIONS			C- SUFFIX TYPES MIN	TYP	MAX	UNIT
SR	Slew rate at unity gain	R_L = 100 kΩ, C_L = 20 pF, See Figure 1	V_{IPP} = 1 V	25°C		0.43		V/μs
				70°C		0.36		
				0°C		0.46		
			V_{IPP} = 2.5 V	25°C		0.40		
				70°C		0.34		
				0°C		0.43		
V_n	Equivalent input noise voltage	f = 1 kHz, R_S = 100 Ω, See Figure 2		25°C		32		nV/√Hz
B_{OM}	Maximum output swing bandwidth	V_O = V_{OH}, C_L = 20 pF, R_L = 100 kΩ, See Figure 1		25°C		55		kHz
				70°C		50		
				0°C		60		
B_1	Unity-gain bandwidth	V_i = 10 mV, C_L = 20 pF, See Figure 3		25°C		525		kHz
				70°C		400		
				0°C		600		
ϕ_m	Phase margin	f = B_1, V_i = 10 mV, C_L = 20 pF, See Figure 3		25°C		40°		
				70°C		39°		
				0°C		41°		

operating characteristics, V_{DD} = 10 V

PARAMETER		TEST CONDTIONS			C- SUFFIX TYPES MIN	TYP	MAX	UNIT
SR	Slew rate at unity gain	R_L = 100 kΩ, C_L = 20 pF, See Figure 1	V_{IPP} = 1 V	25°C		0.62		V/μs
				70°C		0.51		
				0°C		0.67		
			V_{IPP} = 5.5 V	25°C		0.56		
				70°C		0.46		
				0°C		0.61		
V_n	Equivalent input noise voltage	f = 1 kHz, R_S = 100 Ω, See Figure 2		25°C		32		nV/√Hz
B_{OM}	Maximum output swing bandwidth	V_O = V_{OH}, C_L = 20 pF, R_L = 100 kΩ, See Figure 1		25°C		35		kHz
				70°C		30		
				0°C		40		
B_1	Unity-gain bandwidth	V_i = 10 mV, C_L = 20 pF, See Figure 3		25°C		635		kHz
				70°C		510		
				0°C		710		
ϕ_m	Phase margin	f = B_1, V_i = 10 mV, C_L = 20 pF, See Figure 3		25°C		43°		
				70°C		42°		
				0°C		44°		

operating characteristics, V_{DD} = 5 V

PARAMETER		TEST CONDTIONS			I- SUFFIX TYPES MIN	TYP	MAX	UNIT
SR	Slew rate at unity gain	R_L = 100 kΩ, C_L = 20 pF, See Figure 1	V_{IPP} = 1 V	25°C		0.43		V/μs
				85°C		0.35		
				− 40°C		0.51		
			V_{IPP} = 2.5 V	25°C		0.40		
				85°C		0.32		
				− 40°C		0.48		
V_n	Equivalent input noise voltage	f = 1 kHz, R_S = 100 Ω, See Figure 2		25°C		32		nV/√Hz
B_{OM}	Maximum output swing bandwidth	V_O = V_{OH}, C_L = 20 pF, R_L = 100 kΩ, See Figure 1		25°C		55		kHz
				85°C		45		
				− 40°C		75		
B_1	Unity-gain bandwidth	V_i = 10 mV, C_L = 20 pF, See Figure 3		25°C		525		kHz
				85°C		370		
				− 40°C		770		
ϕ_m	Phase margin	f = B_1, V_i = 10 mV, C_L = 20 pF, See Figure 3		25°C		40°		
				85°C		38°		
				− 40°C		43°		

operating characteristics, V_{DD} = 10 V

PARAMETER		TEST CONDTIONS			I- SUFFIX TYPES MIN	TYP	MAX	UNIT
SR	Slew rate at unity gain	R_L = 100 kΩ, C_L = 20 pF, See Figure 1	V_{IPP} = 1 V	25°C		0.62		V/μs
				85°C		0.47		
				− 40°C		0.77		
			V_{IPP} = 5.5 V	25°C		0.56		
				85°C		0.44		
				− 40°C		0.70		
V_n	Equivalent input noise voltage	f = 1 kHz, R_S = 100 Ω, See Figure 2		25°C		32		nV/√Hz
B_{OM}	Maximum output swing bandwidth	V_O = V_{OH}, C_L = 20 pF, R_L = 100 kΩ, See Figure 1		25°C		35		kHz
				85°C		25		
				− 40°C		45		
B_1	Unity-gain bandwidth	V_i = 10 mV, C_L = 20 pF, See Figure 3		25°C		635		kHz
				85°C		480		
				− 40°C		880		
ϕ_m	Phase margin	f = B_1, V_i = 10 mV, C_L = 20 pF, See Figure 3		25°C		43°		
				85°C		41°		
				− 40°C		46°		

operating characteristics, V_{DD} = 5 V

PARAMETER		TEST CONDTIONS			M- SUFFIX TYPES MIN	M- SUFFIX TYPES TYP	M- SUFFIX TYPES MAX	UNIT
SR	Slew rate at unity gain	R_L = 100 kΩ, C_L = 20 pF, See Figure 1	V_{IPP} = 1 V	25°C		0.43		V/μs
				125°C		0.29		
				– 55°C		0.54		
			V_{IPP} = 2.5 V	25°C		0.40		
				125°C		0.28		
				– 55°C		0.50		
V_n	Equivalent input noise voltage	f = 1 kHz, R_S = 100 Ω, See Figure 2		25°C		32		nV/√Hz
B_{OM}	Maximum output swing bandwidth	$V_O = V_{OH}$, C_L = 20 pF, R_L = 100 kΩ, See Figure 1		25°C		55		kHz
				125°C		40		
				– 55°C		80		
B_1	Unity-gain bandwidth	V_i = 10 mV, C_L = 20 pF, See Figure 3		25°C		525		kHz
				125°C		330		
				– 55°C		850		
ϕ_m	Phase margin	f = B_1, V_i = 10 mV, C_L = 20 pF, See Figure 3		25°C		40°		
				125°C		36°		
				– 55°C		44°		

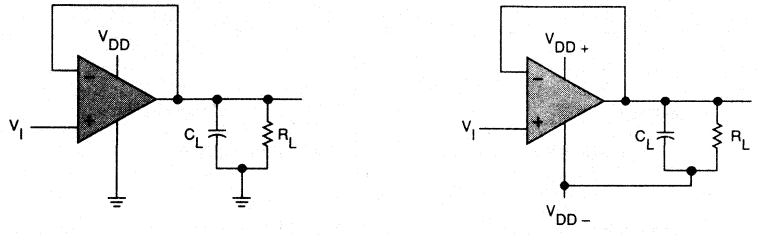
operating characteristics, V_{DD} = 10 V

PARAMETER		TEST CONDTIONS			M- SUFFIX TYPES MIN	M- SUFFIX TYPES TYP	M- SUFFIX TYPES MAX	UNIT
SR	Slew rate at unity gain	R_L = 100 kΩ, C_L = 20 pF, See Figure 1	V_{IPP} = 1 V	25°C		0.62		V/μs
				125°C		0.38		
				– 55°C		0.81		
			V_{IPP} = 5.5 V	25°C		0.56		
				125°C		0.35		
				– 55°C		0.73		
V_n	Equivalent input noise voltage	f = 1 kHz, R_S = 100 Ω, See Figure 2		25°C		32		nV/√Hz
B_{OM}	Maximum output swing bandwidth	$V_O = V_{OH}$, C_L = 20 pF, R_L = 100 kΩ, See Figure 1		25°C		35		kHz
				125°C		20		
				– 55°C		50		
B_1	Unity-gain bandwidth	V_i = 10 mV, C_L = 20 pF, See Figure 3		25°C		635		kHz
				125°C		440		
				– 55°C		960		
ϕ_m	Phase margin	f = B_1, V_i = 10 mV, C_L = 20 pF, See Figure 3		25°C		43°		
				125°C		39°		
				– 55°C		47°		

PARAMETER MEASUREMENT INFORMATION

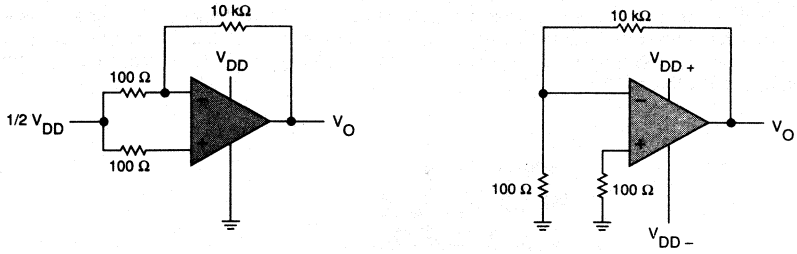
single-supply versus split-supply test circuits

Because the TLC27M4 and TLC27M9 are optimized for single-supply operation, circuit configurations used for the various tests often present some inconvenience since the input signal, in many cases, must be offset from ground. This inconvenience can be avoided by testing the device with split supplies and the output load tied to the negative rail. A comparison of single-supply versus split-supply test circuits is shown below. The use of either circuit will give the same result.



(a) Single-Supply (b) Split-Supply

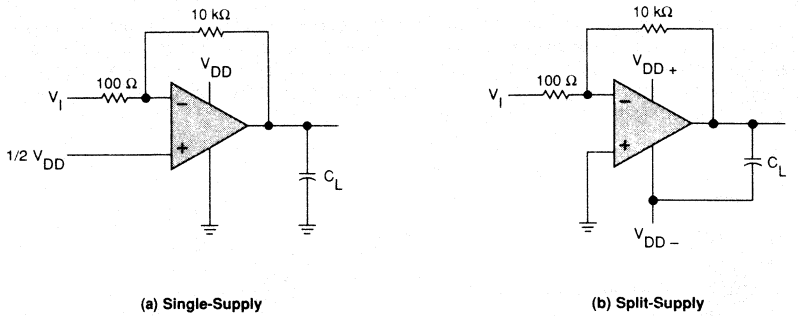
FIGURE 1. UNITY-GAIN AMPLIFIER



(a) Single-Supply (b) Split-Supply

FIGURE 2. NOISE TEST CIRCUIT

PARAMETER MEASUREMENT INFORMATION



(a) Single-Supply (b) Split-Supply

FIGURE 3. GAIN-OF-100 INVERTING AMPLIFIER

input bias current

Because of the high input impedance of the TLC27M4 and TLC27M9 op amps, attempts to measure the input bias current can result in erroneous readings. The typical bias current at normal room ambient temperature is typically less than 1 pA, a value that is easily exceeded by leakages on the test socket. Two suggestions are offered to avoid erroneous measurements:

1 Isolate the device from other potential leakage sources. Use a grounded shield around and between the device inputs (see Figure 4). Leakages that would otherwise flow to the inputs will be shunted away.

2 Compensate for the leakage of the test socket by actually performing an input bias current test (using a picoammeter) with no device in the test socket. The actual input bias current can then be calculated by subtracting the "open-socket" leakage readings from the readings obtained with a device in the test socket.

One word of caution . . . many automatic testers as well as some bench-top op amp testers use the servo-loop technique with a resistor in series with the device input to measure the input bias current (the voltage drop across the series resistor is measured and the bias current is calculated). This method requires that a device be inserted into the test socket to obtain a correct reading; therefore, an "open-socket" reading is not feasible using this method.

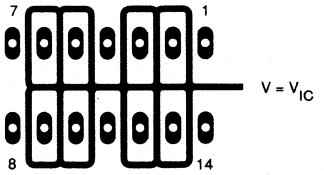


FIGURE 4. ISOLATION METAL AROUND DEVICE INPUTS
(N AND J DUAL-IN-LINE PACKAGE)

PARAMETER MEASUREMENT INFORMATION

low-level output voltage

To obtain low-supply-voltage operation, some compromise was necessary in the input stage. This compromise results in the device low-level output being dependent on both the common-mode input voltage level as well as the differential input voltage level. When attempting to correlate low-level output readings with those quoted in the electrical specifications, these two conditions should be observed. If conditions other than these are to be used, please refer to Figures 14 thru 19 in the Typical Characteristics section of this data sheet.

input offset voltage temperature coefficient

Erroneous readings often result from attempts to measure temperature coefficient of input offset voltage. This parameter is actually a calculation using input offset voltage measurements obtained at two different temperatures. When one (or both) of the temperatures is below freezing, moisture can collect on both the device and the test socket. This moisture will result in leakage and contact resistance which can cause erroneous input offset voltage readings. The isolation techniques previously mentioned have no affect on the leakage since the moisture also covers the isolation metal itself, thereby rendering it useless. It is suggested that these measurements be performed at temperatures above freezing to minimize error.

full power response

Full power response, the frequency above which the op amp slew rate limits the output voltage swing, is often specified two ways . . . full-linear response and full-peak response. The full-linear response is generally measured by monitoring the distortion level of the output while increasing the frequency of a sinusoidal input signal until the maximum frequency is found above which the output contains significant distortion. The full-peak response is defined as the maximum output frequency, without regard to distortion, above which full peak-to-peak output swing cannot be maintained.

Because there is no industry-wide accepted value for "significant" distortion, the full peak response is specified in this data sheet and is measured using the circuit of Figure 1. The initial setup involves the use of a sinusoidal input to determine the maximum peak-to-peak output of the device (the amplitude of the sinusoidal wave is increased until clipping occurs). The sinusoidal wave is then replaced with a square wave of the same amplitude. The frequency is then increased until the maximum peak-to-peak output can no longer be maintained (Figure 5). A square wave is used to allow a more accurate determination of the point at which the maximum peak-to-peak output is reached.

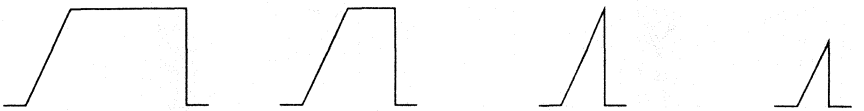


FIGURE 5. FULL-POWER-RESPONSE OUTPUT SIGNAL

test time

Inadequate test time is a frequent problem, especially when testing CMOS devices in a high-volume, short-test-time environment. Internal capacitances are inherently higher in CMOS than in bipolar and BiFET devices, and require longer test times than their bipolar and BiFET counterparts. The problem becomes more pronounced with reduced supply levels and lower temperatures.

TYPICAL CHARACTERISTICS

DISTRIBUTION OF TLC27M4
INPUT OFFSET VOLTAGE

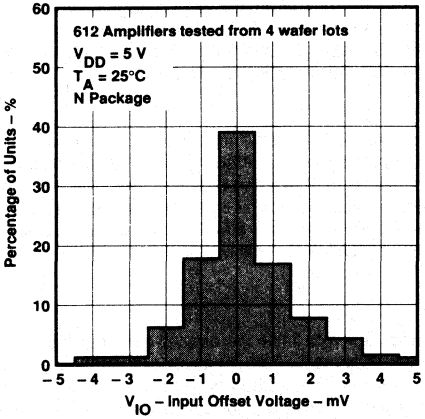


FIGURE 6

DISTRIBUTION OF TLC27M4
INPUT OFFSET VOLTAGE

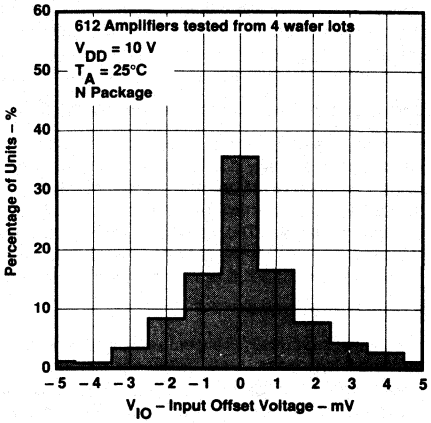


FIGURE 7

DISTRIBUTION OF TLC27M4 AND TLC27M9
INPUT OFFSET VOLTAGE
TEMPERATURE COEFFICIENT

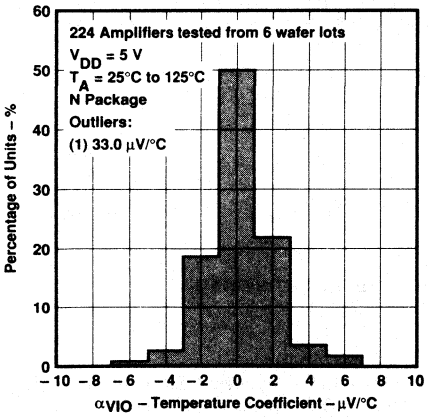


FIGURE 8

DISTRIBUTION OF TLC27M4 AND TLC27M9
INPUT OFFSET VOLTAGE
TEMPERATURE COEFFICIENT

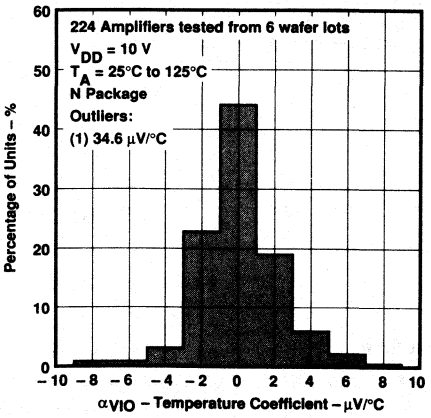


FIGURE 9

TYPICAL CHARACTERISTICS

HIGH-LEVEL OUTPUT VOLTAGE
vs
HIGH-LEVEL OUTPUT CURRENT

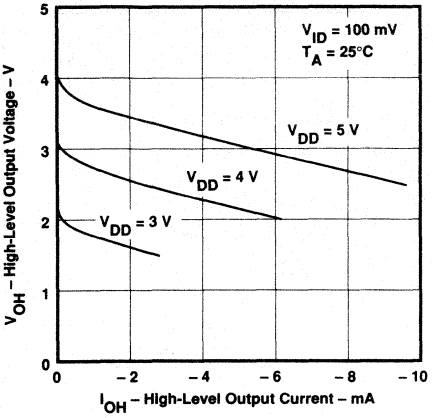


FIGURE 10

HIGH-LEVEL OUTPUT VOLTAGE
vs
HIGH-LEVEL OUTPUT CURRENT

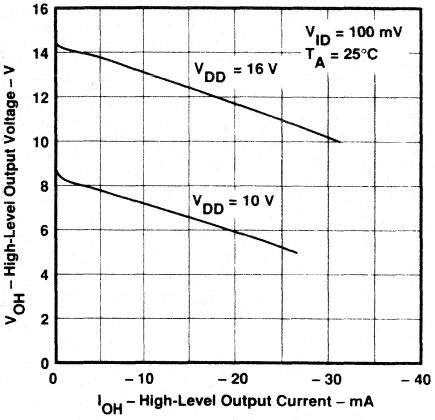


FIGURE 11

HIGH-LEVEL OUTPUT VOLTAGE
vs
SUPPLY VOLTAGE

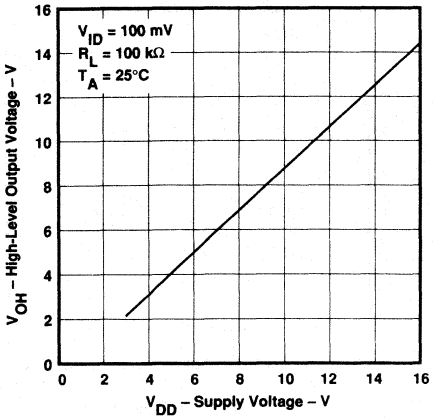


FIGURE 12

HIGH-LEVEL OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE

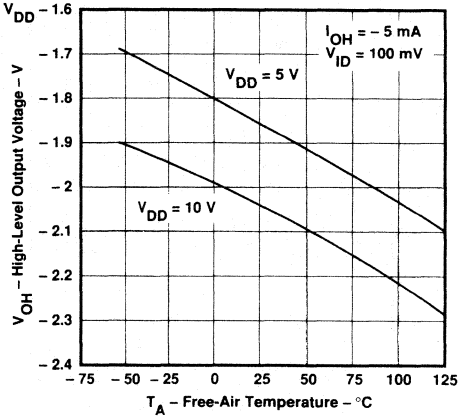


FIGURE 13

TYPICAL CHARACTERISTICS

LOW-LEVEL OUTPUT VOLTAGE
vs
COMMON-MODE INPUT VOLTAGE

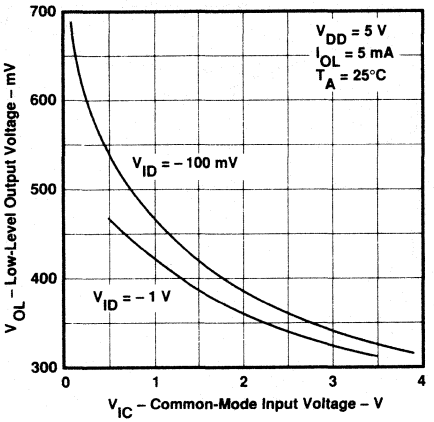


FIGURE 14

LOW-LEVEL OUTPUT VOLTAGE
vs
COMMON-MODE INPUT VOLTAGE

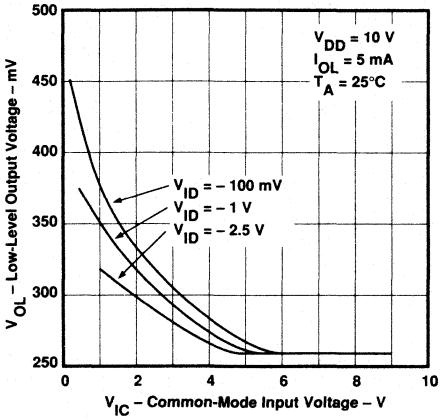


FIGURE 15

LOW-LEVEL OUTPUT VOLTAGE
vs
DIFFERENTIAL INPUT VOLTAGE

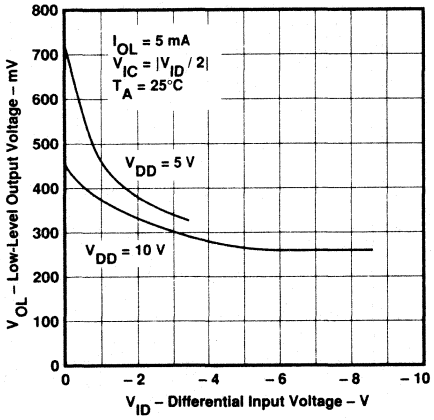


FIGURE 16

LOW-LEVEL OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE

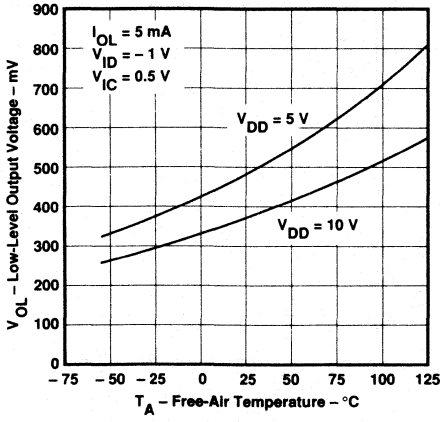


FIGURE 17

TYPICAL CHARACTERISTICS

LOW-LEVEL OUTPUT VOLTAGE
vs
LOW-LEVEL OUTPUT CURRENT

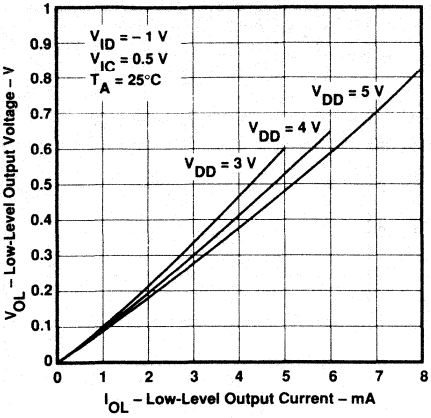


FIGURE 18

LOW-LEVEL OUTPUT VOLTAGE
vs
LOW-LEVEL OUTPUT CURRENT

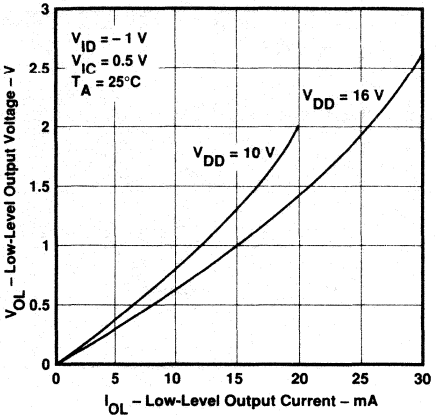


FIGURE 19

LARGE-SIGNAL
DIFFERENTIAL VOLTAGE AMPLIFICATION
vs
SUPPLY VOLTAGE

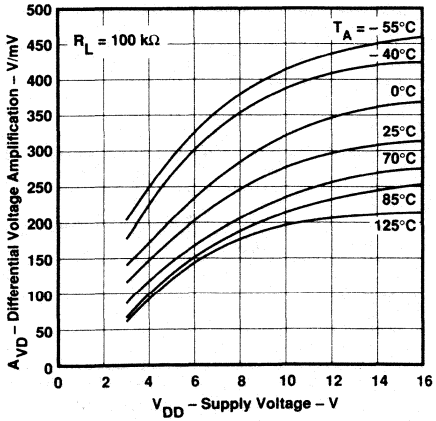


FIGURE 20

LARGE-SIGNAL
DIFFERENTIAL VOLTAGE AMPLIFICATION
vs
FREE-AIR TEMPERATURE

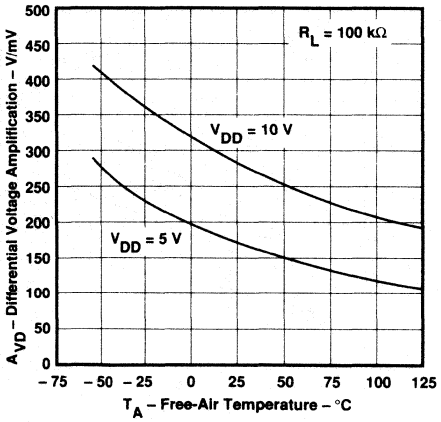


FIGURE 21

TYPICAL CHARACTERISTICS

INPUT BIAS CURRENT AND INPUT OFFSET CURRENT
vs
FREE-AIR TEMPERATURE

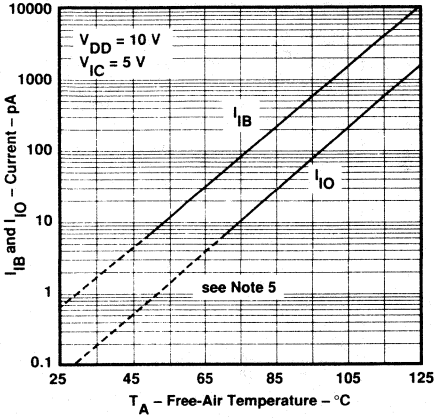


FIGURE 22

MAXIMUM INPUT VOLTAGE
vs
SUPPLY VOLTAGE

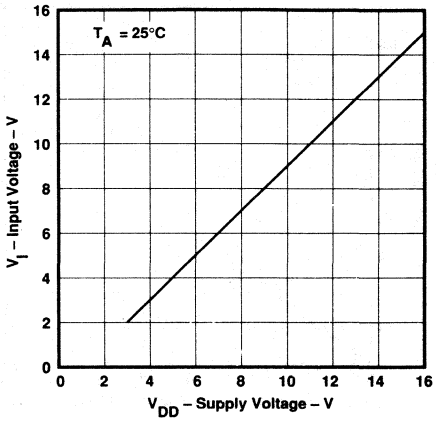


FIGURE 23

SUPPLY CURRENT
vs
SUPPLY VOLTAGE

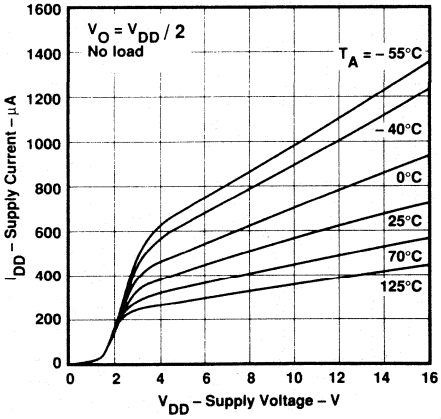


FIGURE 24

SUPPLY CURRENT
vs
FREE-AIR TEMPERATURE

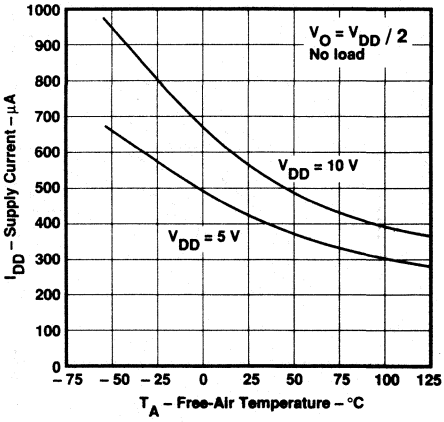


FIGURE 25

NOTE 5: The typical values of input bias current and input offset current below 5 pA were determined mathematically.

TYPICAL CHARACTERISTICS

SLEW RATE
vs
SUPPLY VOLTAGE

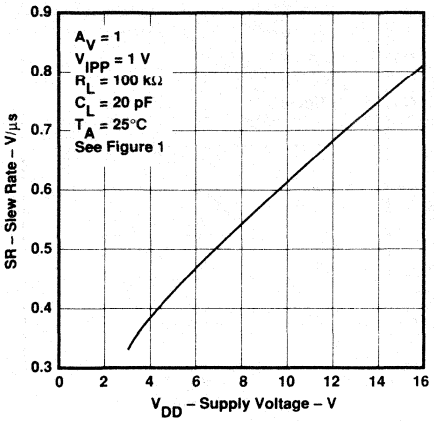


FIGURE 26

SLEW RATE
vs
FREE-AIR TEMPERATURE

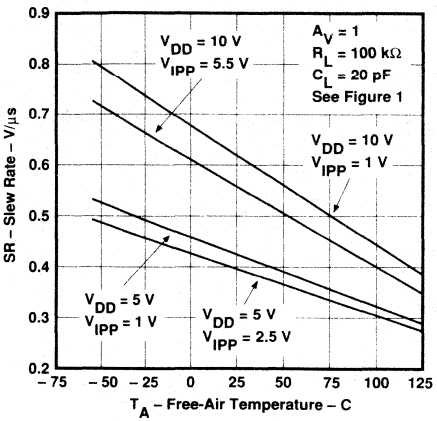


FIGURE 27

NORMALIZED SLEW RATE
vs
FREE-AIR TEMPERATURE

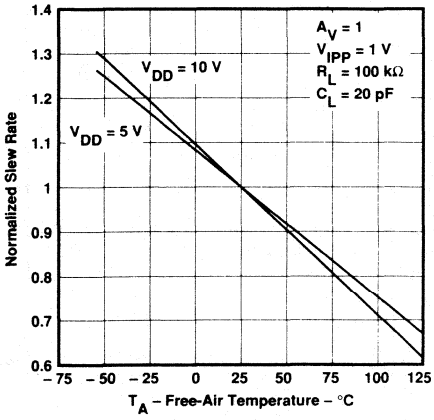


FIGURE 28

MAXIMUM PEAK-TO-PEAK OUTPUT VOLTAGE
vs
FREQUENCY

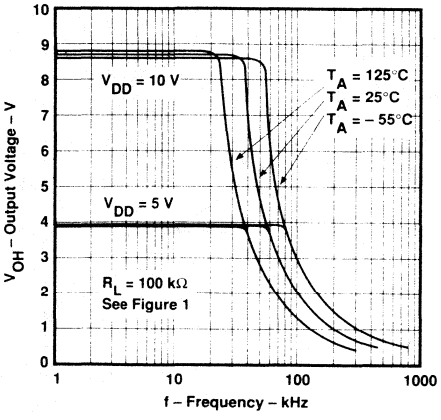


FIGURE 29

TYPICAL CHARACTERISTICS

UNITY-GAIN BANDWIDTH
vs
FREE-AIR TEMPERATURE

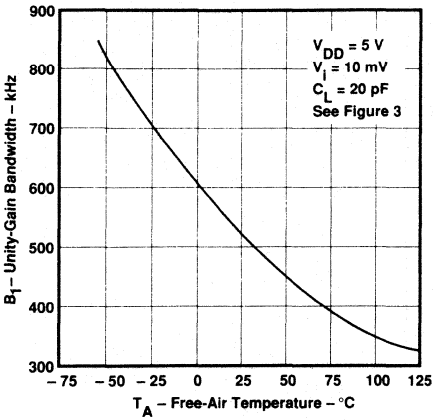


FIGURE 30

UNITY-GAIN BANDWIDTH
vs
SUPPLY VOLTAGE

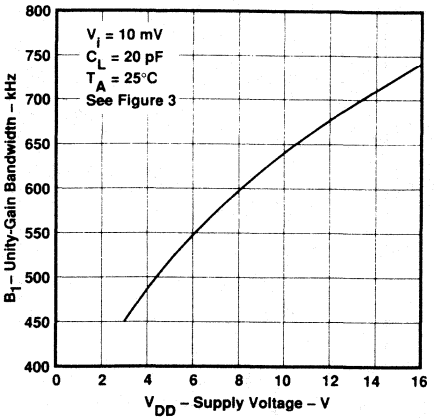


FIGURE 31

LARGE-SIGNAL DIFFERENTIAL VOLTAGE
AMPLIFICATION AND PHASE SHIFT
vs
FREQUENCY

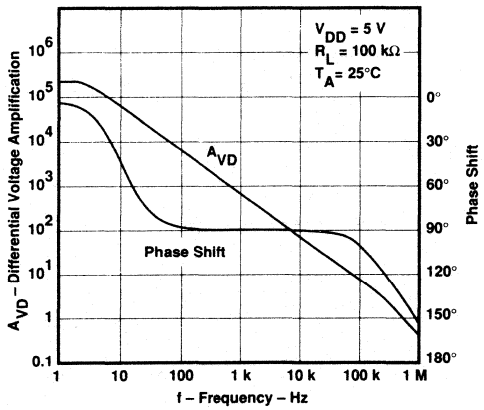


FIGURE 32

LARGE-SIGNAL DIFFERENTIAL VOLTAGE
AMPLIFICATION AND PHASE SHIFT
vs
FREQUENCY

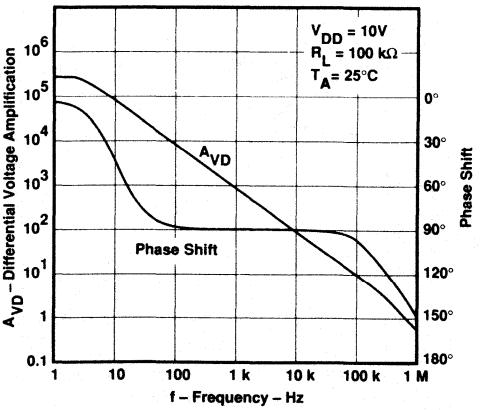


FIGURE 33

TYPICAL CHARACTERISTICS

PHASE MARGIN
vs
SUPPLY VOLTAGE

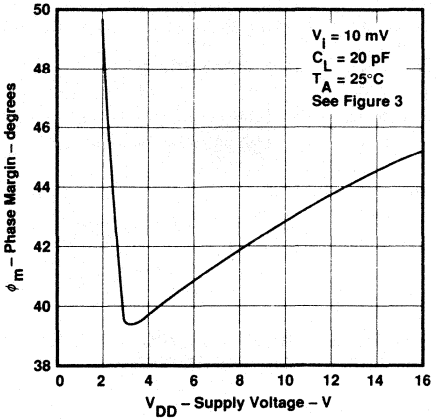


FIGURE 34

PHASE MARGIN
vs
FREE-AIR TEMPERATURE

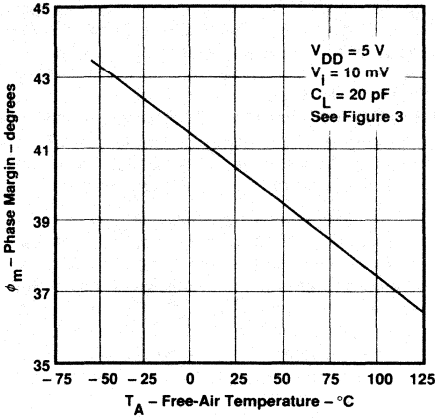


FIGURE 35

PHASE MARGIN
vs
CAPACITIVE LOAD

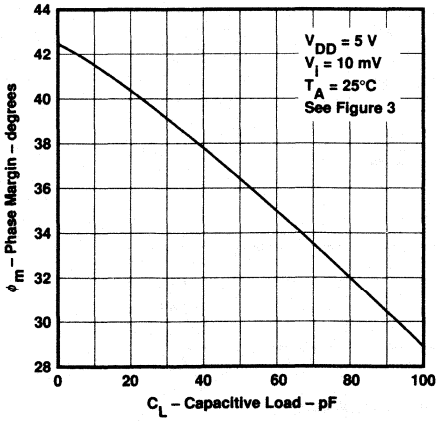


FIGURE 36

EQUIVALENT INPUT NOISE VOLTAGE
vs
FREQUENCY

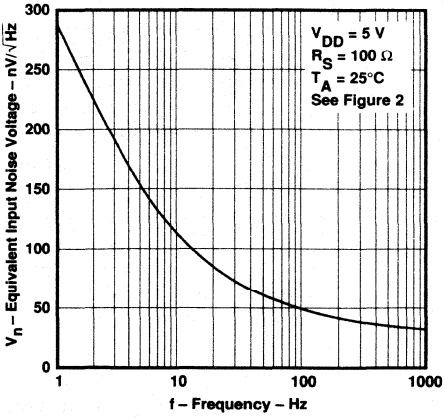


FIGURE 37

TYPICAL APPLICATION DATA

single-supply operation

While the TLC27M4 and TLC27M9 will perform well using dual power supplies (also called balanced or split supplies), the design is optimized for single-supply operation. This includes an input common mode voltage range that encompasses ground as well as an output voltage range that pulls down to ground. The supply voltage range extends down to 3 V (C- suffix types), thus allowing operation with supply levels commonly available for TTL and HCMOS; however, for maximum dynamic range, 16-V single-supply operation is recommended.

Many single-supply applications require that a voltage be applied to one input to establish a reference level that is above ground. A resistive voltage divider is usually sufficient to establish this reference level (see Figure 38). The low input bias current consumption of the TLC27M4 and TLC27M9 permits the use of very large resistive values to implement the voltage divider, thus minimizing power consumption.

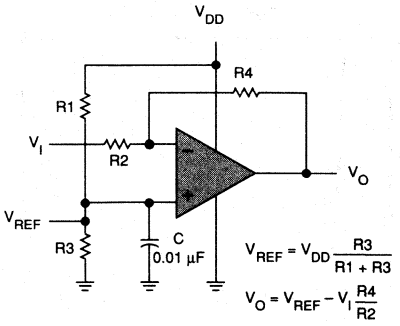
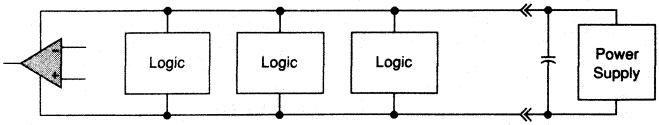


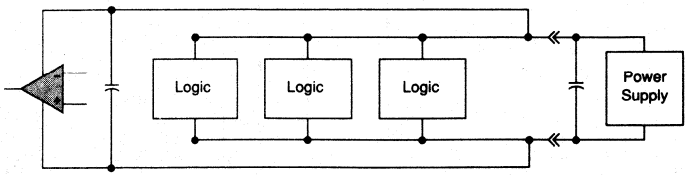
FIGURE 38. INVERTING AMPLIFIER WITH VOLTAGE REFERENCE

The TLC27M4 and TLC27M9 work well in conjunction with digital logic; however, when powering both linear devices and digital logic from the same power supply, the following precautions are recommended:

1. Power the linear devices from separate bypassed supply lines (see Figure 39); otherwise the linear device supply rails can fluctuate due to voltage drops caused by high switching currents in the digital logic.
2. Use proper bypass techniques to reduce the probability of noise-induced errors. Single capacitive decoupling is often adequate; however, RC decoupling may be necessary in high-frequency applications.



(a) Common Supply Rails



(b) Separate Bypassed Supply Rails (preferred)

FIGURE 39. COMMON VERSUS SEPARATE SUPPLY RAILS

TYPICAL APPLICATION DATA

input characteristics

The TLC27M4 and TLC27M9 are specified with a minimum and a maximum input voltage that, if exceeded at either input, could cause the device to malfunction. Exceeding this specified range is a common problem, especially in single-supply operation. Note that the lower range limit includes the negative rail, while the upper range limit is specified at V_{DD} – 1 V at T_A = 25°C and at V_{DD} – 1.5 V at all other temperatures.

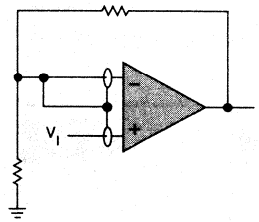
The use of the polysilicon-gate process and the careful input circuit design gives the TLC27M4 and TLC27M9 very good input offset voltage drift characteristics relative to conventional metal-gate processes. Offset voltage drift in CMOS devices is highly influenced by threshold voltage shifts caused by polarization of the phosphorus dopant implanted in the oxide. Placing the phosphorus dopant in a conductor (such as a polysilicon gate) alleviates the polarization problem, thus reducing threshold voltage shifts by more than an order of magnitude. The offset voltage drift with time has been calculated to be typically 0.1 μV/month, including the first month of operation.

Because of the extremely high input impedance and resulting low bias current requirements, the TLC27M4 and TLC27M9 are well suited for low-level signal processing; however, leakage currents on printed circuit boards and sockets can easily exceed bias current requirements and cause a degradation in device performance. It is good practice to include guard rings around inputs (similar to those of Figure 4 in the PARAMETER MEASUREMENT INFORMATION section). These guards should be driven from a low-impedance source at the same voltage level as the common-mode input (see Figure 40).

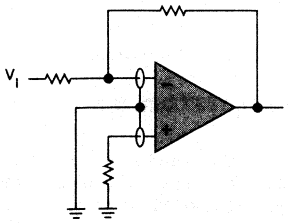
The inputs of any unused amplifiers should be tied to ground to avoid possible oscillation.

noise performance

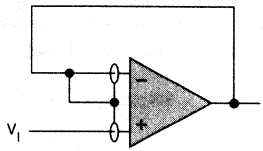
The noise specifications in op amp circuits are greatly dependent on the current in the first-stage differential amplifier. The low input bias current requirements of the TLC27M4 and TLC27M9 result in a very low noise current, which is insignificant in most applications. This feature makes the devices especially favorable over bipolar devices when using values of circuit impedance greater than 50 kΩ, since bipolar devices exhibit greater noise currents.



(a) Noninverting Amplifier



(b) Inverting Amplifier



(c) Unity Gain Amplifier

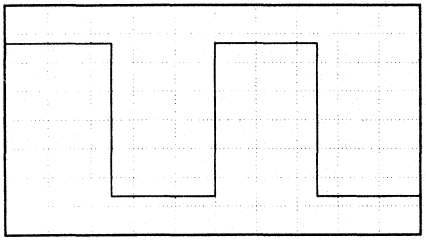
Figure 40. GUARD RING SCHEMES

TYPICAL APPLICATION DATA

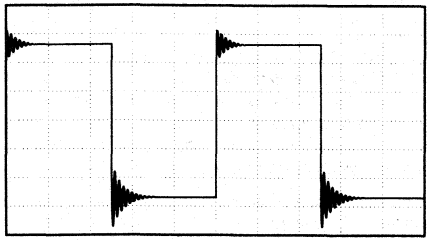
output characteristics

The output stage of the TLC27M4 and TLC27M9 is designed to sink and source relatively high amounts of current (see typical characteristics). If the output is subjected to a short-circuit condition, this high current capability can cause device damage under certain conditions. Output current capability increases with supply voltage.

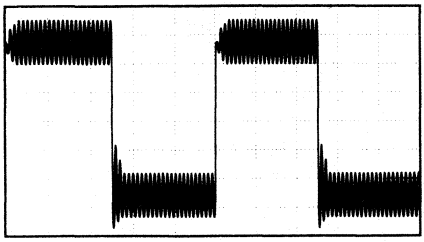
All operating characteristics of the TLC27M4 and TLC27M9 were measured using a 20-pF load. The devices will drive higher capacitive loads; however, as output load capacitance increases, the resulting response pole occurs at lower frequencies, thereby causing ringing, peaking, or even oscillation (see Figure 41). In many cases, adding some compensation in the form of a series resistor in the feedback loop will alleviate the problem.



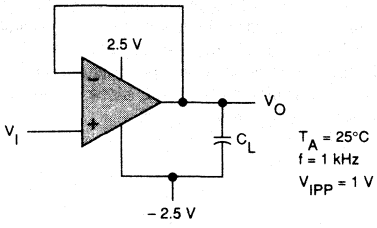
(a) C_L = 20 pF, R_L = no load



(b) C_L = 170 pF, R_L = no load



(c) C_L = 190 pF, R_L = no load



(d) Test Circuit

FIGURE 41. EFFECT OF CAPACITIVE LOADS AND TEST CIRCUIT

Although the TLC27M4 and TLC27M9 possess excellent high-level output voltage and current capability, methods are available for boosting this capability, if needed. The simplest method involves the use of a pullup resistor connected from the output to the positive supply rail. There are two disadvantages to the use of this circuit. First, the NMOS pull-down transistor, N4 (see Figure 42) must sink a comparatively large amount of current. In this circuit, N4 behaves like a linear resistor with an on resistance between approximately 60 Ω and 180 Ω, depending on how hard the op amp input is driven. With very low values of R6, a voltage offset from 0 V at the output will occur. Secondly, pullup resistor R6 acts as a drain load to N4 and the gain of the op amp is reduced at output voltage levels where N5 is not supplying the output current.

TYPICAL APPLICATION DATA

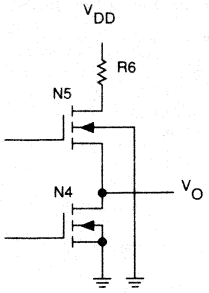


FIGURE 42. TLC27M4 / TLC27M9 OUTPUT STAGE

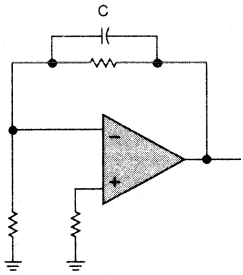


FIGURE 43. COMPENSATION FOR INPUT CAPACITANCE

feedback

Op amp circuits nearly always employ feedback, and since feedback is the first prerequisite for oscillation, a little caution is appropriate. Most oscillation problems result from driving capacitive loads (discussed previously) and ignoring stray input capacitance. A small-value capacitor connected in parallel with the feedback resistor is an effective remedy (see Figure 43). The value of this capacitor is optimized empirically.

electrostatic discharge protection

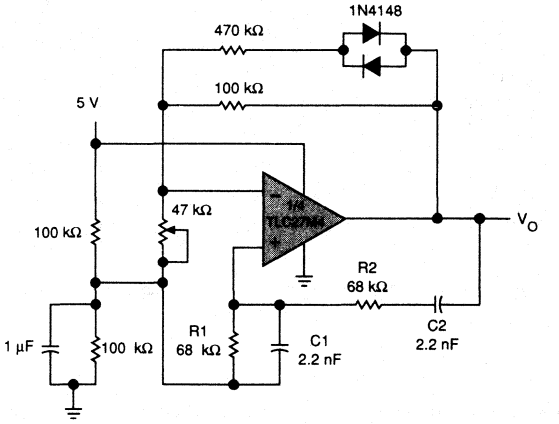
The TLC27M4 and TLC27M9 incorporate an internal electrostatic discharge (ESD) protection circuit that will prevent functional failures at voltages at or below 2000 V as tested under MIL-STD-883C, Method 3015.2. Care should be exercised, however, when handling these devices as exposure to ESD may result in the degradation of the device parametric performance. The protect circuit also causes the input bias currents to be temperature dependent and have the characteristics of a reverse-biased diode.

latchup

Because CMOS devices are susceptible to latchup due to their inherent parasitic thyristors, the TLC27M4 and TLC27M9 inputs and outputs were designed to withstand −100-mA surge currents without sustaining latchup; however, techniques should be used to reduce the chance of latchup whenever possible. Internal protection diodes should not by design be forward biased. Applied input and output voltage should not exceed the supply voltage by more than 300 mV. Care should be exercised when using capacitive coupling on pulse generators. Supply transients should be shunted by the use of decoupling capacitors (0.1 μF typical) located across the supply rails as close to the device as possible.

The current path established if latchup occurs is usually between the positive supply rail and ground and can be triggered by surges on the supply lines and / or voltages on either the output or inputs that exceed the supply voltage. Once latchup occurs, the current flow is limited only by the impedance of the power supply and the forward resistance of the parasitic thyristor and usually results in the destruction of the device. The chance of latchup occurring increases with increasing temperature and supply voltages.

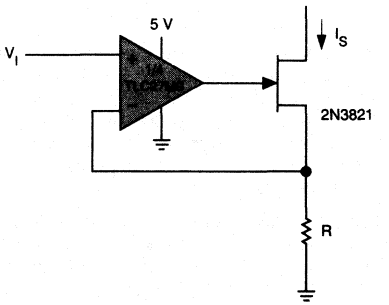
TYPICAL APPLICATION DATA



NOTES: $V_{OPP} \approx 2$ V

$$f_O = \frac{1}{2\pi\sqrt{R1R2C1C2}}$$

FIGURE 44. WIEN OSCILLATOR

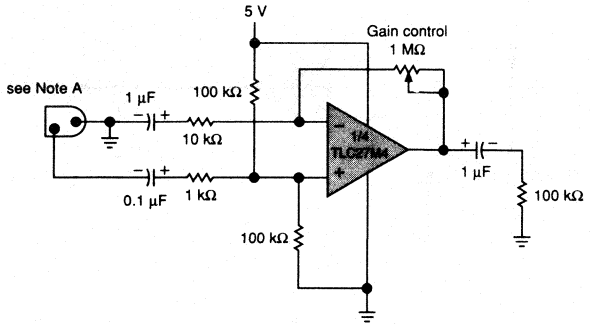


NOTES: $V_I = 0$ V TO 3 V

$$I_S = \frac{V_I}{R}$$

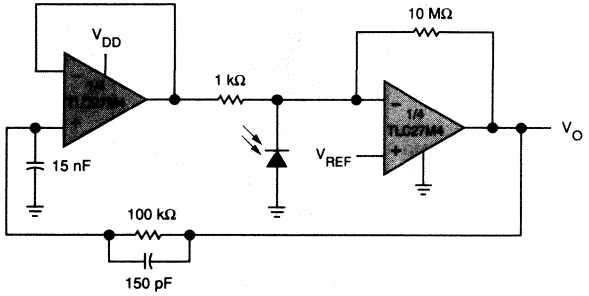
FIGURE 45. PRECISION LOW CURRENT SINK

TYPICAL APPLICATION DATA



NOTE A: Low to medium impedance dynamic mike

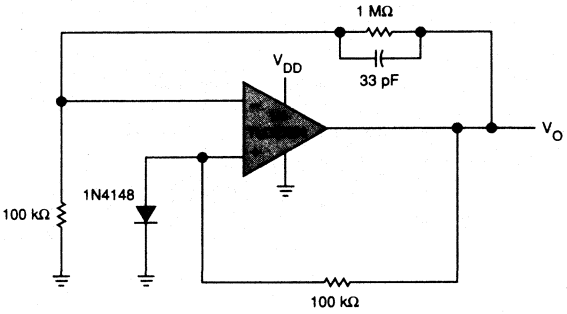
FIGURE 46. MICROPHONE PREAMPLIFIER



NOTES: V_{DD} = 4 V to 15 V
V_{REF} = 0 V to V_{DD} – 2 V

FIGURE 47. PHOTO DIODE AMPLIFIER WITH AMBIENT LIGHT REJECTION

TYPICAL APPLICATION DATA



NOTES: V_{DD} = 8 V to 16 V
V_O = 5 V, 10 mA

FIGURE 48. 5 V LOW POWER VOLTAGE REGULATOR

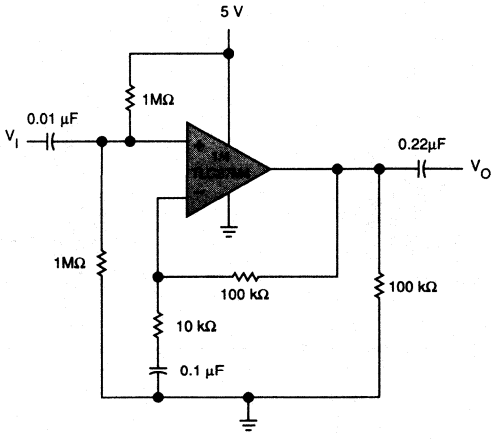
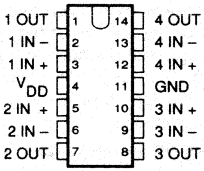


FIGURE 49. SINGLE RAIL A.C. AMPLIFIER

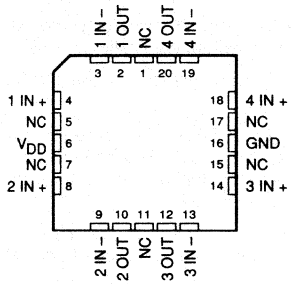
OCTOBER 1987

- **Trimmed Offset Voltage:**
  TLC27L9 . . . 900 μV Max at 25°C, V_{DD} = 5 V
- **Input Offset Voltage Drift Typically**
  0.1 μV / Month, Including the First 30 Days
- **Wide Range of Supply Voltages over Specified Temperature Range:**
  – 55°C to125°C . . . 4 V to 16 V
  – 40°C to 85°C . . . 4 V to 16 V
  0°C to 70°C . . . 3 V to 16 V
- **Single-Supply Operation**
- **Common-Mode Input Voltage Range Extends Below the Negative Rail (C- suffix, I- suffix types)**
- **Ultra-Low Power . . . 195 μW Typically at 25°C, V_{DD} = 5 V**
- **Output Voltage Range Includes Negative Rail**
- **High Input Impedance . . . 10^{12} Ω Typical**
- **ESD Protection Circuitry**
- **Small-Outline Package Option Also Available in Tape-and-Reel**
- **Designed-In Latchup Immunity**

N AND J DUAL-IN-LINE PACKAGE
D SMALL-OUTLINE PACKAGE
(TOP VIEW)



FK CHIP CARRIER PACKAGE
(TOP VIEW)



NC – No internal connection

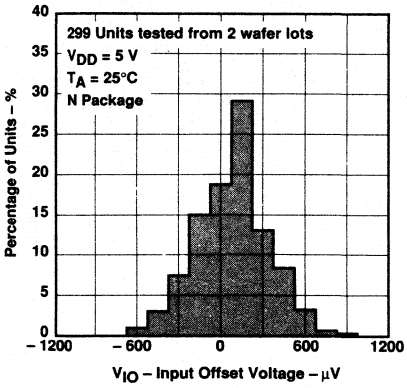
description

The TLC27L4 and TLC27L9 quad operational amplifiers combine a wide range of input offset voltage grades with low offset voltage drift, high input impedance, extremely low power, and high gain.

T_A	V_{IO}max at 25°C	PACKAGE			
		Small-Outline (D) See Note 1	Plastic DIP (N)	Ceramic DIP (J)	Chip Carrier (FK)
0°C to 70°C	900 μV	TLC27L9CD	TLC27L9CN	TLC27L9CJ	—
	2 mV	TLC27L4BCD	TLC27L4BCN	TLC27L4BCJ	—
	5 mV	TLC27L4ACD	TLC27L4ACN	TLC27L4ACJ	—
	10 mV	TLC27L4CD	TLC27L4CN	TLC27L4CJ	—
– 40°C to 85°C	900 μV	TLC27L9ID	TLC27L9IN	TLC27L9IJ	—
	2 mV	TLC27L4BID	TLC27L4BIN	TLC27L4BIJ	—
	5 mV	TLC27L4AID	TLC27L4AIN	TLC27L4AIJ	—
	10 mV	TLC27L4ID	TLC27L4IN	TLC27L4IJ	—
– 55°C to 125°C	900 μV	—	—	TLC27L9MJ	TLC27L9MFK
	10 mV	—	—	TLC27L4MJ	TLC27L4MFK

NOTE 1: Available in tape-and-reel. Add "R" suffix to the device type when ordering (e.g., TLC27L9CDR).

DISTRIBUTION OF TLC27L9
INPUT OFFSET VOLTAGE



LinCMOS is a trademark of Texas Instruments Incorporated

description (continued)

These devices use Texas Instruments silicon-gate LinCMOS technology, which provides offset voltage stability far exceeding the stability available with conventional metal-gate processes.

The extremely high input impedance, low bias currents, and low power consumption make these cost-effective devices ideal for high gain, low frequency, low power applications . Four offset voltage grades are available (C- suffix and I- suffix types), ranging from the low-cost TLC27L4 (10 mV) to the high-precision TLC27L9 (900 μV). These advantages, in combination with good common-mode rejection and supply voltage rejection, make these devices a good choice for new state-of-the-art designs as well as for upgrading existing designs.

In general, many features associated with bipolar technology are available on LinCMOS operational amplifiers, without the power penalties of bipolar technology. General applications such as transducer interfacing, analog calculations, amplifier blocks, active filters, and signal buffering are all easily designed with the TLC27L4 and TLC27L9. The devices also exhibit low voltage single supply operation and ultra-low power consumption making them ideally suited for remote and inaccessible battery-powered applications. The common-mode input voltage range includes the negative rail.

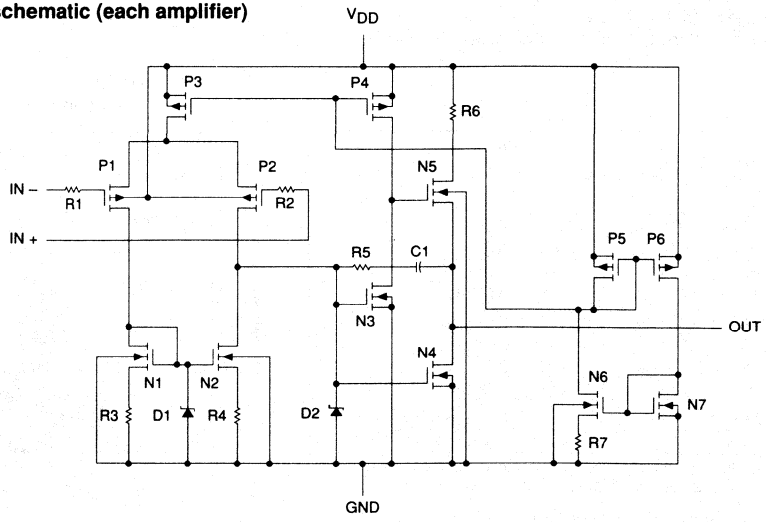
A wide range of packaging options is available, including small outline and chip carrier versions for high-density system applications.

The device inputs and outputs are designed to withstand −100-mA surge currents without sustaining latchup.

The TLC27L4 and TLC27L9 incorporate internal ESD protection circuits that will prevent functional failures at voltages up to 2000 V as tested under MIL-STD-883C, Method 3015.2; however, care should be exercised in handling these devices as exposure to ESD may result in the degradation of the device parametric performance.

The M- suffix devices are characterized for operation over the full military temperature range of −55°C to 125°C, the I- suffix devices from −40°C to 85°C, and the C- suffix devices from 0°C to 70°C.

equivalent schematic (each amplifier)



absolute maximum ratings over operating free-air temperature (unless otherwise noted)

Supply voltage, V_{DD} (see Note 2) . . . . . 18 V
Differential input voltage (see Note 3) . . . . . $\pm V_{DD}$
Input voltage range, V_I (any input) . . . . . −0.3 V to V_{DD}
Input current, I_I . . . . . ±5 mA
Output current, I_O (each output) . . . . . ±30 mA
Total current into V_{DD} terminal . . . . . 45 mA
Total current out of ground terminal . . . . . 45 mA
Duration of short-circuit current at (or below) 25°C (see Note 4) . . . . . Unlimited
Continuous total dissipation . . . . . See Dissipation Rating Table
Operating free-air temperature, T_A: C-suffix types . . . . . 0°C to 70°C
I-suffix types . . . . . −40°C to 85°C
M-suffix types . . . . . −55°C to 125°C
Storage temperature range . . . . . −65°C to 150°C
Case temperature for 60 seconds: FK package . . . . . 260°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds: J package . . . . . 300°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: D and N package . . . . . 260°C

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING	$T_A = 85°C$ POWER RATING	$T_A = 125°C$ POWER RATING
D	950 mW	7.6 mW/°C	608 mW	494 mW	
FK	1375 mW	11 mW/°C	880 mW	715 mW	275 mW
J (C-, I- suffix)	1025 mW	8.2 mW/°C	656 mW	533 mW	
J (M- suffix)	1375 mW	11 mW/°C	880 mW	715 mW	275 mW
N	1575 mW	12.6 mW/°C	1008 mW	819 mW	

recommended operating conditions

		M- SUFFIX TYPES			I- SUFFIX TYPES			C- SUFFIX TYPES			
		MIN	NOM	MAX	MIN	NOM	MAX	MIN	NOM	MAX	UNIT
Supply voltage, V_{DD}		4		16	4		16	3		16	V
Common-mode input voltage, V_{IC}	$V_{DD} = 5$ V	0		3.5	−0.2		3.5	−0.2		3.5	V
	$V_{DD} = 10$ V	0		8.5	−0.2		8.5	−0.2		8.5	V
Input voltage, V_I	$V_{DD} = 5$ V	0		3.5	−0.2		3.5	−0.2		3.5	V
	$V_{DD} = 10$ V	0		8.5	−0.2		8.5	−0.2		8.5	V
Operating free-air temperature, T_A		−55		125	−40		85	0		70	°C

NOTES: 2. All voltage values, except differential voltages, are with respect to network ground.
3. Differential voltages are at the noninverting input with respect to the inverting input.
4. The output may be shorted to either supply. Temperature and/or supply voltages must be limited to ensure that the maximum dissipation rating is not exceeded (see application section).

electrical characteristics at specified free-air temperature, V_{DD} = 5 V (unless otherwise noted)

PARAMETER			TEST CONDITIONS		C- SUFFIX TYPES MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage	TLC27L4C	V_O = 1.4 V, V_{IC} = 0 V, R_S = 50 Ω, R_L = 1 MΩ	25°C		1.1	10	mV
				Full range			12	
		TLC27L4AC	V_O = 1.4 V, V_{IC} = 0 V, R_S = 50 Ω, R_L = 1 MΩ	25°C		0.9	5	
				Full range			6.5	
		TLC27L4BC	V_O = 1.4 V, V_{IC} = 0 V, R_S = 50 Ω, R_L = 1 MΩ	25°C		240	2000	μV
				Full range			3000	
		TLC27L9C	V_O = 1.4 V, V_{IC} = 0 V, R_S = 50 Ω, R_L = 1 MΩ	25°C		200	900	
				Full range			1500	
α_{VIO}	Average temperature coefficient of input offset voltage			25°C to 70°C		1.1		μV/°C
I_{IO}	Input offset current (see Note 5)		V_{IC} = 2.5 V, V_O = 2.5 V	25°C		0.1		pA
				70°C		7	300	
I_{IB}	Input bias current (see Note 5)		V_{IC} = 2.5 V, V_O = 2.5 V	25°C		0.6		pA
				70°C		40	600	
V_{ICR}	Common-mode input voltage range (see Note 6)			25°C	−0.2 to 4	−0.3 to 4.2		V
				Full range	−0.2 to 3.5			V
V_{OH}	High-level output voltage		V_{ID} = 100 mV, R_L = 1 MΩ	25°C	3.2	4.1		V
				70°C	3	4.2		
				0°C	3	4.1		
V_{OL}	Low-level output voltage		V_{ID} = −100 mV, I_{OL} = 0	25°C		0	50	mV
				70°C		0	50	
				0°C		0	50	
A_{VD}	Large-signal differential voltage amplification		V_O = 0.25 V to 2 V, R_L = 1 MΩ	25°C	50	480		V/mV
				70°C	50	380		
				0°C	50	700		
CMRR	Common-mode rejection ratio		V_{IC} = V_{ICR} min	25°C	65	94		dB
				70°C	60	95		
				0°C	60	95		
k_{SVR}	Supply-voltage rejection ratio (ΔV_{DD} / ΔV_{IO})		V_{DD} = 5 V to 10 V, V_O = 1.4 V	25°C	70	97		dB
				70°C	60	98		
				0°C	60	97		
I_{DD}	Supply current (four amplifiers)		No load, V_O = 2.5 V, V_{IC} = 2.5 V	25°C		39	68	μA
				70°C		31	56	
				0°C		48	84	

NOTES: 5. The typical values of input bias current and input offset current below 5 pA were determined mathematically.
6. This range also applies to each input individually.

electrical characteristics at specified free-air temperature, V_{DD} = 10 V (unless otherwise noted)

PARAMETER			TEST CONDITIONS		C- SUFFIX TYPES MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage	TLC27L4C	V_O = 1.4 V, V_{IC} = 0 V, R_S = 50 Ω, R_L = 1 MΩ	25°C		1.1	10	mV
				Full range			12	
		TLC27L4AC	V_O = 1.4 V, V_{IC} = 0 V, R_S = 50 Ω, R_L = 1 MΩ	25°C		0.9	5	
				Full range			6.5	
		TLC27L4BC	V_O = 1.4 V, V_{IC} = 0 V, R_S = 50 Ω, R_L = 1 MΩ	25°C		260	2000	μV
				Full range			3000	
		TLC27L9C	V_O = 1.4 V, V_{IC} = 0 V, R_S = 50 Ω, R_L = 1 MΩ	25°C		210	1200	
				Full range			1900	
α_{VIO}	Average temperature coefficient of input offset voltage			25°C to 70°C		1		μV/°C
I_{IO}	Input offset current (see Note 5)		V_{IC} = 5 V, V_O = 5 V	25°C		0.1		pA
				70°C		8	300	
I_{IB}	Input bias current (see Note 5)		V_{IC} = 5 V, V_O = 5 V	25°C		0.7		pA
				70°C		50	600	
V_{ICR}	Common-mode input voltage range (see Note 6)			25°C	−0.2 to 9	−0.3 to 9.2		V
				Full range	−0.2 to 8.5			V
V_{OH}	High-level output voltage		V_{ID} = 100 mV, R_L = 1 MΩ	25°C	8	8.9		V
				70°C	7.8	8.9		
				0°C	7.8	8.9		
V_{OL}	Low-level output voltage		V_{ID} = −100 mV, I_{OL} = 0	25°C		0	50	mV
				70°C		0	50	
				0°C		0	50	
A_{VD}	Large-signal differential voltage amplification		V_O = 1 V to 6 V, R_L = 1 MΩ	25°C	50	800		V/mV
				70°C	50	660		
				0°C	50	1100		
CMRR	Common-mode rejection ratio		V_{IC} = V_{ICR} min	25°C	65	97		dB
				70°C	60	97		
				0°C	60	97		
k_{SVR}	Supply-voltage rejection ratio (ΔV_{DD} / ΔV_{IO})		V_{DD} = 5 V to 10 V, V_O = 1.4 V	25°C	70	97		dB
				70°C	60	98		
				0°C	60	97		
I_{DD}	Supply current (four amplifiers)		No load, V_O = 5 V, V_{IC} = 5 V	25°C		57	92	μA
				70°C		44	80	
				0°C		72	132	

NOTES: 5. The typical values of input bias current and input offset current below 5 pA were determined mathematically.
6. This range also applies to each input individually.

electrical characteristics at specified free-air temperature, V_{DD} = 5 V (unless otherwise noted)

PARAMETER			TEST CONDITIONS		I-SUFFIX TYPES MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage	TLC27L4I	V_O = 1.4 V, V_{IC} = 0 V, R_S = 50 Ω, R_L = 1 MΩ	25°C		1.1	10	mV
				Full range			13	
		TLC27L4AI	V_O = 1.4 V, V_{IC} = 0 V, R_S = 50 Ω, R_L = 1 MΩ	25°C		0.9	5	
				Full range			7	
		TLC27L4BI	V_O = 1.4 V, V_{IC} = 0 V, R_S = 50 Ω, R_L = 1 MΩ	25°C		240	2000	μV
				Full range			3500	
		TLC27L9I	V_O = 1.4 V, V_{IC} = 0 V, R_S = 50 Ω, R_L = 1 MΩ	25°C		200	900	
				Full range			2000	
α_{VIO}	Average temperature coefficient of input offset voltage			25°C to 85°C		1.1		μV/°C
I_{IO}	Input offset current (see Note 5)		V_{IC} = 2.5 V, V_O = 2.5 V	25°C		0.1		pA
				85°C		24	1000	
I_{IB}	Input bias current (see Note 5)		V_{IC} = 2.5 V, V_O = 2.5 V	25°C		0.6		pA
				85°C		200	2000	
V_{ICR}	Common-mode input voltage range (see Note 6)			25°C	−0.2 to 4	−0.3 to 4.2		V
				Full range	−0.2 to 3.5			V
V_{OH}	High-level output voltage		V_{ID} = 100 mV, R_L = 1 MΩ	25°C	3.2	4.1		V
				85°C	3	4.2		
				−40°C	3	4.1		
V_{OL}	Low-level output voltage		V_{ID} = −100 mV, I_{OL} = 0	25°C		0	50	mV
				85°C		0	50	
				−40°C		0	50	
A_{VD}	Large-signal differential voltage amplification		V_O = 0.25 V to 2 V, R_L = 1 MΩ	25°C	50	480		V/mV
				85°C	50	330		
				−40°C	50	900		
CMRR	Common-mode rejection ratio		V_{IC} = V_{ICR} min	25°C	65	94		dB
				85°C	60	95		
				−40°C	60	95		
k_{SVR}	Supply-voltage rejection ratio (ΔV_{DD} / ΔV_{IO})		V_{DD} = 5 V to 10 V, V_O = 1.4 V	25°C	70	97		dB
				85°C	60	98		
				−40°C	60	97		
I_{DD}	Supply current (four amplifiers)		No load, V_O = 2.5 V, V_{IC} = 2.5 V	25°C		39	68	μA
				85°C		29	52	
				−40°C		62	108	

NOTES: 5. The typical values of input bias current and input offset current below 5 pA were determined mathematically.
6. This range also applies to each input individually.

electrical characteristics at specified free-air temperature, V_{DD} = 10 V (unless otherwise noted)

PARAMETER			TEST CONDITIONS		I- SUFFIX TYPES MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage	TLC27L4I	V_O = 1.4 V, V_{IC} = 0 V, R_S = 50 Ω, R_L = 1 MΩ	25°C		1.1	10	mV
				Full range			13	
		TLC27L4AI	V_O = 1.4 V, V_{IC} = 0 V, R_S = 50 Ω, R_L = 1 MΩ	25°C		0.9	5	
				Full range			7	
		TLC27L4BI	V_O = 1.4 V, V_{IC} = 0 V, R_S = 50 Ω, R_L = 1 MΩ	25°C		260	2000	µV
				Full range			3500	
		TLC27L9I	V_O = 1.4 V, V_{IC} = 0 V, R_S = 50 Ω, R_L = 1 MΩ	25°C		210	1200	
				Full range			2900	
α_{VIO}	Average temperature coefficient of input offset voltage			25°C to 85°C		1		µV/°C
I_{IO}	Input offset current (see Note 5)		V_{IC} = 5 V, V_O = 5 V	25°C		0.1		pA
				85°C		26	1000	
I_{IB}	Input bias current (see Note 5)		V_{IC} = 5 V, V_O = 5 V	25°C		0.7		pA
				85°C		220	2000	
V_{ICR}	Common-mode input voltage range (see Note 6)			25°C	−0.2 to 9	−0.3 to 9.2		V
				Full range	−0.2 to 8.5			V
V_{OH}	High-level output voltage		V_{ID} = 100 mV, R_L = 1 MΩ	25°C	8	8.9		V
				85°C	7.8	8.9		
				−40°C	7.8	8.9		
V_{OL}	Low-level output voltage		V_{ID} = −100 mV, I_{OL} = 0	25°C		0	50	mV
				85°C		0	50	
				−40°C		0	50	
A_{VD}	Large-signal differential voltage amplification		V_O = 1 V to 6 V, R_L = 1 MΩ	25°C	50	800		V/mV
				85°C	50	585		
				−40°C	50	1550		
CMRR	Common-mode rejection ratio		V_{IC} = V_{ICR} min	25°C	65	97		dB
				85°C	60	98		
				−40°C	60	97		
k_{SVR}	Supply-voltage rejection ratio (ΔV_{DD} / ΔV_{IO})		V_{DD} = 5 V to 10 V, V_O = 1.4 V	25°C	70	97		dB
				85°C	60	98		
				−40°C	60	97		
I_{DD}	Supply current (four amplifiers)		No load, V_O = 5 V, V_{IC} = 5 V	25°C		57	92	µA
				85°C		40	72	
				−40°C		98	172	

NOTES: 5. The typical values of input bias current and input offset current below 5 pA were determined mathematically.
6. This range also applies to each input individually.

electrical characteristics at specified free-air temperature, V_{DD} = 5 V (unless otherwise noted)

PARAMETER			TEST CONDITIONS		M- SUFFIX TYPES MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage	TLC27L4M	V_O = 1.4 V, V_{IC} = 0 V, R_S = 50 Ω, R_L = 1 MΩ	25°C		1.1	10	mV
				Full range			12	
		TLC27L9M	V_O = 1.4 V, V_{IC} = 0 V, R_S = 50 Ω, R_L = 1 MΩ	25°C		200	900	μV
				Full range			3750	
α_{VIO}	Average temperature coefficient of input offset voltage			25°C to 125°C		1.4		μV/°C
I_{IO}	Input offset current (see Note 5)		V_{IC} = 2.5 V, V_O = 2.5 V	25°C		0.1		pA
				125°C		1.4	15	nA
I_{IB}	Input bias current (see Note 5)		V_{IC} = 2.5 V, V_O = 2.5 V	25°C		0.6		pA
				125°C		9	35	nA
V_{ICR}	Common-mode input voltage range (see Note 6)			25°C	0 to 4	−0.3 to 4.2		V
				Full range	0 to 3.5			V
V_{OH}	High-level output voltage		V_{ID} = 100 mV, R_L = 1 MΩ	25°C	3.2	4.1		V
				125°C	3	4.2		
				−55°C	3	4.1		
V_{OL}	Low-level output voltage		V_{ID} = −100 mV, I_{OL} = 0	25°C		0	50	mV
				125°C		0	50	
				−55°C		0	50	
A_{VD}	Large-signal differential voltage amplification		V_O = 0.25 V to 2 V, R_L = 1 MΩ	25°C	50	480		V/mV
				125°C	25	200		
				−55°C	25	950		
CMRR	Common-mode rejection ratio		V_{IC} = V_{ICR} min	25°C	65	94		dB
				125°C	60	85		
				−55°C	60	95		
k_{SVR}	Supply-voltage rejection ratio (ΔV_{DD} / ΔV_{IO})		V_{DD} = 5 V to 10 V, V_O = 1.4 V	25°C	70	97		dB
				125°C	60	98		
				−55°C	60	97		
I_{DD}	Supply current (four amplifiers)		No load, V_O = 2.5 V, V_{IC} = 2.5 V	25°C		39	68	μA
				125°C		27	48	
				−55°C		69	120	

NOTES: 5. The typical values of input bias current and input offset current below 5 pA were determined mathematically.
6. This range also applies to each input individually.

electrical characteristics at specified free-air temperature, V_{DD} = 10 V (unless otherwise noted)

PARAMETER			TEST CONDITIONS		M- SUFFIX TYPES MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage	TLC27L4M	V_O = 1.4 V, V_{IC} = 0 V, R_S = 50 Ω, R_L = 1 MΩ	25°C		1.1	10	mV
				Full range			12	
		TLC27L9M	V_O = 1.4 V, V_{IC} = 0 V, R_S = 50 Ω, R_L = 1 MΩ	25°C		210	1200	μV
				Full range			4300	
α_{VIO}	Average temperature coefficient of input offset voltage			25°C to 125°C		1.4		μV/°C
I_{IO}	Input offset current (see Note 5)		V_{IC} = 5 V, V_O = 5 V	25°C		0.1		pA
				125°C		1.8	15	nA
I_{IB}	Input bias current (see Note 5)		V_{IC} = 5 V, V_O = 5 V	25°C		0.7		pA
				125°C		10	35	nA
V_{ICR}	Common-mode input voltage range (see Note 6)			25°C	0 to 9	−0.3 to 9.2		V
				Full range	0 to 8.5			V
V_{OH}	High-level output voltage		V_{ID} = 100 mV, R_L = 1 MΩ	25°C	8	8.9		V
				125°C	7.8	9		
				−55°C	7.8	8.8		
V_{OL}	Low-level output voltage		V_{ID} = −100 mV, I_{OL} = 0	25°C		0	50	mV
				125°C		0	50	
				−55°C		0	50	
A_{VD}	Large-signal differential voltage amplification		V_O = 1 V to 6 V, R_L = 1 MΩ	25°C	50	800		V/mV
				125°C	25	380		
				−55°C	25	1750		
CMRR	Common-mode rejection ratio		V_{IC} = V_{ICR} min	25°C	65	97		dB
				125°C	60	91		
				−55°C	60	97		
k_{SVR}	Supply-voltage rejection ratio (ΔV_{DD} / ΔV_{IO})		V_{DD} = 5 V to 10 V, V_O = 1.4 V	25°C	70	97		dB
				125°C	60	98		
				−55°C	60	97		
I_{DD}	Supply current (four amplifiers)		No load, V_O = 5 V, V_{IC} = 5 V	25°C		57	92	μA
				125°C		35	60	
				−55°C		111	192	

NOTES: 5. The typical values of input bias current and input offset current below 5 pA were determined mathematically.
6. This range also applies to each input individually.

operating characteristics, V_{DD} = 5 V

PARAMETER		TEST CONDITIONS			C- SUFFIX TYPES MIN	C- SUFFIX TYPES TYP	C- SUFFIX TYPES MAX	UNIT
SR	Slew rate at unity gain	R_L = 1 MΩ, C_L = 20 pF, See Figure 1	V_{IPP} = 1 V	25°C		0.03		V/μs
				70°C		0.03		
				0°C		0.04		
			V_{IPP} = 2.5 V	25°C		0.03		
				70°C		0.02		
				0°C		0.03		
V_n	Equivalent input noise voltage	f = 1 kHz, R_S = 100 Ω, See Figure 2		25°C		68		nV/√Hz
B_{OM}	Maximum output swing bandwidth	$V_O = V_{OH}$, C_L = 20 pF, R_L = 1 MΩ, See Figure 1		25°C		5		kHz
				70°C		4.5		
				0°C		6		
B_1	Unity-gain bandwidth	V_i = 10 mV, C_L = 20 pF, See Figure 3		25°C		85		kHz
				70°C		65		
				0°C		100		
ϕ_m	Phase margin	f = B_1, V_i = 10 mV, C_L = 20 pF, See Figure 3		25°C		34°		
				70°C		30°		
				0°C		36°		

operating characteristics, V_{DD} = 10 V

PARAMETER		TEST CONDITIONS			C- SUFFIX TYPES MIN	C- SUFFIX TYPES TYP	C- SUFFIX TYPES MAX	UNIT
SR	Slew rate at unity gain	R_L = 1 MΩ, C_L = 20 pF, See Figure 1	V_{IPP} = 1 V	25°C		0.05		V/μs
				70°C		0.04		
				0°C		0.05		
			V_{IPP} = 5.5 V	25°C		0.04		
				70°C		0.04		
				0°C		0.05		
V_n	Equivalent input noise voltage	f = 1 kHz, R_S = 100 Ω, See Figure 2		25°C		68		nV/√Hz
B_{OM}	Maximum output swing bandwidth	$V_O = V_{OH}$, C_L = 20 pF, R_L = 1 MΩ, See Figure 1		25°C		1		kHz
				70°C		0.9		
				0°C		1.3		
B_1	Unity-gain bandwidth	V_i = 10 mV, C_L = 20 pF, See Figure 3		25°C		110		kHz
				70°C		90		
				0°C		125		
ϕ_m	Phase margin	f = B_1, V_i = 10 mV, C_L = 20 pF, See Figure 3		25°C		38°		
				70°C		34°		
				0°C		40°		

operating characteristics, V_{DD} = 5 V

PARAMETER		TEST CONDITIONS			I- SUFFIX TYPES MIN	TYP	MAX	UNIT
SR	Slew rate at unity gain	R_L = 1 MΩ, C_L = 20 pF, See Figure 1	V_{IPP} = 1 V	25°C		0.03		V/μs
				85°C		0.03		
				−40°C		0.04		
			V_{IPP} = 2.5 V	25°C		0.03		
				85°C		0.02		
				−40°C		0.04		
V_n	Equivalent input noise voltage	f = 1 kHz, R_S = 100 Ω, See Figure 2		25°C		68		nV/√Hz
B_{OM}	Maximum output swing bandwidth	V_O = V_{OH}, R_L = 1 MΩ,	C_L = 20 pF, See Figure 1	25°C		5		kHz
				85°C		4		
				−40°C		7		
B_1	Unity-gain bandwidth	V_i = 10 mV, C_L = 20 pF,	See Figure 3	25°C		85		kHz
				85°C		55		
				−40°C		130		
ϕ_m	Phase margin	f = B_1, V_i = 10 mV, C_L = 20 pF,	See Figure 3	25°C		34°		
				85°C		28°		
				−40°C		38°		

operating characteristics, V_{DD} = 10 V

PARAMETER		TEST CONDITIONS			I- SUFFIX TYPES MIN	TYP	MAX	UNIT
SR	Slew rate at unity gain	R_L = 1 MΩ, C_L = 20 pF, See Figure 1	V_{IPP} = 1 V	25°C		0.05		V/μs
				85°C		0.03		
				−40°C		0.06		
			V_{IPP} = 5.5 V	25°C		0.04		
				85°C		0.03		
				−40°C		0.05		
V_n	Equivalent input noise voltage	f = 1 kHz, R_S = 100 Ω, See Figure 2		25°C		68		nV/√Hz
B_{OM}	Maximum output swing bandwidth	V_O = V_{OH}, R_L = 1 MΩ,	C_L = 20 pF, See Figure 1	25°C		1		kHz
				85°C		0.8		
				−40°C		1.4		
B_1	Unity-gain bandwidth	V_i = 10 mV, C_L = 20 pF,	See Figure 3	25°C		110		kHz
				85°C		80		
				−40°C		155		
ϕ_m	Phase margin	f = B_1, V_i = 10 mV, C_L = 20 pF,	See Figure 3	25°C		38°		
				85°C		32°		
				−40°C		42°		

operating characteristics, V_{DD} = 5 V

PARAMETER		TEST CONDITIONS			M- SUFFIX TYPES MIN	M- SUFFIX TYPES TYP	M- SUFFIX TYPES MAX	UNIT
SR	Slew rate at unity gain	R_L = 1 MΩ, C_L = 20 pF, See Figure 1	V_{IPP} = 1 V	25°C		0.03		V/μs
				125°C		0.02		
				– 55°C		0.04		
			V_{IPP} = 2.5 V	25°C		0.03		
				125°C		0.02		
				– 55°C		0.04		
V_n	Equivalent input noise voltage	f = 1 kHz, See Figure 2	R_S = 100 Ω,	25°C		68		nV/√Hz
B_{OM}	Maximum output swing bandwidth	$V_O = V_{OH}$, R_L = 1 MΩ,	C_L = 20 pF, See Figure 1	25°C		5		kHz
				125°C		3		
				– 55°C		8		
B_1	Unity-gain bandwidth	V_i = 10 mV, C_L = 20 pF,	See Figure 3	25°C		85		kHz
				125°C		45		
				– 55°C		140		
ϕ_m	Phase margin	f = B_1, V_i = 10 mV, C_L = 20 pF,	See Figure 3	25°C		34°		
				125°C		25°		
				– 55°C		39°		

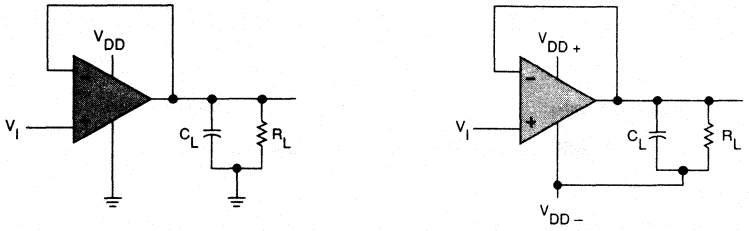
operating characteristics, V_{DD} = 10 V

PARAMETER		TEST CONDITIONS			M- SUFFIX TYPES MIN	M- SUFFIX TYPES TYP	M- SUFFIX TYPES MAX	UNIT
SR	Slew rate at unity gain	R_L = 1 MΩ, C_L = 20 pF, See Figure 1	V_{IPP} = 1 V	25°C		0.05		V/μs
				125°C		0.03		
				– 55°C		0.06		
			V_{IPP} = 5.5 V	25°C		0.04		
				125°C		0.03		
				– 55°C		0.06		
V_n	Equivalent input noise voltage	f = 1 kHz, See Figure 2	R_S = 100 Ω,	25°C		68		nV/√Hz
B_{OM}	Maximum output swing bandwidth	$V_O = V_{OH}$, R_L = 1 MΩ,	C_L = 20 pF, See Figure 1	25°C		1		kHz
				125°C		0.7		
				– 55°C		1.5		
B_1	Unity-gain bandwidth	V_i = 10 mV, C_L = 20 pF,	See Figure 3	25°C		110		kHz
				125°C		70		
				– 55°C		165		
ϕ_m	Phase margin	f = B_1, V_i = 10 mV, C_L = 20 pF,	See Figure 3	25°C		38°		
				125°C		29°		
				– 55°C		43°		

PARAMETER MEASUREMENT INFORMATION

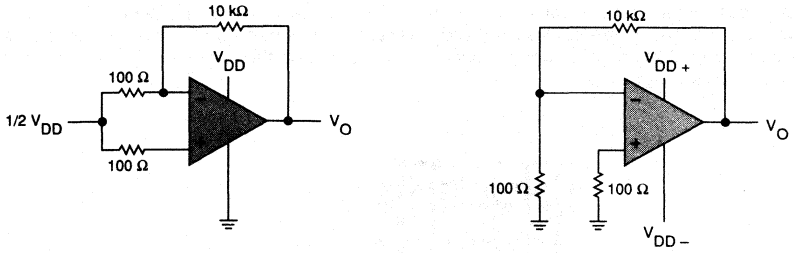
single-supply versus split-supply test circuits

Because the TLC27L4 and TLC27L9 are optimized for single-supply operation, circuit configurations used for the various tests often present some inconvenience since the input signal, in many cases, must be offset from ground. This inconvenience can be avoided by testing the device with split supplies and the output load tied to the negative rail. A comparison of single-supply versus split-supply test circuits is shown below. The use of either circuit will give the same result.



(a) Single-Supply (b) Split-Supply

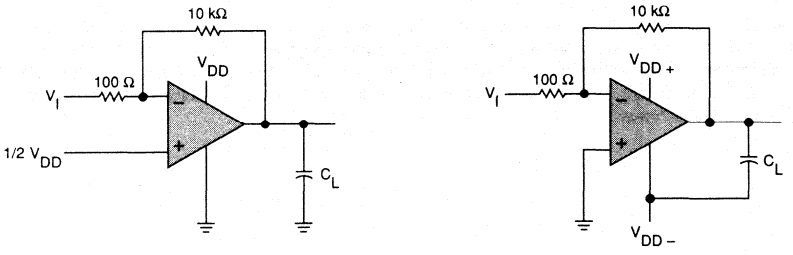
FIGURE 1. UNITY-GAIN AMPLIFIER



(a) Single-Supply (b) Split-Supply

FIGURE 2. NOISE TEST CIRCUIT

PARAMETER MEASUREMENT INFORMATION



(a) Single-Supply (b) Split-Supply

FIGURE 3. GAIN-OF-100 INVERTING AMPLIFIER

input bias current

Because of the high input impedance of the TLC27L4 and TLC27L9 op amps, attempts to measure the input bias current can result in erroneous readings. The typical bias current at normal room ambient temperature is typically less than 1 pA, a value that is easily exceeded by leakages on the test socket. Two suggestions are offered to avoid erroneous measurements:

1 Isolate the device from other potential leakage sources. Use a grounded shield around and between the device inputs (see Figure 4). Leakages that would otherwise flow to the inputs will be shunted away.

2 Compensate for the leakage of the test socket by actually performing an input bias current test (using a picoammeter) with no device in the test socket. The actual input bias current can then be calculated by subtracting the "open-socket" leakage readings from the readings obtained with a device in the test socket.

One word of caution . . . many automatic testers as well as some bench-top op amp testers use the servo-loop technique with a resistor in series with the device input to measure the input bias current (the voltage drop across the series resistor is measured and the bias current is calculated). This method requires that a device be inserted into the test socket to obtain a correct reading; therefore, an "open-socket" reading is not feasible using this method.

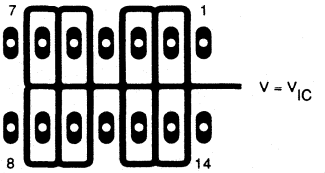


FIGURE 4. ISOLATION METAL AROUND DEVICE INPUTS (N AND J DUAL-IN-LINE PACKAGE)

PARAMETER MEASUREMENT INFORMATION

low-level output voltage

To obtain low-supply-voltage operation, some compromise was necessary in the input stage. This compromise results in the device low-level output being dependent on both the common-mode input voltage level as well as the differential input voltage level. When attempting to correlate low-level output readings with those quoted in the electrical specifications, these two conditions should be observed. If conditions other than these are to be used, please refer to Figures 14 thru 19 in the Typical Characteristics section of this data sheet.

input offset voltage temperature coefficient

Erroneous readings often result from attempts to measure temperature coefficient of input offset voltage. This parameter is actually a calculation using input offset voltage measurements obtained at two different temperatures. When one (or both) of the temperatures is below freezing, moisture can collect on both the device and the test socket. This moisture will result in leakage and contact resistance which can cause erroneous input offset voltage readings. The isolation techniques previously mentioned have no affect on the leakage since the moisture also covers the isolation metal itself, thereby rendering it useless. It is suggested that these measurements be performed at temperatures above freezing to minimize error.

full power response

Full power response, the frequency above which the op amp slew rate limits the output voltage swing, is often specified two ways . . . full-linear response and full-peak response. The full-linear response is generally measured by monitoring the distortion level of the output while increasing the frequency of a sinusoidal input signal until the maximum frequency is found above which the output contains significant distortion. The full-peak response is defined as the maximum output frequency, without regard to distortion, above which full peak-to-peak output swing cannot be maintained.

Because there is no industry-wide accepted value for "significant" distortion, the full peak response is specified in this data sheet and is measured using the circuit of Figure 1. The initial setup involves the use of a sinusoidal input to determine the maximum peak-to-peak output of the device (the amplitude of the sinusoidal wave is increased until clipping occurs). The sinusoidal wave is then replaced with a square wave of the same amplitude. The frequency is then increased until the maximum peak-to-peak output can no longer be maintained (Figure 5). A square wave is used to allow a more accurate determination of the point at which the maximum peak-to-peak output is reached.

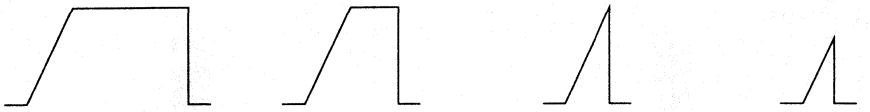


FIGURE 5. FULL-POWER-RESPONSE OUTPUT SIGNAL

test time

Inadequate test time is a frequent problem, especially when testing CMOS devices in a high-volume, short-test-time environment. Internal capacitances are inherently higher in CMOS than in bipolar and BiFET devices, and require longer test times than their bipolar and BiFET counterparts. The problem becomes more pronounced with reduced supply levels and lower temperatures.

TYPICAL CHARACTERISTICS

DISTRIBUTION OF TLC27L4
INPUT OFFSET VOLTAGE

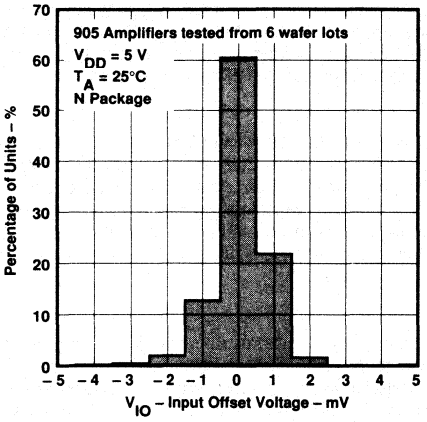


FIGURE 6

DISTRIBUTION OF TLC27L4
INPUT OFFSET VOLTAGE

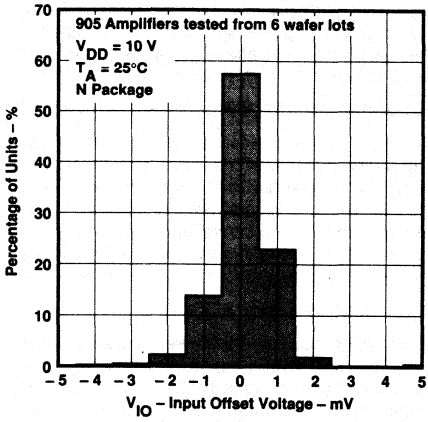


FIGURE 7

DISTRIBUTION OF TLC27L4 AND TLC27L9
INPUT OFFSET VOLTAGE
TEMPERATURE COEFFICIENT

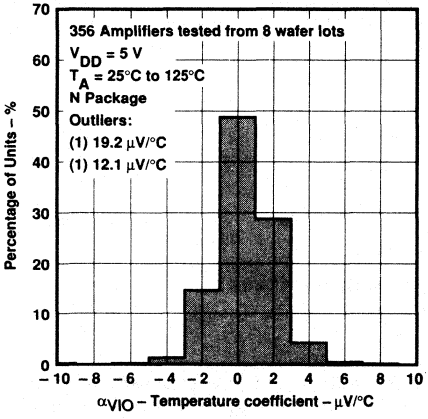


FIGURE 8

DISTRIBUTION OF TLC27L4 AND TLC27L9
INPUT OFFSET VOLTAGE
TEMPERATURE COEFFICIENT

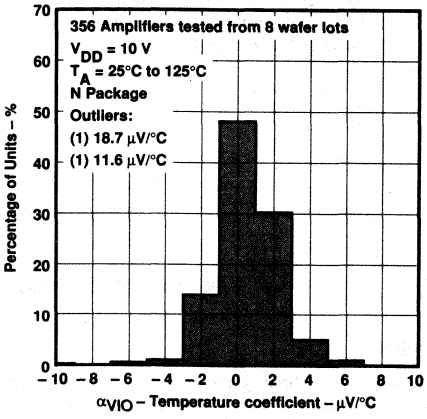


FIGURE 9

TYPICAL CHARACTERISTICS

HIGH-LEVEL OUTPUT VOLTAGE
vs
HIGH-LEVEL OUTPUT CURRENT

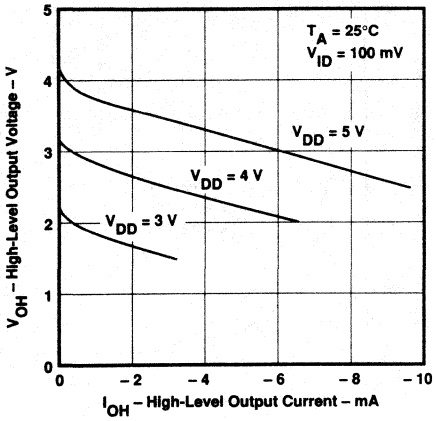


FIGURE 10

HIGH-LEVEL OUTPUT VOLTAGE
vs
HIGH-LEVEL OUTPUT CURRENT

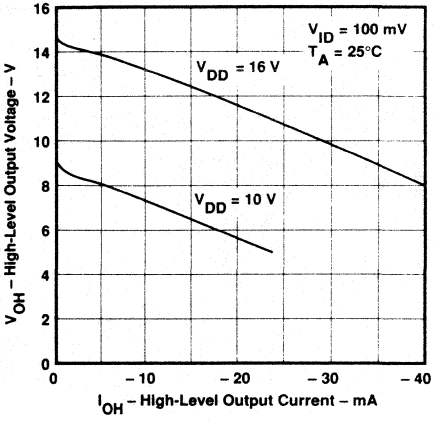


FIGURE 11

HIGH-LEVEL OUTPUT VOLTAGE
vs
SUPPLY VOLTAGE

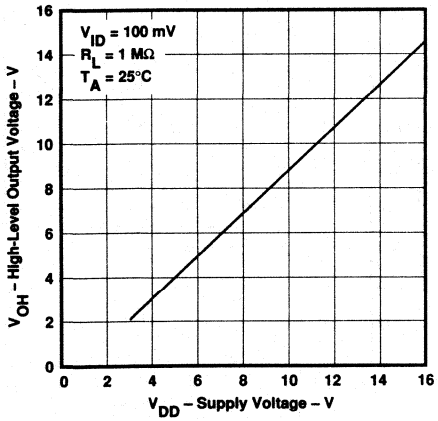


FIGURE 12

HIGH-LEVEL OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE

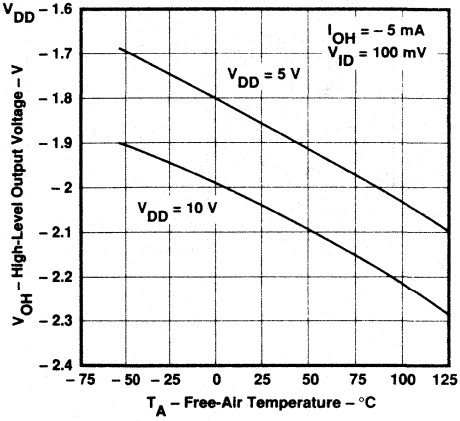


FIGURE 13

TYPICAL CHARACTERISTICS

LOW-LEVEL OUTPUT VOLTAGE
vs
COMMON-MODE INPUT VOLTAGE

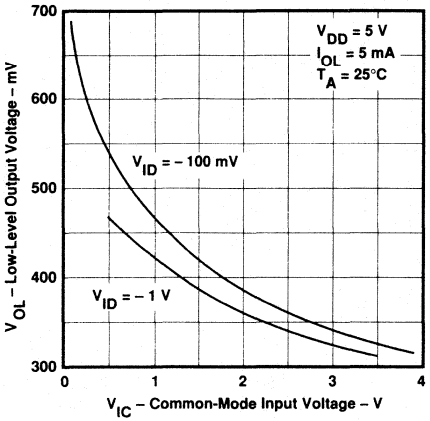


FIGURE 14

LOW-LEVEL OUTPUT VOLTAGE
vs
COMMON-MODE INPUT VOLTAGE

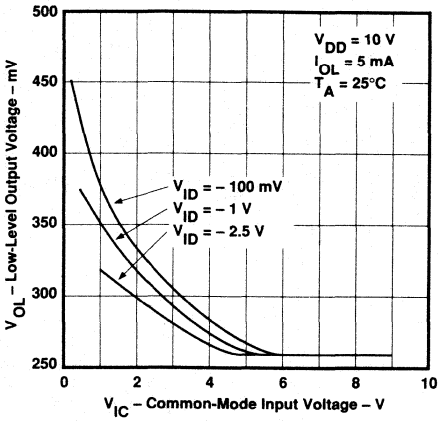


FIGURE 15

LOW-LEVEL OUTPUT VOLTAGE
vs
DIFFERENTIAL INPUT VOLTAGE

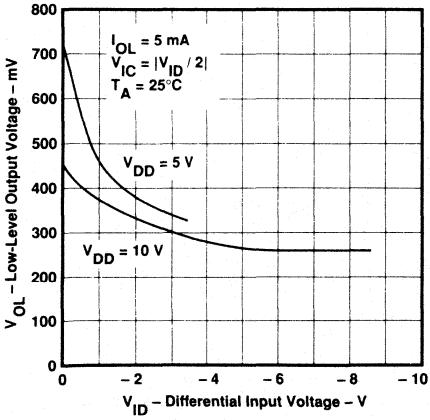


FIGURE 16

LOW-LEVEL OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE

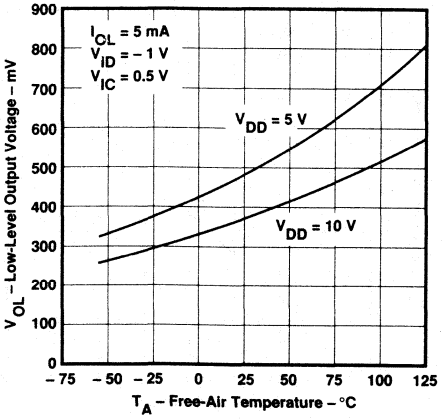


FIGURE 17

TYPICAL CHARACTERISTICS

LOW-LEVEL OUTPUT VOLTAGE
vs
LOW-LEVEL OUTPUT CURRENT

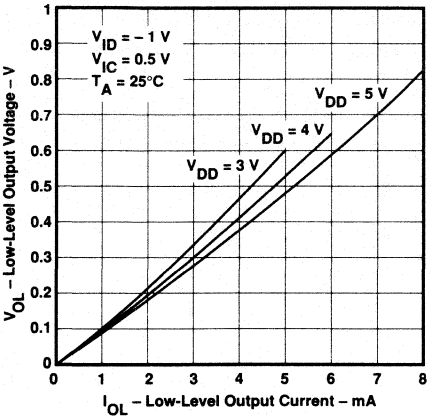


FIGURE 18

LOW-LEVEL OUTPUT VOLTAGE
vs
LOW-LEVEL OUTPUT CURRENT

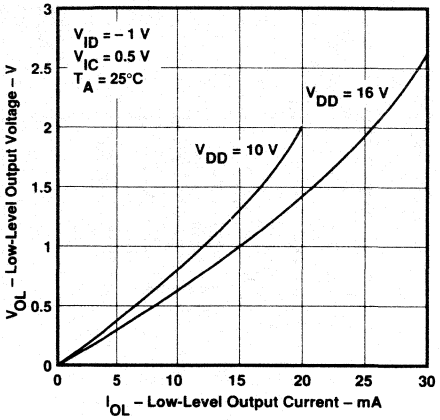


FIGURE 19

LARGE-SIGNAL
DIFFERENTIAL VOLTAGE AMPLIFICATION
vs
SUPPLY VOLTAGE

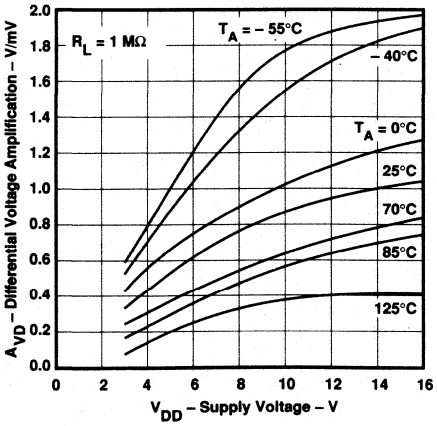


FIGURE 20

LARGE-SIGNAL
DIFFERENTIAL VOLTAGE AMPLIFICATION
vs
FREE-AIR TEMPERATURE

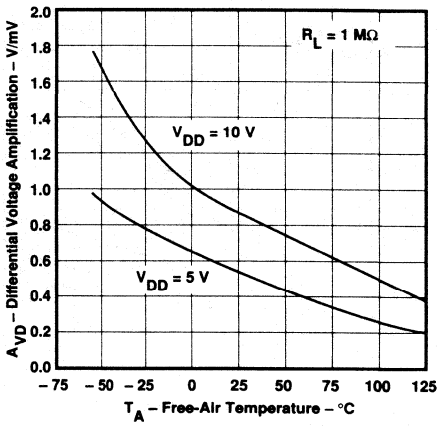


FIGURE 21

TYPICAL CHARACTERISTICS

INPUT BIAS CURRENT AND INPUT OFFSET CURRENT
vs
FREE-AIR TEMPERATURE

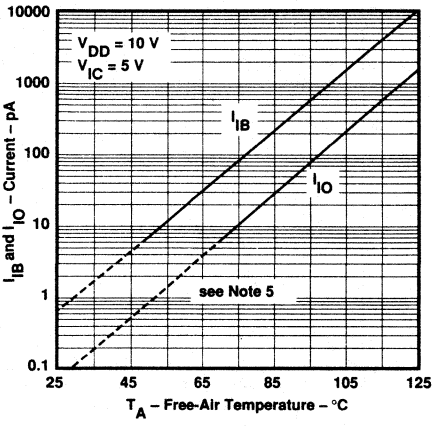


FIGURE 22

MAXIMUM INPUT VOLTAGE
vs
SUPPLY VOLTAGE

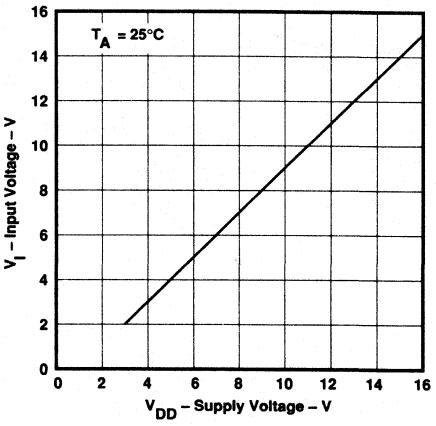


FIGURE 23

SUPPLY CURRENT
vs
SUPPLY VOLTAGE

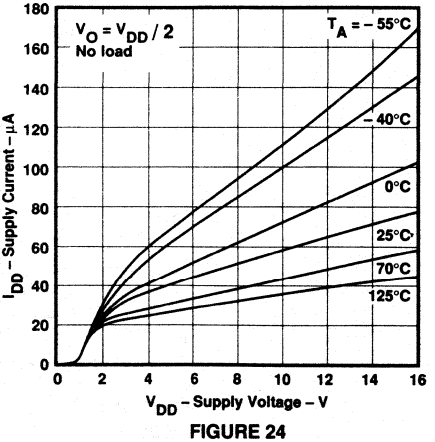


FIGURE 24

SUPPLY CURRENT
vs
FREE-AIR TEMPERATURE

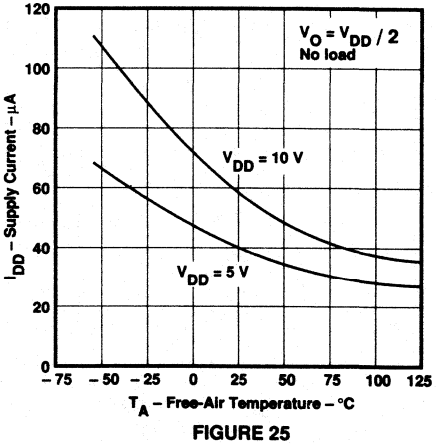


FIGURE 25

NOTE 5: The typical values of input bias current and input offset current below 5 pA were determined mathematically.

TYPICAL CHARACTERISTICS

SLEW RATE
vs
SUPPLY VOLTAGE

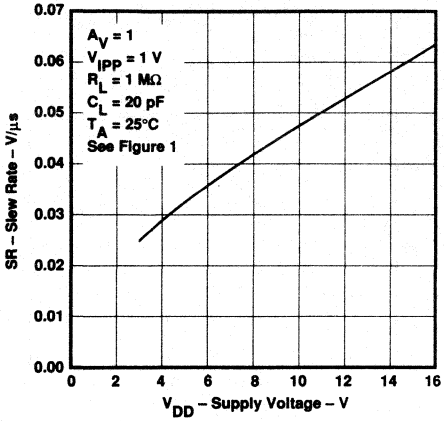


FIGURE 26

SLEW RATE
vs
FREE-AIR TEMPERATURE

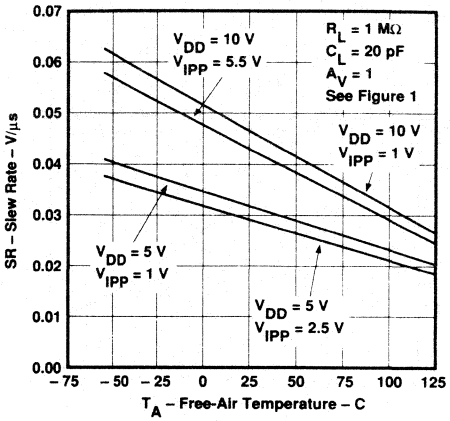


FIGURE 27

NORMALIZED SLEW RATE
vs
FREE-AIR TEMPERATURE

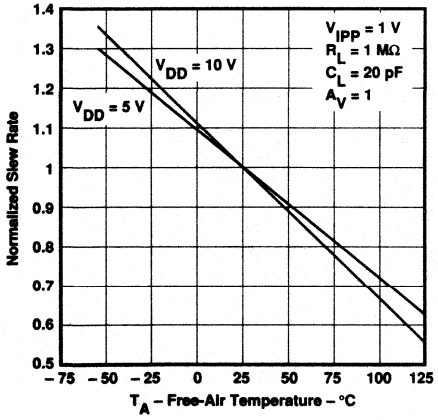


FIGURE 28

MAXIMUM PEAK-TO-PEAK OUTPUT VOLTAGE
vs
FREQUENCY

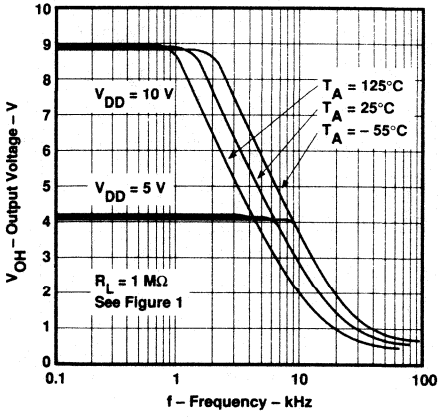


FIGURE 29

TYPICAL CHARACTERISTICS

UNITY-GAIN BANDWIDTH
vs
FREE-AIR TEMPERATURE

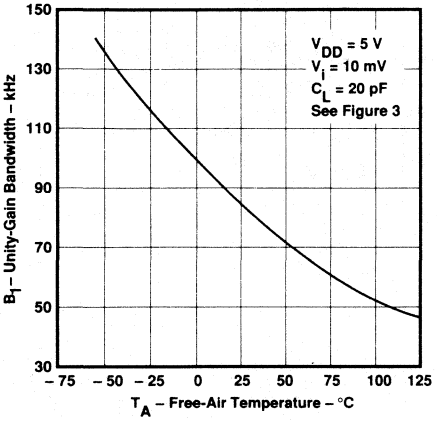


FIGURE 30

UNITY-GAIN BANDWIDTH
vs
SUPPLY VOLTAGE

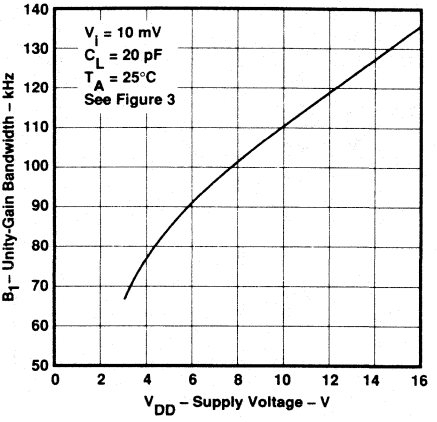


FIGURE 31

LARGE-SIGNAL DIFFERENTIAL VOLTAGE
AMPLIFICATION AND PHASE SHIFT
vs
FREQUENCY

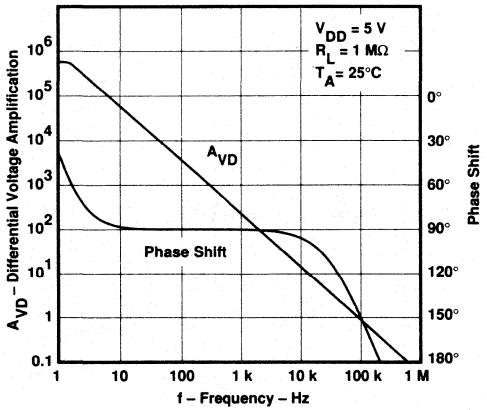


FIGURE 32

LARGE-SIGNAL DIFFERENTIAL VOLTAGE
AMPLIFICATION AND PHASE SHIFT
vs
FREQUENCY

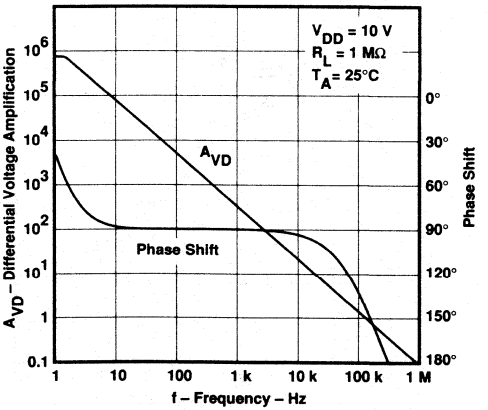


FIGURE 33

TYPICAL CHARACTERISTICS

PHASE MARGIN
vs
SUPPLY VOLTAGE

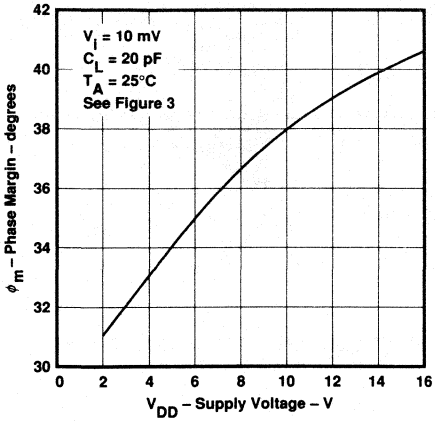


FIGURE 34

PHASE MARGIN
vs
FREE-AIR TEMPERATURE

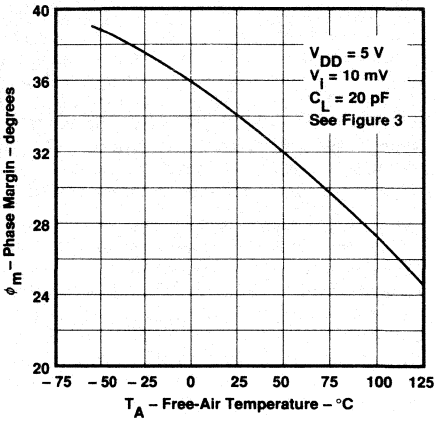


FIGURE 35

PHASE MARGIN
vs
CAPACITIVE LOAD

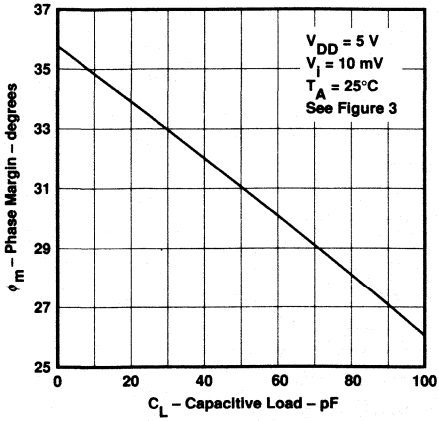


FIGURE 36

EQUIVALENT INPUT NOISE VOLTAGE
vs
FREQUENCY

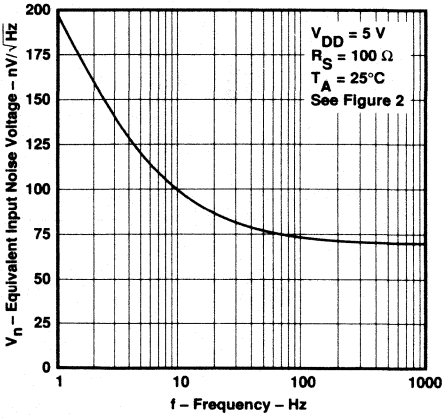


FIGURE 37

TYPICAL APPLICATION DATA

single-supply operation

While the TLC27L4 and TLC27L9 will perform well using dual power supplies (also called balanced or split supplies), the design is optimized for single-supply operation. This includes an input common mode voltage range that encompasses ground as well as an output voltage range that pulls down to ground. The supply voltage range extends down to 3 V (C- suffix types), thus allowing operation with supply levels commonly available for TTL and HCMOS; however, for maximum dynamic range, 16-V single-supply operation is recommended.

Many single-supply applications require that a voltage be applied to one input to establish a reference level that is above ground. A resistive voltage divider is usually sufficient to establish this reference level (see Figure 38). The low input bias current consumption of the TLC27L4 and TLC27L9 permits the use of very large resistive values to implement the voltage divider, thus minimizing power consumption.

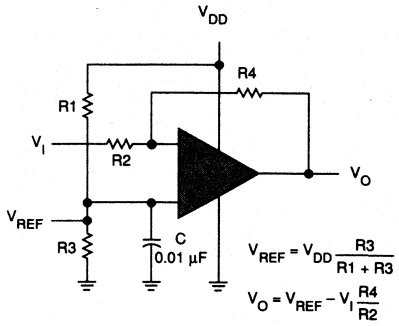
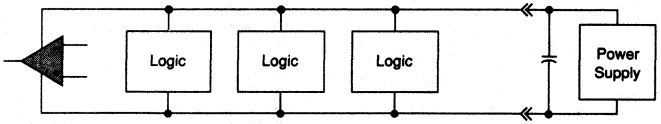


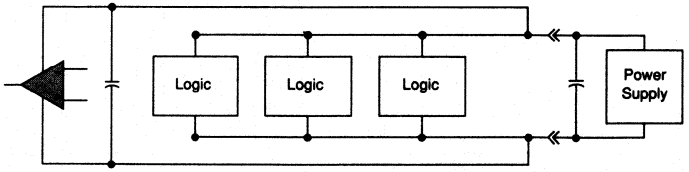
FIGURE 38. INVERTING AMPLIFIER WITH VOLTAGE REFERENCE

The TLC27L4 and TLC27L9 work well in conjunction with digital logic; however, when powering both linear devices and digital logic from the same power supply, the following precautions are recommended:

1. Power the linear devices from separate bypassed supply lines (see Figure 39); otherwise the linear device supply rails can fluctuate due to voltage drops caused by high switching currents in the digital logic.
2. Use proper bypass techniques to reduce the probability of noise-induced errors. Single capacitive decoupling is often adequate; however, RC decoupling may be necessary in high-frequency applications.



(a) Common Supply Rails



(b) Separate Bypassed Supply Rails (preferred)

FIGURE 39. COMMON VERSUS SEPARATE SUPPLY RAILS

TYPICAL APPLICATION DATA

input characteristics

The TLC27L4 and TLC27L9 are specified with a minimum and a maximum input voltage that, if exceeded at either input, could cause the device to malfunction. Exceeding this specified range is a common problem, especially in single-supply operation. Note that the lower range limit includes the negative rail, while the upper range limit is specified at V_{DD} – 1 V at T_A = 25°C and at V_{DD} – 1.5 V at all other temperatures.

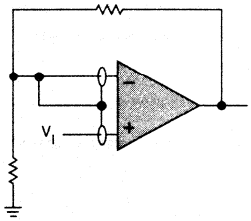
The use of the polysilicon-gate process and the careful input circuit design gives the TLC27L4 and TLC27L9 very good input offset voltage drift characteristics relative to conventional metal-gate processes. Offset voltage drift in CMOS devices is highly influenced by threshold voltage shifts caused by polarization of the phosphorus dopant implanted in the oxide. Placing the phosphorus dopant in a conductor (such as a polysilicon gate) alleviates the polarization problem, thus reducing threshold voltage shifts by more than an order of magnitude. The offset voltage drift with time has been calculated to be typically 0.1 μV/month, including the first month of operation.

Because of the extremely high input impedance and resulting low bias current requirements, the TLC27L4 and TLC27L9 are well suited for low-level signal processing; however, leakage currents on printed circuit boards and sockets can easily exceed bias current requirements and cause a degradation in device performance. It is good practice to include guard rings around inputs (similar to those of Figure 4 in the PARAMETER MEASUREMENT INFORMATION section). These guards should be driven from a low-impedance source at the same voltage level as the common-mode input (see Figure 40).

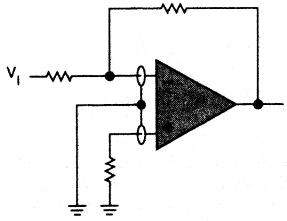
The inputs of any unused amplifiers should be tied to ground to avoid possible oscillation.

noise performance

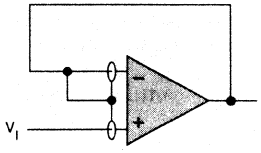
The noise specifications in op amp circuits are greatly dependent on the current in the first-stage differential amplifier. The low input bias current requirements of the TLC27L4 and TLC27L9 result in a very low noise current, which is insignificant in most applications. This feature makes the devices especially favorable over bipolar devices when using values of circuit impedance greater than 50 kΩ, since bipolar devices exhibit greater noise currents.



(a) Noninverting Amplifier



(b) Inverting Amplifier



(c) Unity Gain Amplifier

Figure 40. GUARD RING SCHEMES

TYPICAL APPLICATION DATA

output characteristics

The output stage of the TLC27L4 and TLC27L9 is designed to sink and source relatively high amounts of current (see typical characteristics). If the output is subjected to a short-circuit condition, this high current capability can cause device damage under certain conditions. Output current capability increases with supply voltage.

All operating characteristics of the TLC27L4 and TLC27L9 were measured using a 20-pF load. The devices will drive higher capacitive loads; however, as output load capacitance increases, the resulting response pole occurs at lower frequencies, thereby causing ringing, peaking, or even oscillation (see Figure 41). In many cases, adding some compensation in the form of a series resistor in the feedback loop will alleviate the problem.

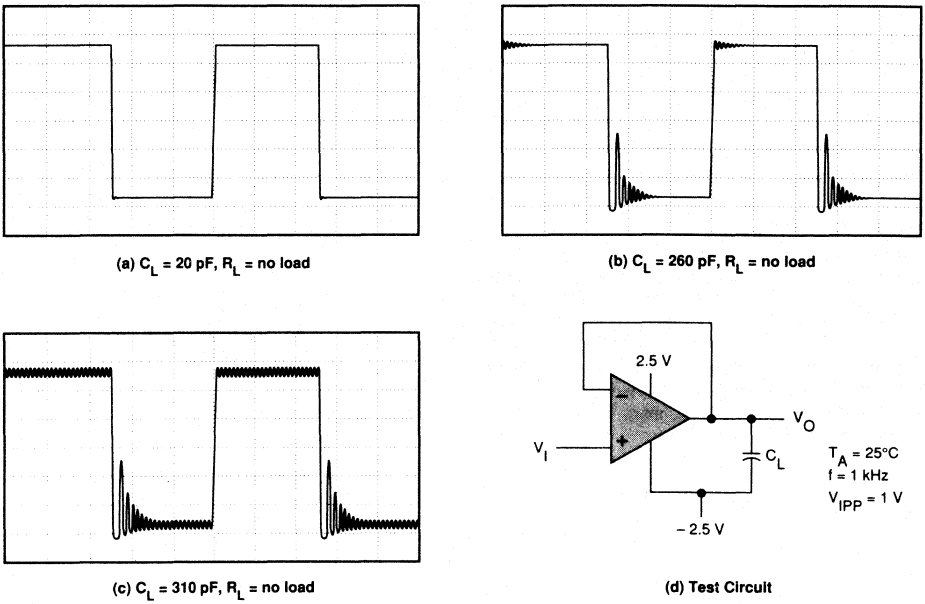


FIGURE 41. EFFECT OF CAPACITIVE LOADS AND TEST CIRCUIT

Although the TLC27L4 and TLC27L9 possess excellent high-level output voltage and current capability, methods are available for boosting this capability, if needed. The simplest method involves the use of a pullup resistor connected from the output to the positive supply rail. There are two disadvantages to the use of this circuit. First, the NMOS pull-down transistor, N4 (see Figure 42) must sink a comparatively large amount of current. In this circuit, N4 behaves like a linear resistor with an on resistance between approximately 60 Ω and 180 Ω, depending on how hard the op amp input is driven. With very low values of R6, a voltage offset from 0 V at the output will occur. Secondly, pullup resistor R6 acts as a drain load to N4 and the gain of the op amp is reduced at output voltage levels where N5 is not supplying the output current.

TYPICAL APPLICATION DATA

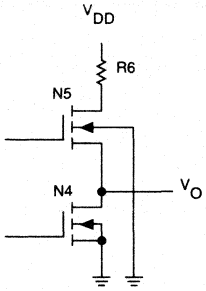


FIGURE 42. TLC27L4 / TLC27L9 OUTPUT STAGE

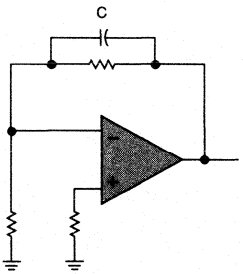


FIGURE 43. COMPENSATION FOR INPUT CAPACITANCE

feedback

Op amp circuits nearly always employ feedback, and since feedback is the first prerequisite for oscillation, a little caution is appropriate. Most oscillation problems result from driving capacitive loads (discussed previously) and ignoring stray input capacitance. A small-value capacitor connected in parallel with the feedback resistor is an effective remedy (see Figure 43). The value of this capacitor is optimized empirically.

electrostatic discharge protection

The TLC27L4 and TLC27L9 incorporate an internal electrostatic discharge (ESD) protection circuit that will prevent functional failures at voltages at or below 2000 V as tested under MIL-STD-883C, Method 3015.2. Care should be exercised, however, when handling these devices as exposure to ESD may result in the degradation of the device parametric performance. The protect circuit also causes the input bias currents to be temperature dependent and have the characteristics of a reverse-biased diode.

latchup

Because CMOS devices are susceptible to latchup due to their inherent parasitic thyristors, the TLC27L4 and TLC27L9 inputs and outputs were designed to withstand −100-mA surge currents without sustaining latchup; however, techniques should be used to reduce the chance of latchup whenever possible. Internal protection diodes should not by design be forward biased. Applied input and output voltage should not exceed the supply voltage by more than 300 mV. Care should be exercised when using capacitive coupling on pulse generators. Supply transients should be shunted by the use of decoupling capacitors (0.1 μF typical) located across the supply rails as close to the device as possible.

The current path established if latchup occurs is usually between the positive supply rail and ground and can be triggered by surges on the supply lines and / or voltages on either the output or inputs that exceed the supply voltage. Once latchup occurs, the current flow is limited only by the impedance of the power supply and the forward resistance of the parasitic thyristor and usually results in the destruction of the device. The chance of latchup occuring increases with increasing temperature and supply voltages.

TYPICAL APPLICATION DATA

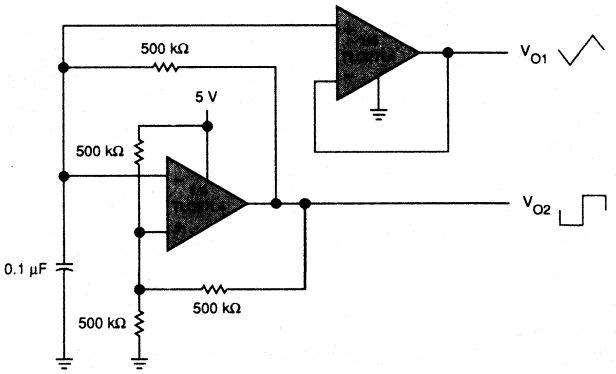
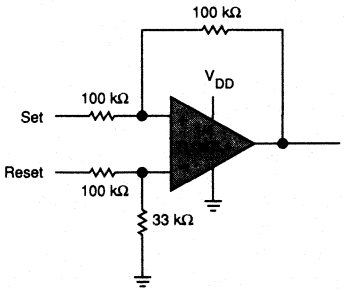


FIGURE 44. MULTIVIBRATOR

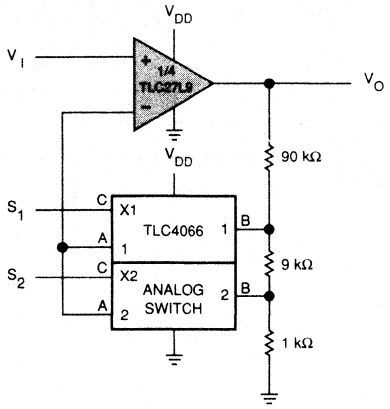


NOTES: V_{DD} = 5 V to 16V

FIGURE 45. SET / RESET FLIP-FLOP

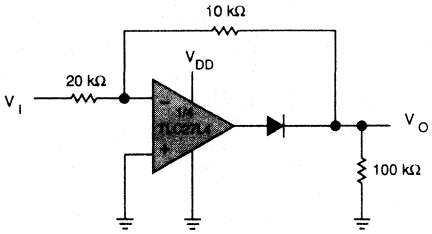
TYPICAL APPLICATION DATA

Select:	S_1	S_2
A_V	10	100



NOTES: V_{DD} = 5 V to 12V

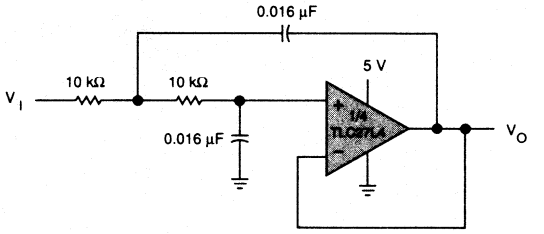
FIGURE 46. AMPLIFIER WITH DIGITAL GAIN SELECTION



NOTES: V_{DD} = 5 V to 16V

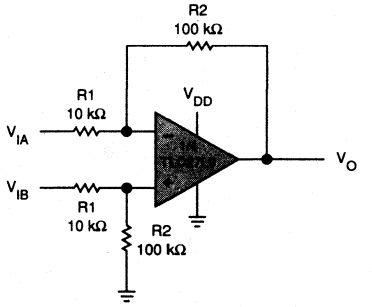
FIGURE 47. FULL WAVE RECTIFIER

TYPICAL APPLICATION DATA



NOTE: Normalized to F_C = 1 kHz and R_L = 10 kΩ

FIGURE 48. TWO-POLE LOW-PASS BUTTERWORTH FILTER



NOTES: V_{DD} = 5 V to 16 V

$$V_O = \frac{R2}{R1}(V_{IB} - V_{IA})$$

FIGURE 49. DIFFERENCE AMPLIFIER

General Information 1

Operational Amplifiers 2

Voltage Comparators 3

Timers 4

Analog to Digital Converters 5

Digital to Analog Converters 6

Analog Switches 7

Switched Capacitor Filters 8

Packaging Information 9

COMPARATORS

	INPUT OFFSET VOLTAGE (mV)	INPUT OFFSET CURRENT (pA)	INPUT BIAS CURRENT AT 25°C (pA)	RESPONSE TIME (μS)	SUPPLY CURRENT (uA)	SUPPLY VOLTAGE RANGE (V)		OUTPUT TYPE	PAGE No
						Min	Max		
Dual									
TLC372	12.0	1	5	0.65	750	3	16	Open Drain	3-23
TLC393	10	1	5	2.10	50	3	16	Open Drain	3-31
TLC3702	10	1	5	2.30	50	3	16	Totem Pole*	3-47
Quad									
TLC374	12.0	1	5	0.65	1000	3	16	Open Drain	3-27
TLC339	10	1	5	2.10	100	3	16	Open Drain	3-7
TLC3704	10	1	5	2.30	100	3	16	Totem Pole*	3-61

**Totem Pole Outputs are HCMOS and TTL compatible*

Input Offset Voltage (V_{IO})

The d-c voltage that must be applied between the input terminals to force the quiescent d-c output voltage to the specified level.

Average Temperature Coefficient of Input Offset Voltage (α_{VIO})

The ratio of the change in input offset voltage to the change in free-air temperature. This is an average value for the specified temperature range.

$$\alpha_{VIO} = \left[\frac{(V_{IO} \text{ @ } T_{A(1)}) - (V_{IO} \text{ @ } T_{A(2)})}{T_{A(1)} - T_{A(2)}}\right] \text{ where } T_{A(1)} \text{ and } T_{A(2)} \text{ are the specified temperature extremes.}$$

Input Offset Current (I_{IO})

The difference between the currents into the two input terminals with the output at the specified level.

Average Temperature Coefficient of Input Offset Current (α_{IIO})

The ratio of the change in input offset current to the change in free-air temperature. This is an average value for the specified temperature range.

$$\alpha_{IIO} = \left[\frac{(I_{IO} \text{ @ } T_{A(1)}) - (I_{IO} \text{ @ } T_{A(2)})}{T_{A(1)} - T_{A(2)}}\right] \text{ where } T_{A(1)} \text{ and } T_{A(2)} \text{ are the specified temperature extremes.}$$

Input Bias Current (I_{IB})

The average of the currents into the two input terminals with the output at the specified level.

High-Level Strobe Curent ($I_{IH(S)}$)

The current flowing into or out of * the strobe at a high-level voltage.

Low-Level Strobe Current ($I_{IL(S)}$)

The current flowing out of * the strobe at a low-level voltage.

High-Level Strobe Voltage ($V_{IH(S)}$)

For a device having an active-low strobe, a voltage within the range that is guaranteed not to interfere with the operation of the compactor.

Low-Level Strobe Voltage ($V_{IL(S)}$)

For a device having an active-low strobe, a voltage within the range that is guaranteed to force the output high or low, as specified, independently of the differential inputs.

Input Voltage Range (V_I)

The range of voltage that if exceeded at either input terminal will cause the comparator to cease functioning properly.

Common-Mode Input Voltage (V_{IC})

The average of the two input voltages.

*Current out of a terminal is given as a negative value.

Common-Mode Input Voltage Range (V_{ICR})

The range of common-mode input voltage that if exceeded will cause the comparator to cease functioning properly.

Differential Input Voltage (V_{ID})

The voltage at the noninverting input with respect to the inverting input.

Differential Input Voltage Range (V_{ID})

The range of voltage between the two input terminals that if exceeded will cause the comparator to cease functioning properly.

Differential Voltage Amplification (A_{VD})

The ratio of the change in output to the change in differential input voltage producing it with the common-mode input voltage held constant.

High-Level Output Voltage (V_{OH})

The voltage at an output with input conditions applied that according to the product specification will establish a high level at the output.

Low-Level Output Voltage (V_{OL})

The voltage at an output with input conditions applied that according to the product specification will establish a low level at the output.

High-Level Output Current, (I_{OH})

The current into * an output with input conditions applied that according to the product specification will establish a high level at the output.

Low-Level Output Current, (I_{OL})

The current into * an output with input conditions applied that according to the product specification will establish a low level at the output.

Output Resistance (r_o)

The resistance between the output terminal and ground.

Common-Mode Rejection Ratio (k_{CMR}, CMRR)

The ratio of differential voltage amplification to common-mode voltage amplification.
NOTE: This is measured by determining the ratio of a change in input common-mode voltage to the resulting change in input offset voltage.

Supply Current (I_{CC+}, I_{CC-})

The current into * the V_{CC+} or V_{CC-} terminal of an integrated circuit.

Total Power Dissipation (P_D)

The total d-c power supplied to the device less any power delivered from the device to a load.
NOTE: At no load: $P_D = V_{CC+} \bullet I_{CC+} + V_{CC-} \bullet I_{CC-}$.

*Current out of a terminal is given as a negative value.

Response Time

The interval between the application of an input step function and the instant at when the output crosses the logic threshold voltage.

NOTE: The input step drives the comparator from some initial condition sufficient to saturate the output (or in the case of high-to-low-level response time, to turn the output off) to an input level just barely in excess of that required to bring the output back to the logic threshold voltage. This excess is referred to as the voltage overdrive.

Strobe Release Time

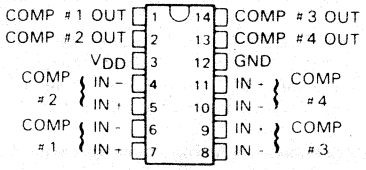
The time required for the output to rise to the logic threshold voltage after the strobe terminal has been driven from its active logic level to its inactive logic level.

TLC339M, TLC339I, TLC339C
QUADRUPLE MICROPOWER LinCMOS™ COMPARATORS

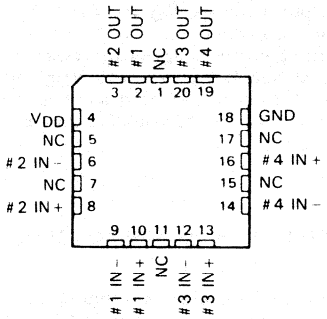
DECEMBER 1986

- Very Low Power ... 200 μW Typ at 5 V
- Fast Response Time ... 2.5 μs Typ with 5 mV Overdrive
- Single Supply Operation:
  TLC339M ... 4 V to 16 V
  TLC339I ... 3 V to 16 V
  TLC339C ... 3 V to 16 V
- High Input Impedance ... $10^{12}\Omega$ Typ
- Input Offset Voltage Change at Worst Case Input Condition Typically 0.23 μV/Month Including the First 30 Days
- On-Chip ESD Protection

TLC339M ... J PACKAGE
TLC339I ... D, J, OR N PACKAGE
TLC339C ... D, J, OR N PACKAGE
(TOP VIEW)



TLC339M ... FK PACKAGE
(TOP VIEW)

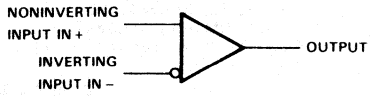


NC – No internal connection

description

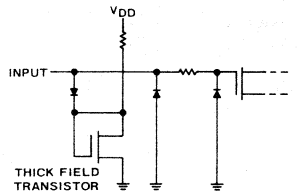
The TLC339 consists of four independent differential-voltage comparators designed to operate from a single supply. It is functionally similar to the LM339 but uses 1/20th the power for similar response times. The open-drain MOS output stage will interface to a variety of loads and supplies, as well as "wired" logic functions. For a similar device with a push-pull output configuration, see the TLC3704 data sheet.

symbol (each comparator)

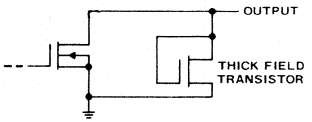


schematics of inputs and outputs

EQUIVALENT OF EACH INPUT



TYPICAL OF ALL OUTPUTS



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TEXAS INSTRUMENTS

TLC339M, TLC339I, TLC339C
QUADRUPLE MICROPOWER LinCMOS™ COMPARATORS

Texas Instruments LinCMOS process offers superior analog performance to standard CMOS processes. Along with the standard CMOS advantages of low power without sacrificing speed, high input impedance, and low bias currents, the LinCMOS process offers extremely stable input offset voltages, even with differential input stresses of several volts. This characteristic makes it possible to build reliable CMOS comparators.

The TLC339M is characterized for operation over the full military temperature range of -55°C to 125°C. The TLC339I is characterized for operation over the extended industrial temperature range of -40°C to 85°C. The TLC339C is characterized for operation over the commercial temperature range of 0°C to 70°C.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{DD} (see Note 1)	-0.3 V to 18 V
Differential input voltage (see Note 2)	±18 V
Input voltage, V_I	-0.3 V to V_{DD}
Output voltage, V_O	-0.3 V to V_{DD}
Input current, I_I	±5 mA
Output current, I_O (each output)	20 mA
Total supply current into V_{DD} terminal	40 mA
Total current out of ground terminal	60 mA
Continuous total dissipation at (or below) 25°C free-air temperature (see Note 3):	
D package	950 mW
FK or J package (alloy mount)	1375 mW
J package (glass mount)	1025 mW
N package	875 mW
Operating free-air temperature range: TLC339M	-55°C to 125°C
TLC339I	-40°C to 85°C
TLC339C	0°C to 70°C
Storage temperature range	-65°C to 150°C
Lead temperature 1.6 mm (1/16 inch) from case for 60 seconds: FK or J package	300°C
Lead temperature 1.6 mm (1/16 inch) from case for 10 seconds: D or N package	260°C

NOTES: 1. All voltage values, except differential voltages, are with respect to network ground.
2. Differential voltages are at the noninverting input with respect to the inverting input.
3. For operation above 25°C free-air temperature, refer to the Dissipation Derating Table. For the TLC339M in the J package, use the alloy mount derating factor; for the TLC339I and TLC339C in the J package, use the glass mount derating factor.

DISSIPATION DERATING TABLE

PACKAGE	POWER RATING	DERATING FACTOR	ABOVE T_A
D	950 mW	7.6 mW/°C	25°C
FK	1375 mW	11 mW/°C	25°C
J (alloy mount)	1375 mW	11 mW/°C	25°C
J (glass mount)	1025 mW	6.6 mW/°C	25°C
N	875 mW	7 mW/°C	25°C

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage, V_{DD}	4	5	16	V
Common-mode input voltage, V_{IC}	-0.2		V_{DD}-1.5	V
Low-level output current, I_{OL}		8	20	mA
Operating free-air temperature, T_A	-55		125	°C

electrical characteristics at specified operating free-air temperature, V_{DD} = 5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS †		MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage	V_{IC} = V_{ICR}min, V_{DD} = 5 V to 10 V, See Note 4	25°C		1.4	5	mV
			Full range			10	
I_{IO}	Input offset current	V_{IC} = 2.5 V	25°C		1		pA
			125°C			15	nA
I_{IB}	Input bias current	V_{IC} = 2.5 V	25°C		5		pA
			125°C			30	nA
V_{ICR}	Common-mode input voltage range		25°C	0 to V_{DD}-1			V
			Full range	0 to V_{DD}-1.5			
CMRR	Common-mode rejection ratio	V_{IC} = V_{ICR}min	25°C		84		dB
			125°C		84		
			-55°C		84		
k_{SVR}	Supply voltage rejection ratio	V_{DD} = 5 V to 10 V	25°C		85		dB
			125°C		84		
			-55°C		84		
V_{OL}	Low-level output voltage	V_{ID} = -1 V, I_{OL} = 6 mA	25°C		300	400	mV
			125°C			800	
I_{OH}	High-level output current	V_{ID} = 1 V, V_O = 5 V	25°C		0.8	40	nA
			125°C			1	µA
I_{DD}	Supply current (four comparators)	No load, Outputs low	25°C		44	80	µA
			Full range			175	

† All characteristics are measured with zero common-mode voltage unless otherwise noted. Full range is -55°C to 125°C for the TLC339M.

NOTE 4: The offset voltage limits given are the maximum values required to drive the output up to 4.5 V or down to 0.3 V.

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage, V_{DD}	3	5	16	V
Common-mode input voltage, V_{IC}	-0.2		V_{DD}-1.5	V
Low-level output current, I_{OL}		8	20	mA
Operating free-air temperature, T_A	-40		85	°C

electrical characteristics at specified operating free-air temperature, V_{DD} = 5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS †		MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage	$V_{IC} = V_{ICR}$min, V_{DD} = 5 V to 10 V, See Note 4	25°C		1.4	5	mV
			Full range			7	
I_{IO}	Input offset current	V_{IC} = 2.5 V	25°C		1		pA
			85°C			1	nA
I_{IB}	Input bias current	V_{IC} = 2.5 V	25°C		5		pA
			85°C			2	nA
V_{ICR}	Common-mode input voltage range		25°C	0 to V_{DD}-1			V
			Full range	0 to V_{DD}-1.5			
CMRR	Common-mode rejection ratio	$V_{IC} = V_{ICR}$min	25°C		84		dB
			85°C		84		
			-40°C		84		
k_{SVR}	Supply voltage rejection ratio	V_{DD} = 5 V to 10 V	25°C		85		dB
			85°C		85		
			-40°C		84		
V_{OL}	Low-level output voltage	V_{ID} = -1 V, I_{OL} = 6 mA	25°C		300	400	mV
			85°C			700	
I_{OH}	High-level output current	V_{ID} = 1 V, V_O = 5 V	25°C		0.8	40	nA
			85°C			1	μA
I_{DD}	Supply current (four comparators)	No load	25°C		44	80	μA
			Full range			125	

† All characteristics are measured with zero common-mode voltage unless otherwise noted. Full range is -40°C to 85°C for the TLC339I.

NOTE 4: The offset voltage limits given are the maximum values required to drive the output up to 4.5 V or down to 0.3 V.

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage, V_{DD}	3	5	16	V
Common-mode input voltage, V_{IC}	-0.2		V_{DD}-1.5	V
Low-level output current, I_{OL}		8	20	mA
Operating free-air temperature, T_A	0		70	°C

electrical characteristics at specified operating free-air temperature, V_{DD} = 5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS †		MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage	V_{IC} = V_{ICR}min, V_{DD} = 5 V to 10 V, See Note 4	25°C		1.4	5	mV
			Full range			6.5	
I_{IO}	Input offset current	V_{IC} = 2.5 V	25°C		1		pA
			70°C			0.3	nA
I_{IB}	Input bias current	V_{IC} = 2.5 V	25°C		5		pA
			70°C			0.6	nA
V_{ICR}	Common-mode input voltage range		25°C	0 to V_{DD}-1			V
			Full range	0 to V_{DD}-1.5			
CMRR	Common-mode rejection ratio	V_{IC} = V_{ICR}min	25°C		84		dB
			70°C		84		
			0°C		84		
k_{SVR}	Supply voltage rejection ratio	V_{DD} = 5 V to 10 V	25°C		85		dB
			70°C		85		
			0°C		85		
V_{OL}	Low-level output voltage	V_{ID} = -1 V, I_{OL} = 6 mA	25°C		300	400	mV
			70°C			650	
I_{OH}	High-level output current	V_{ID} = 1 V, V_O = 5 V	25°C		0.8	40	nA
			70°C			1	µA
I_{DD}	Supply current (four comparators)	No load, Outputs low	25°C		44	80	µA
			Full range			100	

† All characteristics are measured with zero common-mode voltage unless otherwise noted. Full range is 0°C to 70°C for the TLC339C.

NOTE 4: The offset voltage limits given are the maximum values required to drive the output up to 4.5 V or down to 0.3 V.

switching charactistics, V_{DD} = 5 V, T_A = 25°C (see Figure 3)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_{PHL}	Response time, high-to-low-level output	f = 10 kHz, C_L = 15 pF	Overdrive = 2 mV		3.6		µs
			Overdrive = 5 mV		2.1		
			Overdrive = 10 mV		1.3		
			Overdrive = 20 mV		0.85		
			Overdrive = 40 mV		0.55		
		V_I = 1.4 V step at IN+ pin			0.10		
t_{PLH}	Response time, low-to-high-level output	f = 10 kHz, C_L = 15 pF	Overdrive = 2 mV		4.5		µs
			Overdrive = 5 mV		2.5		
			Overdrive = 10 mV		1.7		
			Overdrive = 20 mV		1.2		
			Overdrive = 40 mV		1.0		
		V_I = 1.4 V step at IN+ pin			1.1		
t_{THL}	Transition time, high-to-low-level output	f = 10 kHz, C_L = 15 pF	Overdrive = 50 mV		20		ns

PARAMETER MEASUREMENT INFORMATION

The TLC339 contains a digital output stage which, if held in the linear region of the transfer curve, can cause damage to the device. Conventional operational amplifier/comparator testing incorporates the use of a servo-loop which is designed to force the device output to a level within this linear region. Since the servo-loop method of testing cannot be used, we offer the following alternatives for measuring parameters such as input offset voltage, common-mode rejection, etc.

To verify that the input offset voltage falls within the limits specified, the limit value is applied to the input as shown in Figure 1a. With the noninverting input positive with respect to the inverting input, the output should be high. With the input polarity reversed, the output should be low.

A similar test can be made to verify the input offset voltage at the common-mode extremes. The supply voltages can be slewed as shown in Figure 1b for the V_{ICR} test, rather than changing the input voltages, to provide greater accuracy.

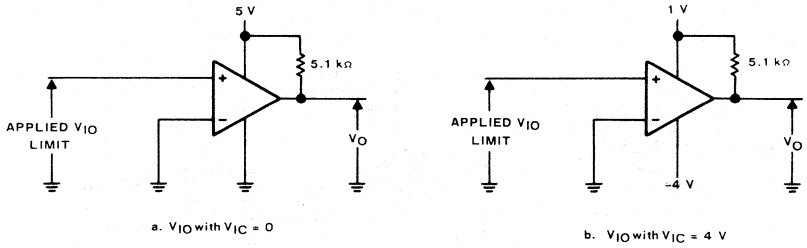


FIGURE 1. METHOD FOR VERIFYING THAT INPUT OFFSET VOLTAGE IS WITHIN SPECIFIED LIMITS

A close approximation of the input offset voltage can be obtained by using a binary search method to vary the differential input voltage while monitoring the output state. When the applied input voltage differential is equal, but opposite in polarity, to the input offset voltage, the output will change states.

PARAMETER MEASUREMENT INFORMATION

Figure 2 illustrates a practical circuit for direct d.c. measurement of input offset voltage that does not bias the comparator into the linear region. The circuit consists of a switching mode servo loop in which IC1a generates a triangular waveform of approximately 20 mV amplitude. IC1b acts as a buffer, with C2 and R4 removing any residual d.c. offset. The signal is then applied to the inverting input of the comparator under test, while the noninverting input is driven by the output of the integrator formed by IC1c through the voltage divider formed by R9 and R10. The loop reaches a stable operating point when the output of the comparator under test has a duty cycle of exactly 50%, which can only occur when the incoming triangle wave is "sliced" symmetrically or when the voltage at the noninverting input exactly equals the input offset voltage.

Voltage divider R9 and R10 provides a step-up of the input offset voltage by a factor of 100 to make measurement easier. The values of R5, R8, R9, and R10 can significantly influence the accuracy of the reading; therefore, it is suggested that their tolerance level be one percent or lower.

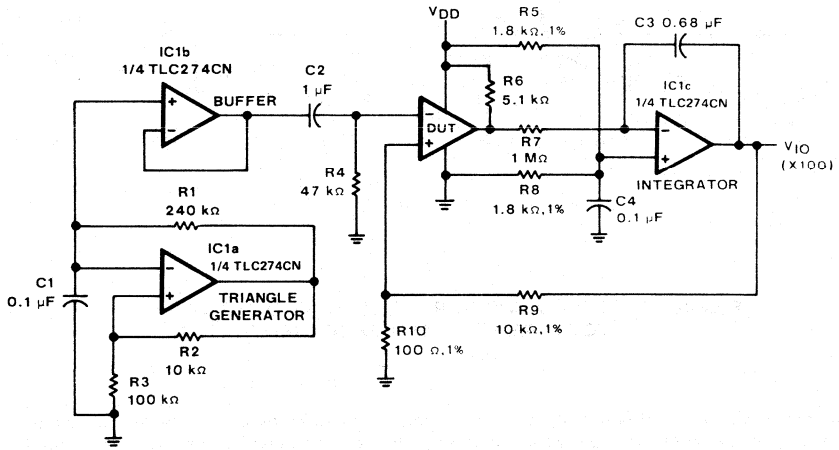
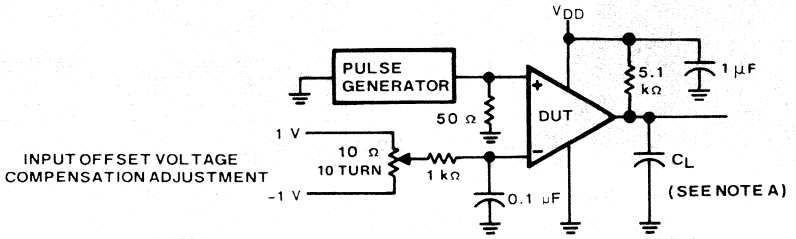


FIGURE 2. CIRCUIT FOR INPUT OFFSET VOLTAGE MEASUREMENT

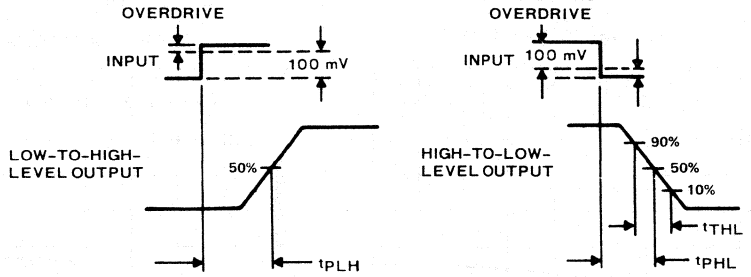
Measuring the extremely low values of input current requires isolation from all other sources of leakage current and compensation for the leakage of the test socket and board. With a good picoammeter, the socket and board leakage can be measured with no device in the socket. Subsequently, this open socket leakage value can be subtracted from the measurement obtained with a device in the socket to obtain the actual input current of the device.

PARAMETER MEASUREMENT INFORMATION

Response time is defined as the interval between the application of an input step function and the instant when the output reaches 50% of its maximum value. Response time, low-to-high-level output is measured from the leading edge of the input pulse, while response time, high-to-low-level output, is measured from the trailing edge of the input pulse. Response time measurement at low input signal levels can be greatly affected by the input offset voltage. The offset voltage should be balanced by the adjustment at the inverting input (as shown in Figure 3) so that the circuit is just at the transition point. Then a low signal, for example 105 mV or 5 mV overdrive, will cause the output to change state.



TEST CIRCUIT



VOLTAGE WAVEFORMS

NOTE A: C_L includes probe and jig capacitance.

FIGURE 3. RESPONSE, RISE, AND FALL TIMES
CIRCUIT AND VOLTAGE WAVEFORMS

TYPICAL CHARACTERISTICS

DISTRIBUTION OF INPUT OFFSET VOLTAGE

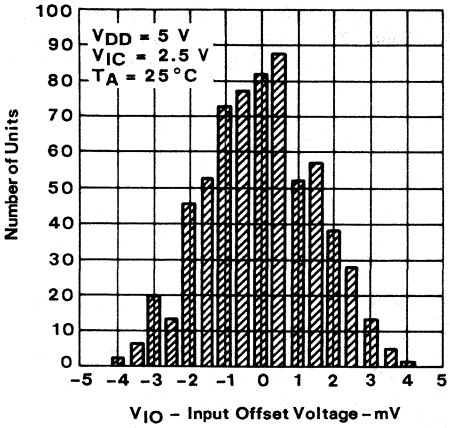


FIGURE 4

INPUT BIAS CURRENT vs FREE-AIR TEMPERATURE

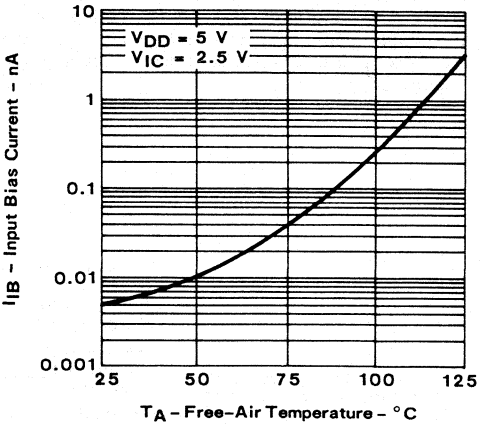


FIGURE 5

COMMON-MODE REJECTION RATIO vs FREE-AIR TEMPERATURE

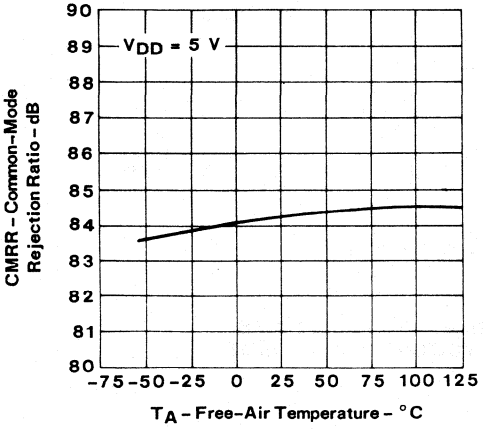


FIGURE 6

SUPPLY VOLTAGE REJECTION RATIO vs FREE-AIR TEMPERATURE

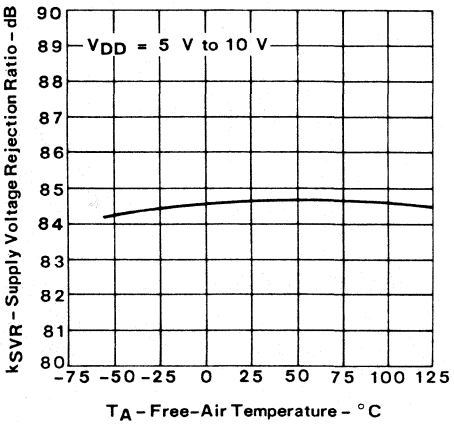


FIGURE 7

TYPICAL CHARACTERISTICS

HIGH-LEVEL OUTPUT CURRENT
vs
HIGH-LEVEL OUTPUT VOLTAGE

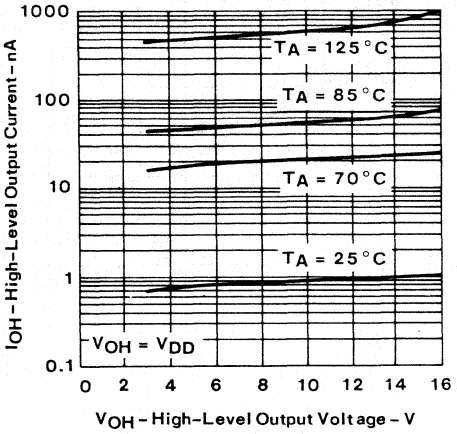


FIGURE 8

HIGH-LEVEL OUTPUT CURRENT
vs
FREE-AIR TEMPERATURE

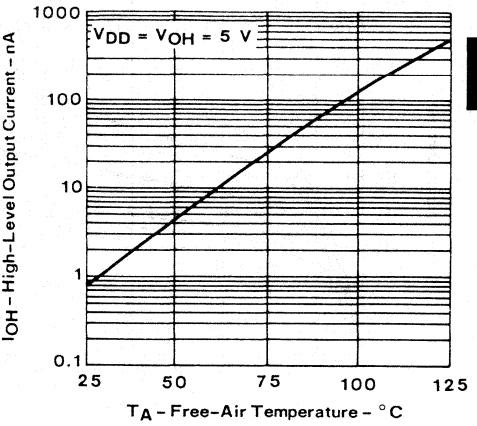


FIGURE 9

LOW-LEVEL OUTPUT VOLTAGE
vs
LOW-LEVEL OUTPUT CURRENT

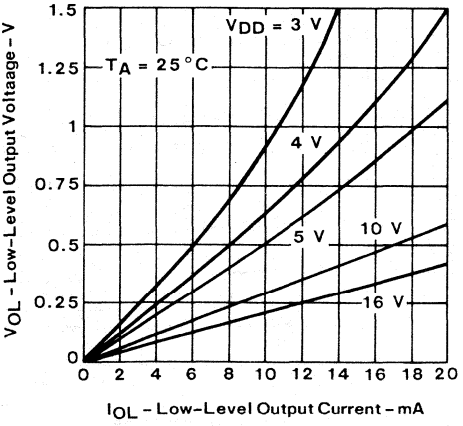


FIGURE 10

LOW-LEVEL OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE

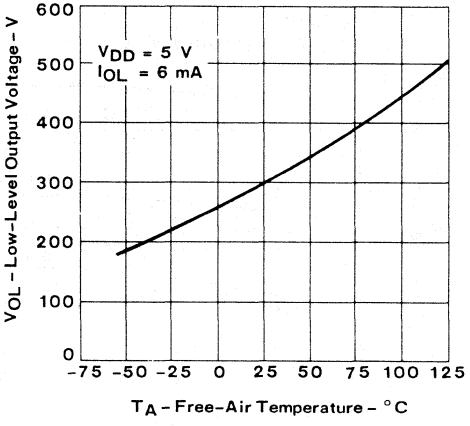


FIGURE 11

TYPICAL CHARACTERISTICS

SUPPLY CURRENT
vs
SUPPLY VOLTAGE

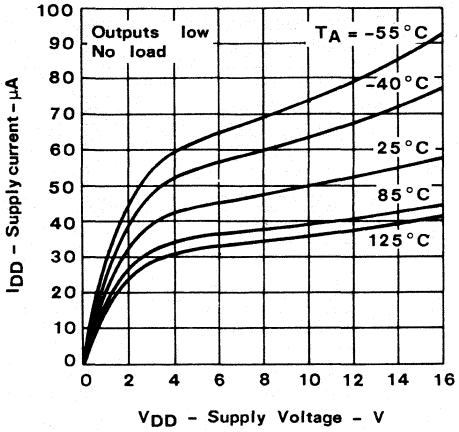


FIGURE 12

SUPPLY CURRENT
vs
FREE-AIR TEMPERATURE

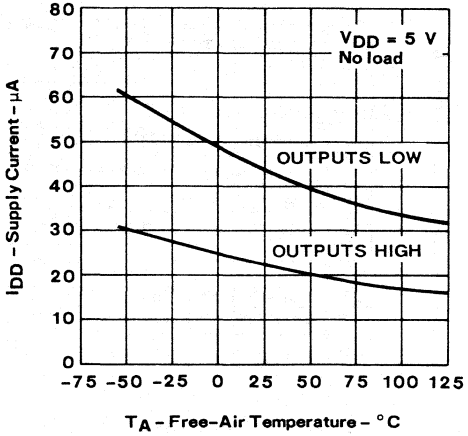


FIGURE 13

LOW-TO-HIGH-LEVEL
OUTPUT RESPONSE TIME
vs
SUPPLY VOLTAGE

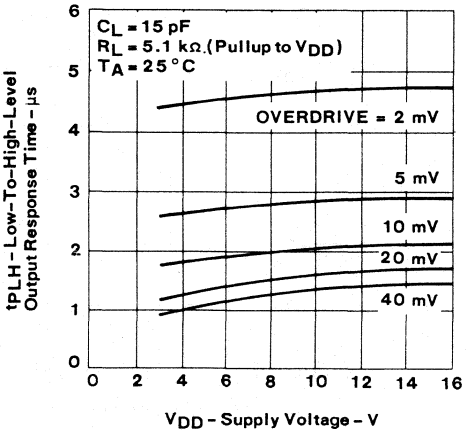


FIGURE 14

HIGH-TO-LOW-LEVEL
OUTPUT RESPONSE TIME
vs
SUPPLY VOLTAGE

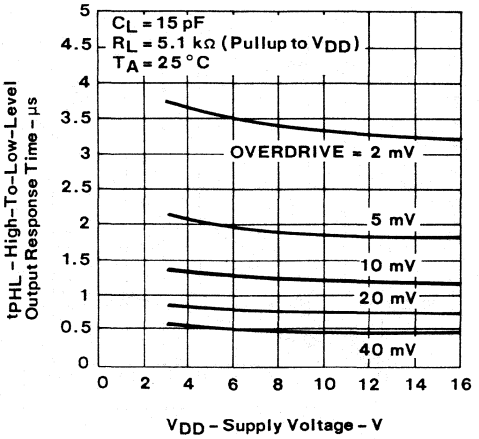


FIGURE 15

TYPICAL CHARACTERISTICS

LOW-TO-HIGH-LEVEL OUTPUT RESPONSE
FOR VARIOUS OVERDRIVE VOLTAGES

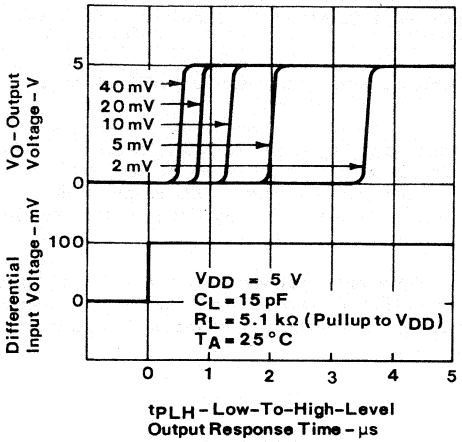


FIGURE 16

OUTPUT FALL TIME
vs
SUPPLY VOLTAGE

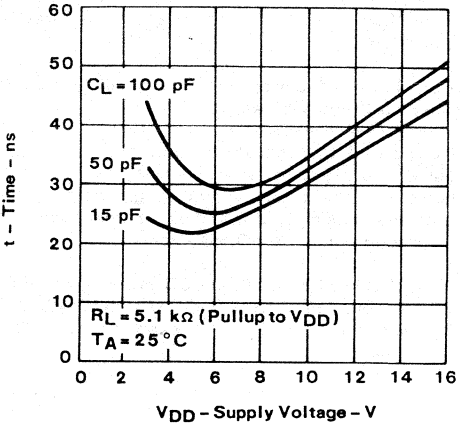


FIGURE 17

HIGH-TO-LOW-LEVEL OUTPUT RESPONSE
FOR VARIOUS OVERDRIVE VOLTAGES

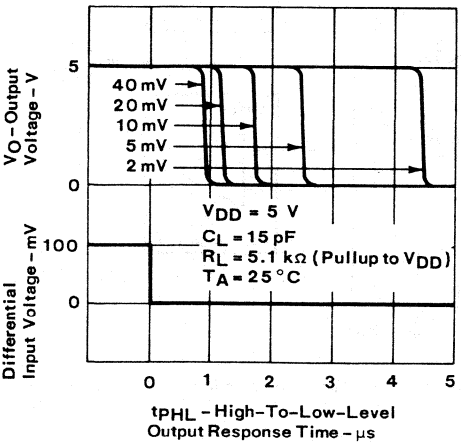


FIGURE 18

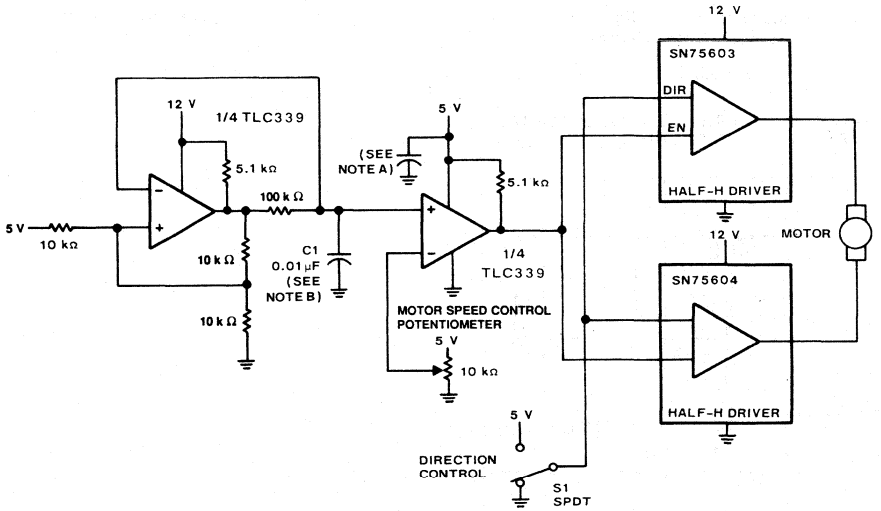
TYPICAL APPLICATION DATA

The inputs should always remain within the supply rails in order to avoid forward biasing the diodes in the electrostatic discharge (ESD) protection structure. If either input exceeds this range, the device will not be damaged as long as the input current is limited to less than 5 milliamperes. To maintain the expected output state, the inputs must remain within the common-mode range. For example, at 25°C with V_{DD} = 5 V, both inputs must remain between -0.2 V and 4 V to assure proper device operation.

To assure reliable operation, the supply should be decoupled with a capacitor (0.1 μF) positioned as close to the device as possible.

Be careful to note the output and supply current limitations since the TLC339 does not provide current protection. For example, each output can source or sink a maximum of 20 milliamperes; however, the total current to ground can only be an absolute maximum of 60 milliamperes. This prohibits sinking 20 milliamperes from each of the four outputs simultaneously since the total current to ground would be 80 milliamperes.

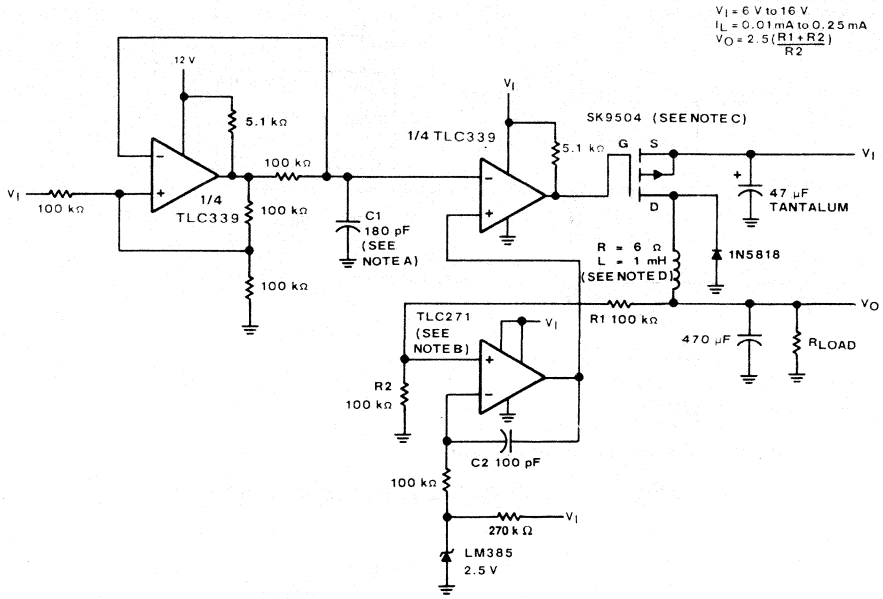
The TLC339 has internal ESD protection circuits that will prevent functional failures at voltages up to 2000 volts as tested under MIL-STD-883C, Method 3015.2; however, care should be exercised in handling these devices as exposure to ESD may result in the degradation of the device parametric performance.



NOTES: A. The recommended minimum capacitance is 10 μF to eliminate common ground switching noise.
B. Select C1 for change in oscillator frequency.

FIGURE 19. PULSE-WIDTH-MODULATED MOTOR SPEED CONTROLLER

TYPICAL APPLICATION DATA



NOTES: A. Select C1 for a change in oscillator frequency.

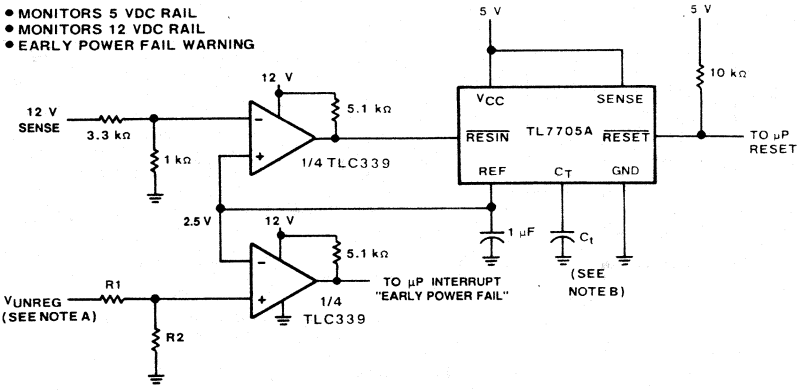
B. TLC271 – Tie pin 8 to pin 7 for low bias operation.

C. SK9504 – V_{DS} = 40 V
I_{DS} = 1 A

D. To achieve microampere current drive, the inductance of the circuit must be increased.

FIGURE 20. MICROPOWER SWITCHING REGULATOR

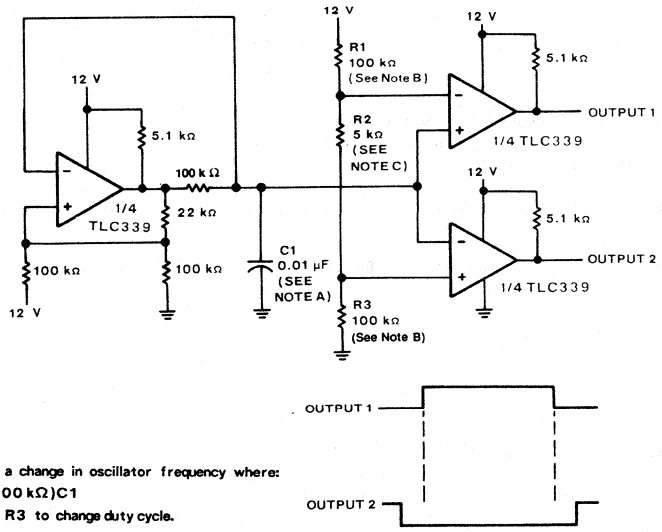
TYPICAL APPLICATION DATA



NOTES: A. $V_{UNREG} = 2.5\left(\frac{R1+R2}{R2}\right)$

B. The value of C_t determines the time delay of reset.

FIGURE 21. ENHANCED SUPPLY SUPERVISOR



NOTES: A. Select C1 for a change in oscillator frequency where:
$1/f = 1.85(100\,k\Omega)C1$

B. Select R1 and R3 to change duty cycle.

C. Select R2 to change deadtime.

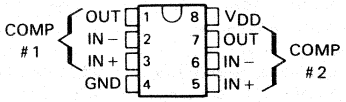
FIGURE 22. TWO-PHASE NONOVERLAPPING CLOCK GENERATOR

TLC372M, TLC372I, TLC372C
LinCMOS™ DUAL DIFFERENTIAL COMPARATORS

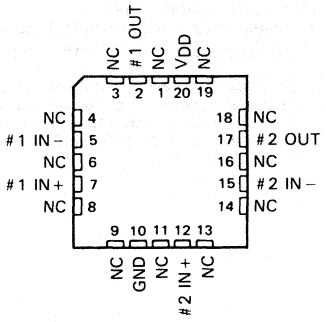
D2821, NOVEMBER 1983—REVISED OCTOBER 1985

- Single or Dual-Supply Operation
- Wide Range of Supply Voltages . . . 2 V to 18 V
- Very Low Supply Current Drain 0.3 mA Typ at 5 V
- Fast Response Time . . . 200 ns Typ for TTL-Level Input Step
- Built-In ESD Protection
- High Input Impedance . . . 10^{12} Typ
- Extremely Low Input Bias Current 5 pA Typ
- Ultrastable Low Input Offset Voltage
- Input Offset Voltage Change at Worst-Case Input Conditions Typically 0.23 μV/Month, Including the First 30 Days
- Common-Mode Input Voltage Range Includes Ground
- Outputs Compatible with TTL, MOS, and CMOS
- Pin-Compatible with LM393

TLC372M . . . JG
TLC372I, TLC372C . . . D, JG, OR P
DUAL-IN-LINE PACKAGE
(TOP VIEW)



TLC372M . . . FK PACKAGE
(TOP VIEW)

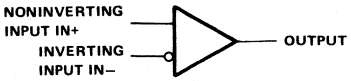


NC—No internal connection

description

This device is fabricated using LinCMOS™ technology and consists of two independent voltage comparators each designed to operate from a single power supply. Operation from dual supplies is also possible so long as the difference between the two supplies is 2 to 18 volts. Each device features extremely high input impedance (typically greater than 10^{12} ohms) allowing direct interfacing with high-impedance sources. The outputs are n-channel open-drain configurations, and can be connected to achieve positive-logic wired-AND relationships.

symbol (each comparator)



The TLC372 has internal electrostatic discharge (ESD) protection circuits and has been classified with a 2000-volt ESD rating tested under MIL-STD-883B, Method 3015.1. However, care should be exercised in handling this device as exposure to ESD may result in a degradation of the device parametric performance.

The TLC372M is characterized for operation over the full military temperature range of −55°C to 125°C. The TLC372I is characterized for operation from −40°C to 85°C. The TLC372C is characterized for operation from 0°C to 70°C.

LinCMOS is a trademark of Texas Instruments.

TEXAS INSTRUMENTS

absolute maximum ratings over free-air operating temperature range (unless otherwise noted)

Supply voltage, V_{DD} (see Note 1)	18 V
Differential input voltage, V_{ID} (see Note 2)	±18 V
Input voltage, V_I	V_{DD}
Output voltage, V_O	18 V
Output current, I_O	20 mA
Duration of output short-circuit to ground (see Note 3)	unlimited
Continuous total dissipation at (or below) 70°C free-air temperature (see Note 4)	300 mW
Free-air temperature range: TLC372M	−55°C to 125°C
TLC372I	−40°C to 85°C
TLC372C	0°C to 70°C
Storage temperature range	−65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds, FK or JG package	300°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds, D or P package	260°C

NOTES: 1. All voltage values except differential voltages are with respect to network ground.
2. Differential voltages are at the noninverting input terminal with respect to the inverting input terminal.
3. Short circuits from outputs to V_{DD} can cause excessive heating and eventual device destruction.
4. For operation of the TLC372M in the JG package above 114°C free-air temperature, derate linearly at the rate of 8.4 mW/°C to 210 mW at 125°C.

electrical characteristics at specified free-air temperature, V_{DD} = 5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS†			TLC372M			TLC372I			TLC372C			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	$V_{IC} = V_{ICR}$ min, See Note 5		25°C		2	10		2	10		2	10	mV
				Full range			12			13			12	
I_{IO}	Input offset current			25°C		1			1			1		pA
				MAX T_A			10			1			0.3	nA
I_{IB}	Input bias current			25°C		5			5			5		pA
				MAX T_A			20			2			0.6	nA
V_{ICR}	Common-mode input voltage range			25°C	0 to $V_{DD}-1.75$			0 to $V_{DD}-1.75$			0 to $V_{DD}-1.75$			V
				Full range	0 to $V_{DD}-2$			0 to $V_{DD}-2$			0 to $V_{DD}-2$			
I_{OH}	High-level output current	V_{ID} = 1 V	V_{OH} = 5 V	25°C		0.1			0.1			0.1		nA
			V_{OH} = 15 V	Full range			1			1			1	μA
V_{OL}	Low-level output voltage	V_{ID} = −1 V,	I_{OL} = 4 mA	25°C		150	400		150	400		150	400	mV
				Full range			700			700			700	
I_{OL}	Low-level output current	V_{ID} = −1 V,	V_{OL} = 1.5 V	25°C	6	16		6	16		6	16		mA
I_{DD}	Supply current (four comparators)	V_{ID} = 1 V,	No load	25°C		0.3	0.75		0.3	0.75		0.3	0.75	mA

† All characteristics are measured with zero common-mode input voltage unless otherwise noted. Full range is −55°C to 125°C for TLC372M, 0°C to 70°C for TLC372C, and −40°C to 85°C for TLC372I. IMPORTANT: See Parameter Measurement Information.

NOTE 5: The offset voltage limits given are the maximum values required to drive the output above 4 V or below 400 mV with a 10-kΩ resistor between the output and V_{DD}. They can be verified by applying the limit value to the input and checking for the appropriate output state.

switching characteristics, V_{DD} = 5 V, T_A = 25°C

PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
Response time	R_L connected to 5 V through 5.1 kΩ, C_L = 15 pF‡, See Note 6	100-mV input step with 5-mV overdrive		650		ns
		TTL-level input step		200		

‡ C_L includes probe and jig capacitance.

NOTE 6: The response time specified is the interval between the input step function and the instant when the output crosses 1.4 V.

PARAMETER MEASUREMENT INFORMATION

The TLC372 must not be tested in the servo-loop configuration often used for operational amplifiers. This device has a digital output stage. Attempts to force the device into the linear region of the transfer curve can cause damage. Test equipment should operate in accordance with the following recommendations and no attempt should be made to measure the gain of the device on an automatic tester.

To verify that V_{IO} falls within the limits specified, the limit value is applied to the input as shown in Figure 1. With IN+ positive with respect to IN−, the output should be high. With the input polarity reversed, the output should be low. If it is desired to measure the actual value of V_{IO}, a binary search method can be used to vary the input potential and check the output states until a good approximation of the critical point is obtained.

Measuring the extremely low values of input current requires isolation from all other sources of leakage current or, at least, compensating for the leakage of test socket and board. With a good picoammeter, the socket and board leakage can be measured with no device in the socket and the reading subtracted from that obtained with a device in the socket.

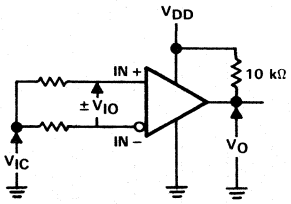


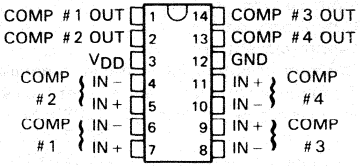
FIGURE 1. TEST CIRCUIT

TLC374M, TLC374I, TLC374C
LinCMOS™ QUADRUPLE DIFFERENTIAL COMPARATOR

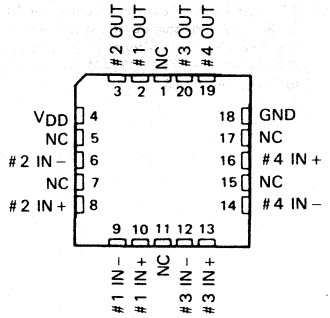
D2783, NOVEMBER 1983—REVISED OCTOBER 1985

- Single or Dual-Supply Operation
- Wide Range of Supply Voltages . . . 2 V to 18 V
- Very Low Supply Current Drain 0.6 mA Typ at 5 V
- Fast Response Time . . . 200 ns Typ for TTL-Level Input Step
- Built-In ESD Protection
- High Input Impedance . . . 10^{12} Typ
- Extremely Low Input Bias Current 5 pA Typ
- Ultrastable Low Input Offset Voltage
- Input Offset Voltage Change at Worst-Case Input Conditions Typically 0.23 μV/Month, Including the First 30 Days
- Common-Mode Input Voltage Range Includes Ground
- Outputs Compatible with TTL, MOS, and CMOS
- Pin-Compatible with LM339

TLC374M . . . J
TLC374I, TLC374C . . . D, J, OR N
DUAL-IN-LINE PACKAGE
(TOP VIEW)



TLC374M . . . FK PACKAGE
(TOP VIEW)

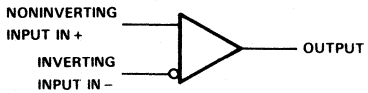


NC—No internal connection

description

This device is fabricated using LinCMOS™ technology and consists of four independent voltage comparators designed to operate from a single power supply. Operation from dual supplies is also possible so long as the difference between the two supplies is 2 to 18 volts. Each device features extremely high input impedance (typically greater than 10^{12} ohms) allowing direct interfacing with high-impedance sources. The outputs are n-channel open-drain configurations, and can be connected to achieve positive-logic wired-AND relationships.

symbol (each comparator)



The TLC374 has internal electrostatic discharge (ESD) protection circuits and has been classified with a 2000-volt ESD rating tested under MIL-STD-883B, Method 3015.1. However, care should be exercised in handling this device as exposure to ESD may result in a degradation of the device parametric performance.

The TLC374M is characterized for operation over the full military temperature range of −55°C to 125°C. The TLC374I is characterized for operation from −40°C to 85°C. The TLC374C is characterized for operation from 0°C to 70°C.

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absolute maximum ratings over free-air operating temperature range (unless otherwise noted)

Supply voltage, V_{DD} (see Note 1)	18 V
Differential input voltage, V_{ID} (see Note 2)	±18 V
Input voltage, V_I	V_{DD}
Output voltage, V_O	18 V
Output current, I_O	20 mA
Duration of output short-circuit to ground (see Note 3)	unlimited
Continuous total dissipation at (or below) 70°C free-air temperature (see Note 4)	300 mW
Free-air temperature range: TLC374M	−55°C to 125°C
TLC374I	−40°C to 85°C
TLC374C	0°C to 70°C
Storage temperature range	−65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds, J or FK package	300°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds, D or N package	260°C

NOTES: 1. All voltage values except differential voltages are with respect to network ground.
2. Differential voltages are at the noninverting input terminal with respect to the inverting input terminal.
3. Short circuits from outputs to V_{DD} can cause excessive heating and eventual device destruction.
4. For operation of the TLC374M in the J package above 114°C free-air temperature, derate linearly at the rate of 8.4 mW/°C to 210 mW at 125°C.

electrical characteristics at specified free-air temperature, V_{DD} = 5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS†			TLC374M			TLC374I			TLC374C			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	$V_{IC} = V_{ICR}$ min, See Note 5		25°C		2	10		2	10		2	10	mV
				Full range			12			13			12	
I_{IO}	Input offset current			25°C		1			1			1		pA
				MAX T_A			10			1			0.3	nA
I_{IB}	Input bias current			25°C		5			5			5		pA
				MAX T_A			20			2			0.6	nA
V_{ICR}	Common-mode input voltage range			25°C	0 to $V_{DD}-1.75$			0 to $V_{DD}-1.75$			0 to $V_{DD}-1.75$			V
				Full range	0 to $V_{DD}-2$			0 to $V_{DD}-2$			0 to $V_{DD}-2$			
I_{OH}	High-level output current	V_{ID} = 1 V	V_{OH} = 5 V	25°C		0.1			0.1			0.1		nA
			V_{OH} = 15 V	Full range			1			1			1	μA
V_{OL}	Low-level output voltage	V_{ID} = −1 V,	I_{OL} = 4 mA	25°C		150	400		150	400		150	400	mV
				Full range			700			700			700	
I_{OL}	Low-level output current	V_{ID} = −1 V,	V_{OL} = 1.5 V	25°C	6	16		6	16		6	16		mA
I_{DD}	Supply current (four comparators)	V_{ID} = 1 V,	No load	25°C		0.6	1		0.6	1		0.6	1	mA

† All characteristics are measured with zero common-mode input voltage unless otherwise noted. Full range is −55°C to 125°C for TLC374M, −40°C to 85°C for TLC374I, and 0°C to 70°C for TLC374C. IMPORTANT: See Parameter Measurement Information.

NOTE 5: The offset voltage limits given are the maximum values required to drive the output above 4 V or below 400 mV with a 10-kΩ resistor between the output and V_{DD}. They can be verified by applying the limit value to the input and checking for the appropriate output state.

switching characteristics, V_{DD} = 5 V, T_A = 25°C

PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
Response time	R_L connected to 5 V through 5.1 kΩ, C_L = 15 pF‡, See Note 6	100-mV input step with 5-mV overdrive		650		ns
		TTL-level input step		200		

‡ C_L includes probe and jig capacitance.

NOTE 6: The response time specified is the interval between the input step function and the instant when the output crosses 1.4 V.

PARAMETER MEASUREMENT INFORMATION

The TLC374 must not be tested in the servo-loop configuration often used for operational amplifiers. This device has a digital output stage. Attempts to force the device into the linear region of the transfer curve can cause damage. Test equipment should operate in accordance with the following recommendations and no attempt should be made to measure the gain of the device on an automatic tester.

To verify that V_{IO} falls within the limits specified, the limit value is applied to the input as shown in Figure 1. With IN + positive with respect to IN −, the output should be high. With the input polarity reversed, the output should be low. If it is desired to measure the actual value of V_{IO}, a binary search method can be used to vary the input potential and check the output states until a good approximation of the critical point is obtained.

Measuring the extremely low values of input current requires isolation from all other sources of leakage current or, at least, compensating for the leakage of test socket and board. With a good picoammeter, the socket and board leakage can be measured with no device in the socket and the reading subtracted from that obtained with a device in the socket.

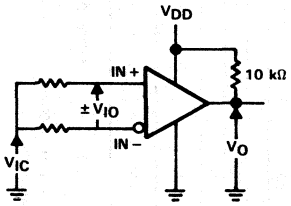


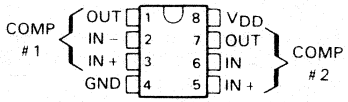
FIGURE 1. TEST CIRCUIT

TLC393M, TLC393I, TLC393C
DUAL MICROPOWER LinCMOS™ COMPARATORS

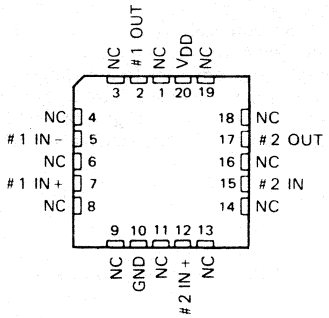
DECEMBER 1986

- Very Low Power ... 100 μW Typ at 5 V
- Fast Response Time ... 2.5 μs Typ with 5 mV Overdrive
- Single Supply Operation:
  TLC393M ... 4 V to 16 V
  TLC393I ... 3 V to 16 V
  TLC393C ... 3 V to 16 V
- High Input Impedance ... $10^{12}\Omega$ Typ
- Input Offset Voltage Change at Worst Case Input Condition Typically 0.23 μV/Month Including the First 30 Days
- On-Chip ESD Protection

TLC393M ... JG PACKAGE
TLC393I ... D, JG, OR P PACKAGE
TLC393C ... D, JG, OR P PACKAGE
(TOP VIEW)



TLC393M ... FK PACKAGE
(TOP VIEW)

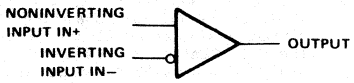


NC – No internal connection

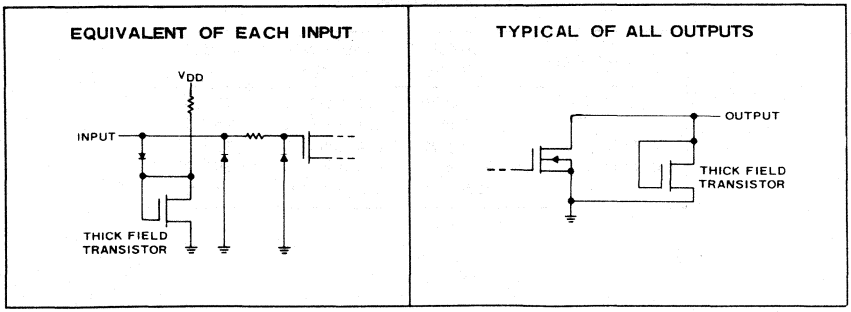
description

The TLC393 consists of two independent differential-voltage comparators designed to operate from a single supply. It is functionally similar to the LM393 but uses 1/20th the power for similar response times. The open-drain MOS output stage will interface to a variety of loads and supplies, as well as "wired" logic functions. For a similar device with a push-pull output configuration, see the TLC3702 data sheet.

symbol (each comparator)



schematics of inputs and outputs



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TLC393M, TLC393I, TLC393C
DUAL MICROPOWER LinCMOS™ COMPARATORS

Texas Instruments LinCMOS process offers superior analog performance to standard CMOS processes. Along with the standard CMOS advantages of low power without sacrificing speed, high input impedance, and low bias currents, the LinCMOS process offers extremely stable input offset voltages, even with differential input stresses of several volts. This characteristic makes it possible to build reliable CMOS comparators.

The TLC393M is characterized for operation over the full military temperature range of -55°C to 125°C. The TLC393I is characterized for operation over the extended industrial temperature range of -40°C to 85°C. The TLC393C is characterized for operation over the commercial temperature range of 0°C to 70°C.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{DD} (see Note 1)	-0.3 V to 18 V
Differential input voltage (see Note 2)	±18 V
Input voltage, V_I	-0.3 V to V_{DD}
Output voltage, V_O	-0.3 V to V_{DD}
Input current, I_I	±5 mA
Output current, I_O (each output)	20 mA
Total supply current into V_{DD} terminal	40 mA
Total current out of ground terminal	40 mA
Continuous total dissipation at (or below) 25°C free-air temperature (see Note 3):	
D package	725 mW
FK	1375 mW
JG package (alloy mount)	1025 mW
JG package (glass mount)	825 mW
P package	725 mW
Operating free-air temperature range: TLC393M	-55°C to 125°C
TLC393I	-40°C to 85°C
TLC393C	0°C to 70°C
Storage temperature range	-65°C to 150°C
Lead temperature 1.6 mm (1/16 inch) from case for 60 seconds: FK or JG package	300°C
Lead temperature 1.6 mm (1/16 inch) from case for 10 seconds: D or P package	260°C

NOTES: 1. All voltage values, except differential voltages, are with respect to network ground.
2. Differential voltages are at the noninverting input with respect to the inverting input.
3. For operation above 25°C free-air temperature, refer to the Dissipation Derating Table. For the TLC393M in the JG package, use the alloy mount derating factor; for the TLC393I and TLC393C in the JG package, use the glass mount derating factor.

DISSIPATION DERATING TABLE

PACKAGE	POWER RATING	DERATING FACTOR	ABOVE T_A
D	725 mW	5.8 mW/°C	25°C
FK	1375 mW	11 mW/°C	25°C
JG (alloy mount)	1050 mW	8.4 mW/°C	25°C
JG (glass mount)	825 mW	6.6 mW/°C	25°C
P	725 mW	5.8 mW/°C	25°C

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage, V_{DD}	4	5	16	V
Common-mode input voltage, V_{IC}	-0.2		V_{DD}-1.5	V
Low-level output current, I_{OL}		8	20	mA
Operating free-air temperature, T_A	-55		125	°C

electrical characteristics at specified operating free-air temperature, V_{DD} = 5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS †		MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage	V_{IC} = V_{ICR}min, V_{DD} = 5 V to 10 V, See Note 4	25°C		1.4	5	mV
			Full range			10	
I_{IO}	Input offset current	V_{IC} = 2.5 V	25°C		1		pA
			125°C			15	nA
I_{IB}	Input bias current	V_{IC} = 2.5 V	25°C		5		pA
			125°C			30	nA
V_{ICR}	Common-mode input voltage range		25°C	0 to V_{DD}-1			V
			Full range	0 to V_{DD}-1.5			
CMRR	Common-mode rejection ratio	V_{IC} = V_{ICR}min	25°C		84		dB
			125°C		84		
			-55°C		84		
k_{SVR}	Supply voltage rejection ratio	V_{DD} = 5 V to 10 V	25°C		85		dB
			125°C		84		
			-55°C		84		
V_{OL}	Low-level output voltage	V_{ID} = -1 V, I_{OL} = 6 mA	25°C		300	400	mV
			125°C			800	
I_{OH}	High-level output current	V_{ID} = 1 V, V_O = 5 V	25°C		0.8	40	nA
			125°C			1	μA
I_{DD}	Supply current (both comparators)	No load, Outputs low	25°C		22	40	μA
			Full range			90	

† All characteristics are measured with zero common-mode voltage unless otherwise noted. Full range is -55°C to 125°C for the TLC393M.

NOTE 4: The offset voltage limits given are the maximum values required to drive the output up to 4.5 V or down to 0.3 V.

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage, V_{DD}	3	5	16	V
Common-mode input voltage, V_{IC}	-0.2		V_{DD}-1.5	V
Low-level output current, I_{OL}		8	20	mA
Operating free-air temperature, T_A	-40		85	°C

electrical characteristics at specified operating free-air temperature, V_{DD} = 5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS †		MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage	V_{IC} = V_{ICR}min, V_{DD} = 5 V to 10 V, See Note 4	25°C		1.4	5	mV
			Full range			7	
I_{IO}	Input offset current	V_{IC} = 2.5 V	25°C		1		pA
			85°C			1	nA
I_{IB}	Input bias current	V_{IC} = 2.5 V	25°C		5		pA
			85°C			2	nA
V_{ICR}	Common-mode input voltage range		25°C	0 to V_{DD}-1			V
			Full range	0 to V_{DD}-1.5			
CMRR	Common-mode rejection ratio	V_{IC} = V_{ICR}min	25°C		84		dB
			84°C		84		
			-40°C		84		
k_{SVR}	Supply voltage rejection ratio	V_{DD} = 5 V to 10 V	25°C		85		dB
			85°C		85		
			-40°C		84		
V_{OL}	Low-level output voltage	V_{ID} = -1 V, I_{OL} = 6 mA	25°C		300	400	mV
			85°C			700	
I_{OH}	High-level output current	V_{ID} = 1 V, V_O = 5 V	25°C		0.8	40	nA
			85°C			1	µA
I_{DD}	Supply current (both comparators)	No load, Outputs low	25°C		22	40	µA
			Full range			65	

† All characteristics are measured with zero common-mode voltage unless otherwise noted. Full range is -40°C to 85°C for the TLC393I.

NOTE 4: The offset voltage limits given are the maximum values required to drive the output up to 4.5 V or down to 0.3 V.

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage, V_{DD}	3	5	16	V
Common-mode input voltage, V_{IC}	-0.2		V_{DD}-1.5	V
Low-level output current, I_{OL}		8	20	mA
Operating free-air temperature, T_A	0		70	°C

electrical characteristics at specified operating free-air temperature, V_{DD} = 5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS †		MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage	V_{IC} = V_{ICR}min, V_{DD} = 5 V to 10 V, See Note 4	25°C		1.4	5	mV
			Full range			6.5	
I_{IO}	Input offset current	V_{IC} = 2.5 V	25°C		1		pA
			70°C			0.3	nA
I_{IB}	Input bias current	V_{IC} = 2.5 V	25°C		5		pA
			70°C			0.6	nA
V_{ICR}	Common-mode input voltage range		25°C	0 to V_{DD}-1			V
			Full range	0 to V_{DD}-1.5			
CMRR	Common-mode rejection ratio	V_{IC} = V_{ICR}min	25°C		84		dB
			70°C		84		
			0°C		84		
k_{SVR}	Supply voltage rejection ratio	V_{DD} = 5 V to 10 V	25°C		85		dB
			70°C		85		
			0°C		85		
V_{OL}	Low-level output voltage	V_{ID} = -1 V, I_{OL} = 6 mA	25°C		300	400	mV
			70°C			650	
I_{OH}	High-level output current	V_{ID} = 1 V, V_O = 5 V	25°C		0.8	40	nA
			70°C			1	µA
I_{DD}	Supply current (both comparators)	No load, Outputs low	25°C		22	40	µA
			Full range			50	

† All characteristics are measured with zero common-mode voltage unless otherwise noted. Full range is 0°C to 70°C for the TLC393C.

NOTE 4: The offset voltage limits given are the maximum values required to drive the output up to 4.5 V or down to 0.3 V.

switching charactistics, V_{DD} = 5 V, T_A = 25°C (see Figure 3)

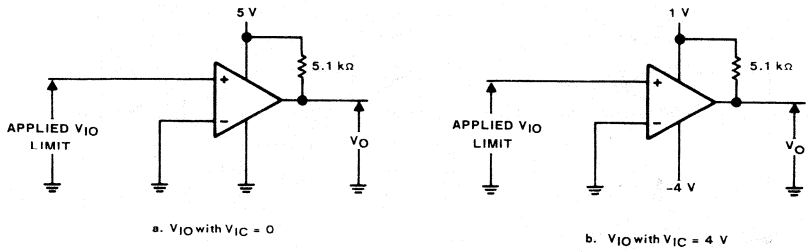
PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_{PHL}	Response time, high-to-low-level output	f = 10 kHz, C_L = 15 pF	Overdrive = 2 mV		3.6		µs
			Overdrive = 5 mV		2.1		
			Overdrive = 10 mV		1.3		
			Overdrive = 20 mV		0.85		
			Overdrive = 40 mV		0.55		
		V_I = 1.4 V step at IN+ pin			0.10		
t_{PLH}	Response time, low-to-high-level output	f = 10 kHz, C_L = 15 pF	Overdrive = 2 mV		4.5		µs
			Overdrive = 5 mV		2.5		
			Overdrive = 10 mV		1.7		
			Overdrive = 20 mV		1.2		
			Overdrive = 40 mV		1.0		
		V_I = 1.4 V step at IN+ pin			1.1		
t_{THL}	Transition time, high-to-low-level output	f = 10 kHz, C_L = 15 pF	Overdrive = 50 mV		20		ns

PARAMETER MEASUREMENT INFORMATION

The TLC393 contains a digital output stage which, if held in the linear region of the transfer curve, can cause damage to the device. Conventional operational amplifier/comparator testing incorporates the use of a servo-loop which is designed to force the device output to a level within this linear region. Since the servo-loop method of testing cannot be used, we offer the following alternatives for measuring parameters such as input offset voltage, common-mode rejection, etc.

To verify that the input offset voltage falls within the limits specified, the limit value is applied to the input as shown in Figure 1a. With the noninverting input positive with respect to the inverting input, the output should be high. With the input polarity reversed, the output should be low.

A similar test can be made to verify the input offset voltage at the common-mode extremes. The supply voltages can be slewed as shown in Figure 1b for the V_{ICR} test, rather than changing the input voltages, to provide greater accuracy.



a. V_{IO} with V_{IC} = 0

b. V_{IO} with V_{IC} = 4 V

FIGURE 1. METHOD FOR VERIFYING THAT INPUT OFFSET VOLTAGE IS WITHIN SPECIFIED LIMITS

A close approximation of the input offset voltage can be obtained by using a binary search method to vary the differential input voltage while monitoring the output state. When the applied input voltage differential is equal, but opposite in polarity, to the input offset voltage, the output will change states.

PARAMETER MEASUREMENT INFORMATION

Figure 2 illustrates a practical circuit for direct d.c. measurement of input offset voltage that does not bias the comparator into the linear region. The circuit consists of a switching mode servo loop in which IC1a generates a triangular waveform of approximately 20 mV amplitude. IC1b acts as a buffer, with C2 and R4 removing any residual d.c. offset. The signal is then applied to the inverting input of the comparator under test, while the noninverting input is driven by the output of the integrator formed by IC1c through the voltage divider formed by R9 and R10. The loop reaches a stable operating point when the output of the comparator under test has a duty cycle of exactly 50%, which can only occur when the incoming triangle wave is "sliced" symmetrically or when the voltage at the noninverting input exactly equals the input offset voltage.

Voltage divider R9 and R10 provides a step-up of the input offset voltage by a factor of 100 to make measurement easier. The values of R5, R8, R9, and R10 can significantly influence the accuracy of the reading; therefore, it is suggested that their tolerance level be one percent or lower.

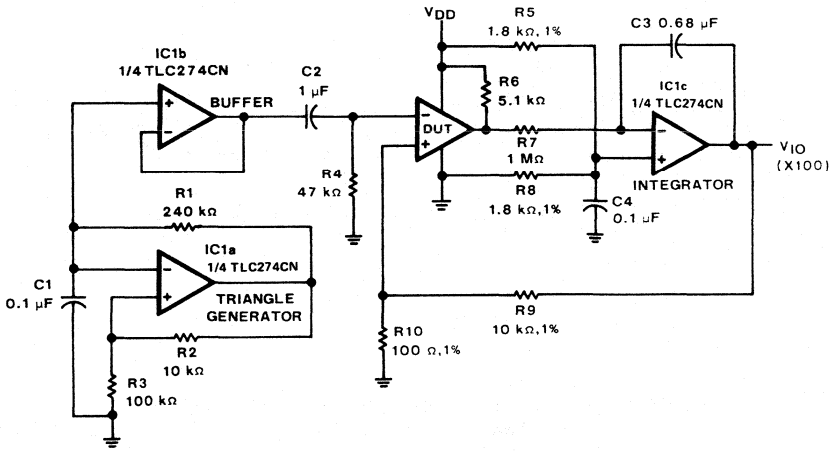
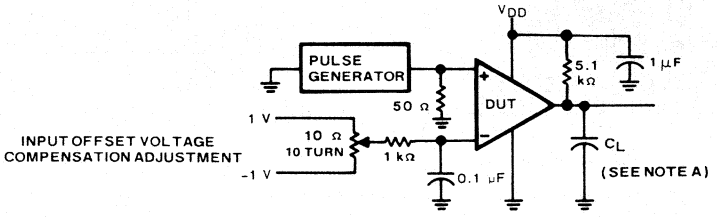


FIGURE 2. CIRCUIT FOR INPUT OFFSET VOLTAGE MEASUREMENT

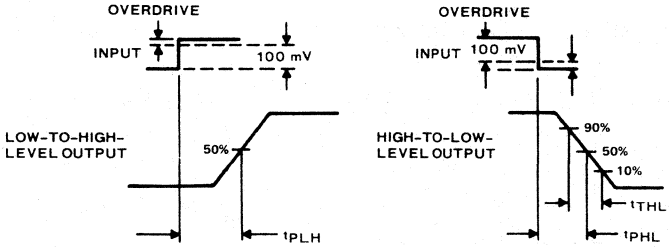
Measuring the extremely low values of input current requires isolation from all other sources of leakage current and compensation for the leakage of the test socket and board. With a good picoammeter, the socket and board leakage can be measured with no device in the socket. Subsequently, this open socket leakage value can be subtracted from the measurement obtained with a device in the socket to obtain the actual input current of the device.

PARAMETER MEASUREMENT INFORMATION

Response time is defined as the interval between the application of an input step function and the instant when the output reaches 50% of its maximum value. Response time, low-to-high-level output is measured from the leading edge of the input pulse, while response time, high-to-low-level output, is measured from the trailing edge of the input pulse. Response time measurement at low input signal levels can be greatly affected by the input offset voltage. The offset voltage should be balanced by the adjustment at the inverting input (as shown in Figure 3) so that the circuit is just at the transition point. Then a low signal, for example 105 mV or 5 mV overdrive, will cause the output to change state.



TEST CIRCUIT



VOLTAGE WAVEFORMS

NOTE A: C_L includes probe and jig capacitance.

FIGURE 3. RESPONSE, RISE, AND FALL TIMES
CIRCUIT AND VOLTAGE WAVEFORMS

TYPICAL CHARACTERISTICS

DISTRIBUTION OF INPUT OFFSET VOLTAGE

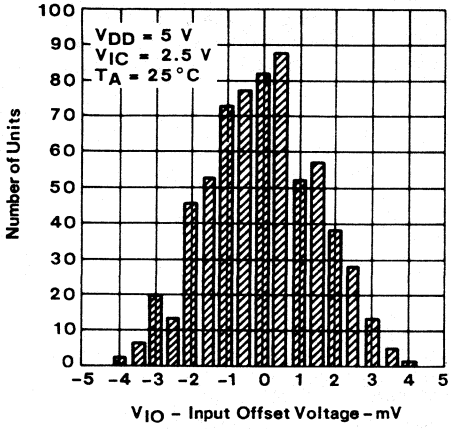


FIGURE 4

INPUT BIAS CURRENT vs FREE-AIR TEMPERATURE

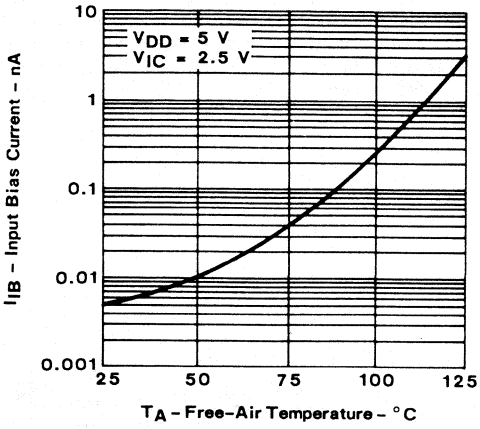


FIGURE 5

COMMON-MODE REJECTION RATIO vs FREE-AIR TEMPERATURE

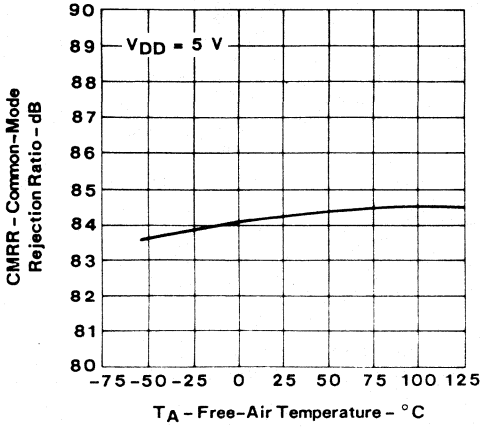


FIGURE 6

SUPPLY VOLTAGE REJECTION RATIO vs FREE-AIR TEMPERATURE

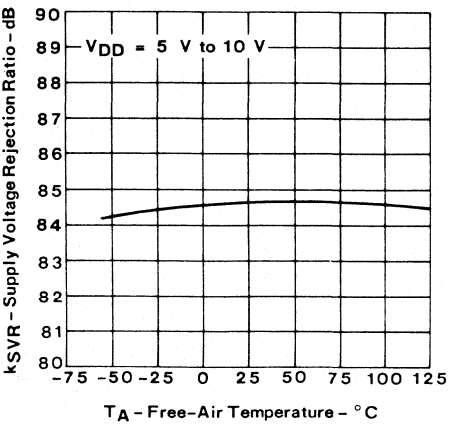


FIGURE 7

TYPICAL CHARACTERISTICS

HIGH-LEVEL OUTPUT CURRENT
vs
HIGH-LEVEL OUTPUT VOLTAGE

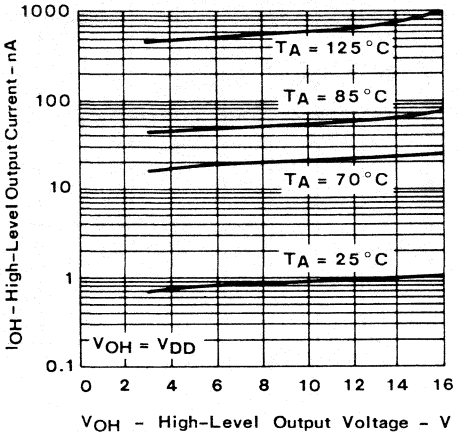


FIGURE 8

HIGH-LEVEL OUTPUT CURRENT
vs
FREE-AIR TEMPERATURE

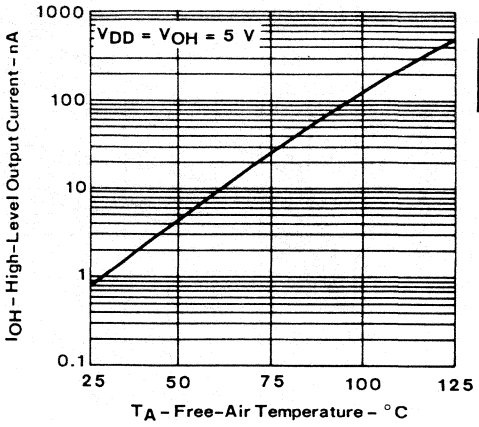


FIGURE 9

LOW-LEVEL OUTPUT VOLTAGE
vs
LOW-LEVEL OUTPUT CURRENT

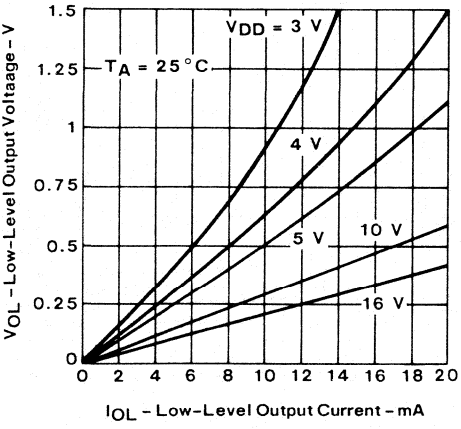


FIGURE 10

LOW-LEVEL OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE

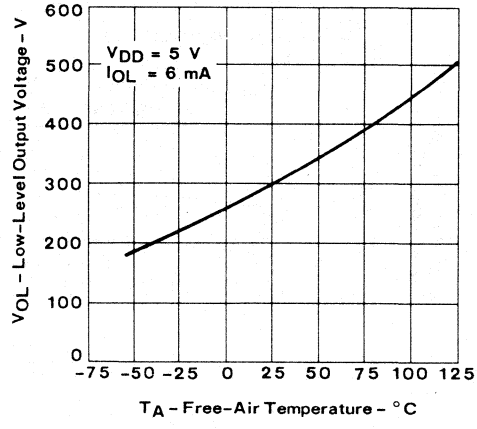


FIGURE 11

TYPICAL CHARACTERISTICS

SUPPLY CURRENT
vs
SUPPLY VOLTAGE

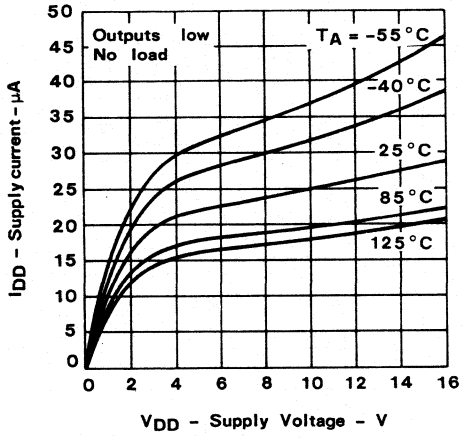


FIGURE 12

SUPPLY CURRENT
vs
FREE-AIR TEMPERATURE

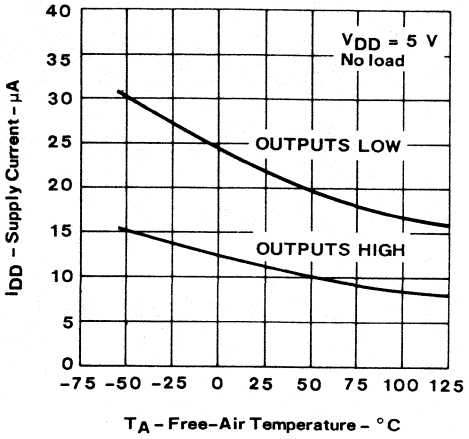


FIGURE 13

LOW-TO-HIGH-LEVEL
OUTPUT RESPONSE TIME
vs
SUPPLY VOLTAGE

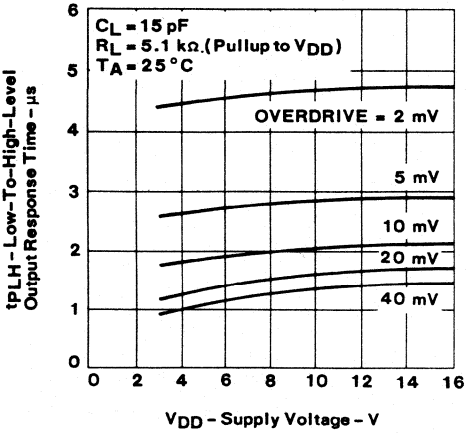


FIGURE 14

HIGH-TO-LOW-LEVEL
OUTPUT RESPONSE TIME
vs
SUPPLY VOLTAGE

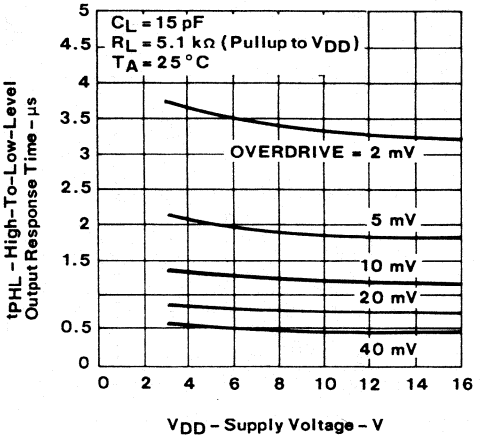


FIGURE 15

TYPICAL CHARACTERISTICS

LOW-TO-HIGH-LEVEL OUTPUT RESPONSE
FOR VARIOUS OVERDRIVE VOLTAGES

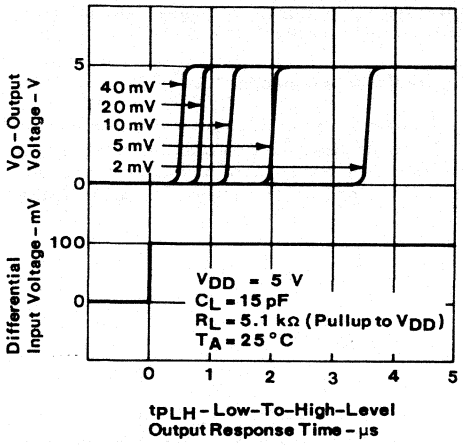


FIGURE 16

OUTPUT FALL TIME
vs
SUPPLY VOLTAGE

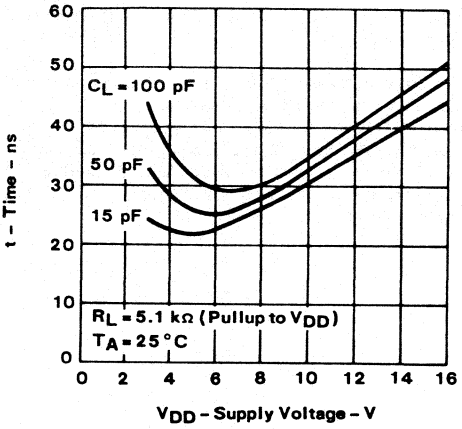


FIGURE 17

HIGH-TO-LOW-LEVEL OUTPUT RESPONSE
FOR VARIOUS OVERDRIVE VOLTAGES

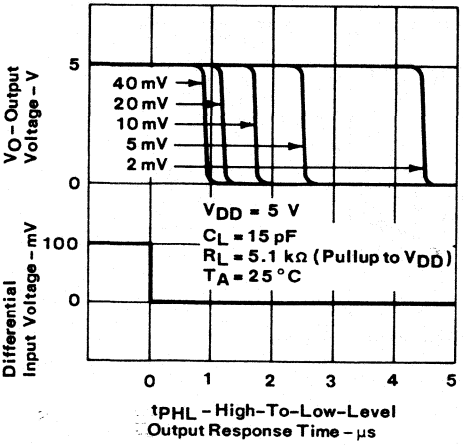


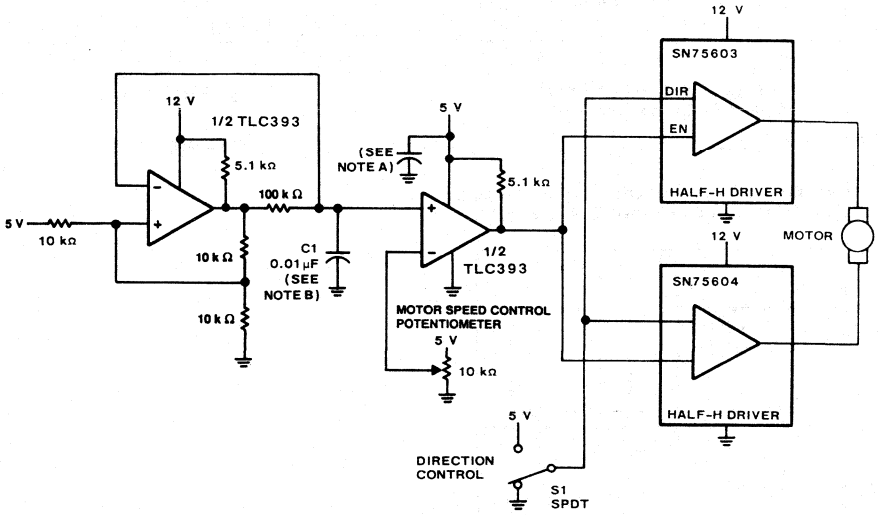
FIGURE 18

TYPICAL APPLICATION DATA

The inputs should always remain within the supply rails in order to avoid forward biasing the diodes in the electrostatic discharge (ESD) protection structure. If either input exceeds this range, the device will not be damaged as long as the input current is limited to less than 5 milliamperes. to maintain the expected output state, the inputs must remain within the common-mode range. For example, at 25°C with V_{DD} = 5 V, both inputs must remain between -0.2 V and 4 V to assure proper device operation.

To assure reliable operation, the supply should be decoupled with a capacitor (0.1 μF) positioned as close to the device as possible.

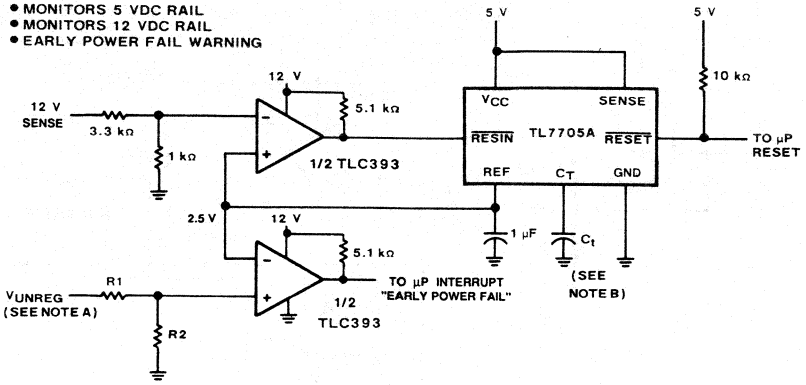
The TLC393 has internal ESD protection circuits that will prevent functional failures at voltages up to 2000 volts as tested under MIL-STD-883C, Method 3015.2; however, care should be exercised in handling these devices as exposure to ESD may result in the degradation of the device parametric performance.



NOTES: A. The recommended minimum capacitance is 10 μF to eliminate common ground switching noise.
B. Select C1 for change in oscillator frequency.

FIGURE 19. PULSE-WIDTH-MODULATED MOTOR SPEED CONTROLLER

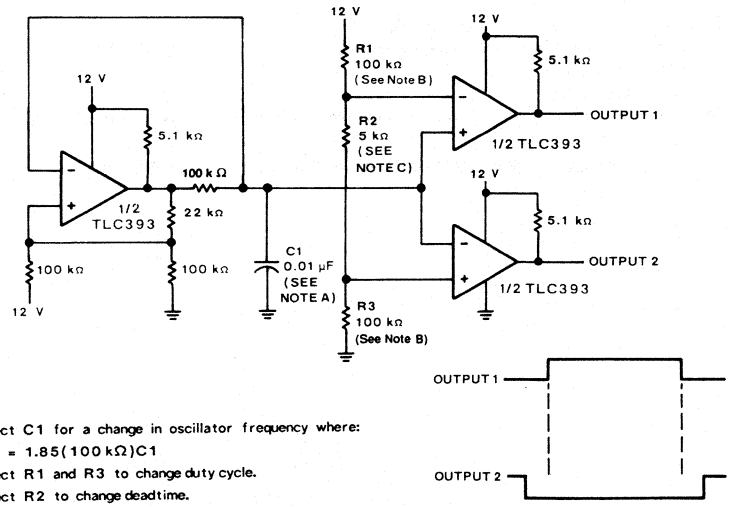
TYPICAL APPLICATION DATA



NOTES: A. $V_{UNREG} = 2.5\left(\frac{R1+R2}{R2}\right)$

B. The value of C_t determines the time delay of reset.

FIGURE 21. ENHANCED SUPPLY SUPERVISOR



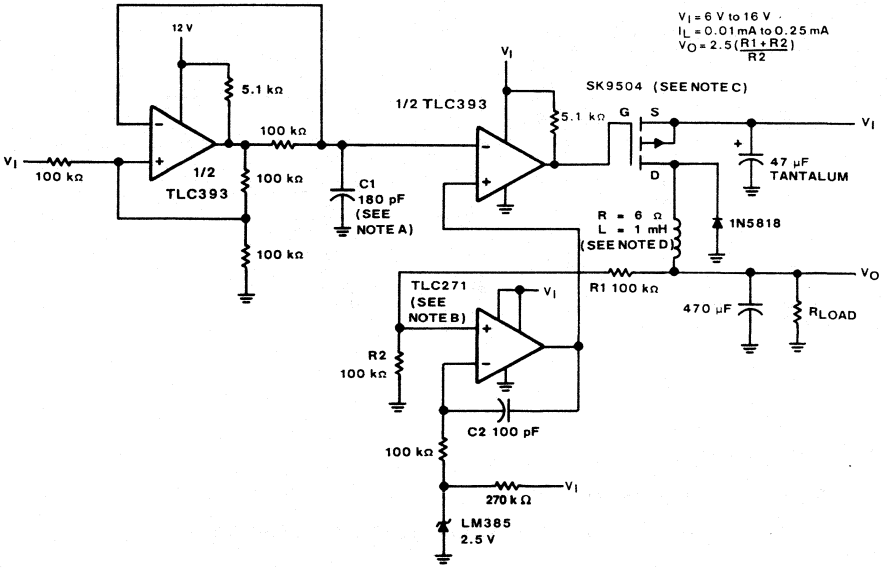
NOTES: A. Select C1 for a change in oscillator frequency where:
$1/f = 1.85(100\,k\Omega)C1$

B. Select R1 and R3 to change duty cycle.

C. Select R2 to change deadtime.

FIGURE 22. TWO-PHASE NONOVERLAPPING CLOCK GENERATOR

TYPICAL APPLICATION DATA



NOTES: A. Select C1 for a change in oscillator frequency.

B. TLC271 – Tie pin 8 to pin 7 for low bias operation.

C. SK9504 – V_{DS} = 40 V
I_{DS} = 1 A

D. To achieve microampere current drive, the inductance of the circuit must be increased.

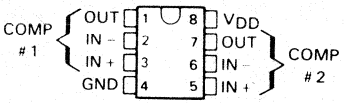
FIGURE 20. MICROPOWER SWITCHING REGULATOR

TLC3702M, TLC3702I, TLC3702C
DUAL MICROPOWER LinCMOS™ COMPARATORS

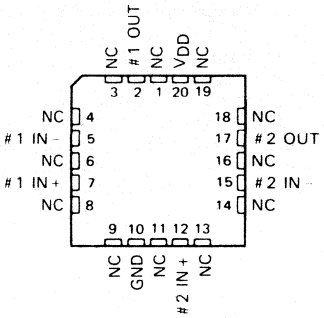
NOVEMBER 1986

- Push-Pull CMOS Output Drives Capacitive Loads without Pull-up Resistor, $I_O = \pm 8$ mA
- Very Low Power ... 100 μW Typ at 5 V
- Fast Response Time ... 2.5 μs Typ with 5 mV Overdrive
- Single Supply Operation:
  TLC3702M ... 4 V to 16 V
  TLC3702I ... 3 V to 16 V
  TLC3702C ... 3 V to 16 V
- High Input Impedance ... $10^{12}\ \Omega$ Typ
- Input Offset Voltage Change at Worst Case Input Condition Typically 0.23 μV/Month Including the First 30 Days
- On-Chip ESD Protection

TLC3702M ... JG PACKAGE
TLC3702I ... D, JG, OR P PACKAGE
TLC3702C ... D, JG, OR P PACKAGE
(TOP VIEW)



TLC3702M ... FK PACKAGE
(TOP VIEW)

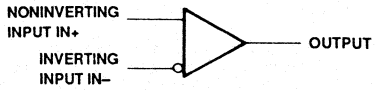


NC — No internal connection

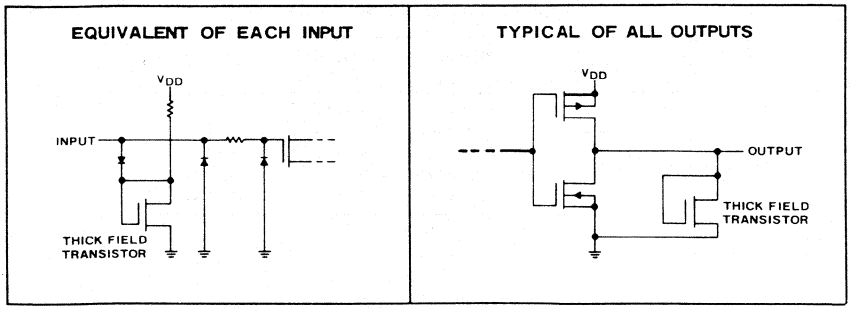
description

The TLC3702 consists of two independent differential-voltage comparators designed to operate from a single supply and be compatible with modern HCMOS logic systems. It is functionally similar to the LM393 but uses 1/20th the power for similar response times. The push-pull CMOS output stage will drive capacitive loads directly without a power-consuming pull-up resistor to achieve the stated response time. Eliminating the pull-up resistor not only reduces power dissipation, but also saves board space and component cost. The output stage is also fully compatible with TTL requirements.

symbol (each comparator)



schematics of inputs and outputs



LinCMOS is a trademark of Texas Instruments

Texas Instruments LinCMOS process offers superior analog performance to standard CMOS processes. Along with the standard CMOS advantages of low power without sacrificing speed, high input impedance, and low bias currents, the LinCMOS process offers extremely stable input offset voltages, even with differential input stresses of several volts. This characteristic makes it possible to build reliable CMOS comparators.

The TLC3702M is characterized for operation over the full military temperature range of -55°C to 125°C. The TLC3702I is characterized for operation over the extended industrial temperature range of -40°C to 85°C. The TLC3702C is characterized for operation over the commercial temperature range of 0°C to 70°C.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{DD} (see Note 1) . . . . . -0.3 V to 18 V
Differential input voltage (see Note 2) . . . . . ±18 V
Input voltage, V_I . . . . . -0.3 V to V_{DD}
Output voltage, V_O . . . . . -0.3 V to V_{DD}
Input current, I_I . . . . . ±5 mA
Output current, I_O (each output) . . . . . ±20 mA
Total supply current into V_{DD} terminal . . . . . 40 mA
Total current out of ground terminal . . . . . 40 mA
Continuous total dissipation at (or below) 25°C free-air temperature (see Note 3):
D package . . . . . 725 mW
FK . . . . . 1375 mW
JG package (alloy mount) 1025mW
JG package (glass mount) . . . . . 825 mW
P package . . . . . 725 mW
Operating free-air temperature range: TLC3702M . . . . . -55°C to 125°C
TLC3702I . . . . . -40°C to 85°C
TLC3702C . . . . . 0°C to 70°C
Storage temperature range . . . . . -65°C to 150°C
Lead temperature 1.6 mm (1/16 inch) from case for 60 seconds: FK or JG package . . . . . 300°C
Lead temperature 1.6 mm (1/16 inch) from case for 10 seconds: D or P package . . . . . 260°C

NOTES: 1. All voltage values, except differential voltages, are with respect to network ground.
2. Differential voltages are at the noninverting input with respect to the inverting input.
3. For operation above 25°C free-air temperature, refer to the Dissipation Derating Table. For the TLC3702M in the JG package, use the alloy mount derating factor; for TLC3702I and TLC3702C in the JG package, use the glass mount derating factor.

DISSIPATION DERATING TABLE

PACKAGE	POWER RATING	DERATING FACTOR	ABOVE T_A
D	725 mW	5.8 mW/°C	25°C
FK	1375 mW	11 mW/°C	25°C
JG (alloy mount)	1050 mW	8.4 mW/°C	25°C
JG (glass mount)	825 mW	6.6 mW/°C	25°C
P	725 mW	5.8 mW/°C	25°C

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage, V_{DD}	4	5	16	V
Common-mode input voltage, V_{IC}	-0.2		V_{DD}-1.5	V
High-level output current, I_{OH}		-8	-20	mA
Low-level output current, I_{OL}		8	20	mA
Operating free-air temperature, T_A	-55		125	°C

electrical characteristics at specified operating free-air temperature, V_{DD} = 5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS †		MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage	V_{IC} = V_{ICR}min, V_{DD} = 5 V to 10 V, See Note 4	25°C		1.2	5	mV
			Full range			10	
I_{IO}	Input offset current	V_{IC} = 2.5 V	25°C		1		pA
			125°C			15	nA
I_{IB}	Input bias current	V_{IC} = 2.5 V	25°C		5		pA
			125°C			30	nA
V_{ICR}	Common-mode input voltage range		25°C	0 to V_{DD}-1			V
			Full range	0 to V_{DD}-1.5			
CMRR	Common-mode rejection ratio	V_{IC} = V_{ICR}min	25°C		84		dB
			125°C		83		
			-55°C		82		
k_{SVR}	Supply voltage rejection ratio	V_{DD} = 5 V to 10 V	25°C		85		dB
			125°C		85		
			-55°C		82		
V_{OH}	High-level output voltage	V_{ID} = 1 V, I_{OH} = -4 mA	25°C	4.5	4.7		V
			125°C	4.2			
V_{OL}	Low-level output voltage	V_{ID} = -1 V, I_{OL} = 4 mA	25°C		210	300	mV
			125°C			500	
I_{DD}	Supply current (both comparators)	No load	25°C		18	40	µA
			Full range			90	

† All characteristics are measured with zero common-mode voltage unless otherwise noted. Full range is -55°C to 125°C for the TLC3702M.

NOTE 4: The offset voltage limits given are the maximum values required to drive the output up to 4.5 V or down to 0.3 V.

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage, V_{DD}	3	5	16	V
Common-mode input voltage, V_{IC}	-0.2		V_{DD}-1.5	V
High-level output current, I_{OH}		-8	-20	mA
Low-level output current, I_{OL}		8	20	mA
Operating free-air temperature, T_A	-40		85	°C

electrical characteristics at specified operating free-air temperature, V_{DD} = 5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS †		MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage	V_{IC} = V_{ICR}min, V_{DD} = 5 V to 10 V, See Note 4	25°C		1.2	5	mV
			Full range			7	
I_{IO}	Input offset current	V_{IC} = 2.5 V	25°C		1		pA
			85°C			1	nA
I_{IB}	Input bias current	V_{IC} = 2.5 V	25°C		5		pA
			85°C			2	nA
V_{ICR}	Common-mode input voltage range		25°C	0 to V_{DD}-1			V
			Full range	0 to V_{DD}-1.5			
CMRR	Common-mode rejection ratio	V_{IC} = V_{ICR}min	25°C		84		dB
			85°C		84		
			-40°C		83		
k_{SVR}	Supply voltage rejection ratio	V_{DD} = 5 V to 10 V	25°C		85		dB
			85°C		85		
			-40°C		83		
V_{OH}	High-level output voltage	V_{ID} = 1 V, I_{OH} = -4 mA	25°C	4.5	4.7		V
			85°C	4.3			
V_{OL}	Low-level output voltage	V_{ID} = -1 V, I_{OL} = 4 mA	25°C		210	300	mV
			85°C			400	
I_{DD}	Supply current (both comparators)	No load	25°C		18	40	µA
			Full range			65	

† All characteristics are measured with zero common-mode voltage unless otherwise noted. Full range is -40°C to 85°C for the TLC3702I.

NOTE 4: The offset voltage limits given are the maximum values required to drive the output up to 4.5 V or down to 0.3 V.

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage, V_{DD}	3	5	16	V
Common-mode input voltage, V_{IC}	-0.2		V_{DD}-1.5	V
High-level output current, I_{OH}		-8	-20	mA
Low-level output current, I_{OL}		8	20	mA
Operating free-air temperature, T_A	0		70	°C

electrical characteristics at specified operating free-air temperature, V_{DD} = 5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS †		MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage	V_{IC} = V_{ICR}min, V_{DD} = 5 V to 10 V, See Note 4	25°C		1.2	5	mV
			Full range			6.5	
I_{IO}	Input offset current	V_{IC} = 2.5 V	25°C		1		pA
			70°C			0.3	nA
I_{IB}	Input bias current	V_{IC} = 2.5 V	25°C		5		pA
			70°C			0.6	nA
V_{ICR}	Common-mode input voltage range		25°C	0 to V_{DD}-1			V
			Full range	0 to V_{DD}-1.5			
CMRR	Common-mode rejection ratio	V_{IC} = V_{ICR}min	25°C		84		dB
			70°C		84		
			0°C		84		
k_{SVR}	Supply voltage rejection ratio	V_{DD} = 5 V to 10 V	25°C		85		dB
			70°C		85		
			0°C		85		
V_{OH}	High-level output voltage	V_{ID} = 1 V, I_{OH} = -4 mA	25°C	4.5	4.7		V
			70°C	4.3			
V_{OL}	Low-level output voltage	V_{ID} = -1 V, I_{OL} = 4 mA	25°C		210	300	mV
			70°C			375	
I_{DD}	Supply current (both comparators)	No load	25°C		18	40	μA
			Full range			50	

† All characteristics are measured with zero common-mode voltage unless otherwise noted. Full range is 0°C to 70°C for the TLC3702C.

NOTE 4: The offset voltage limits given are the maximum values required to drive the output up to 4.5 V or down to 0.3 V.

switching charactistics, V_{DD} = 5 V, T_A = 25°C (see Figure 3)

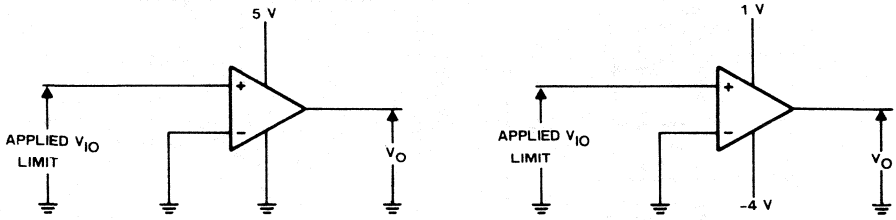
PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_{PHL}	Response time, high-to-low-level output	f = 10 kHz, C_L = 50 pF	Overdrive = 2 mV		4.0		µs
			Overdrive = 5 mV		2.3		
			Overdrive = 10 mV		1.5		
			Overdrive = 20 mV		0.95		
			Overdrive = 40 mV		0.65		
		V_I = 1.4 V step at IN+ pin			0.15		
t_{PLH}	Response time, low-to-high-level output	f = 10 kHz, C_L = 50 pF	Overdrive = 2 mV		4.5		µs
			Overdrive = 5 mV		2.7		
			Overdrive = 10 mV		1.9		
			Overdrive = 20 mV		1.4		
			Overdrive = 40 mV		1.0		
		V_I = 1.4 V step at IN+ pin			1.3		
t_{THL}	Transition time, high-to-low-level output	f = 10 kHz, C_L = 50 pF	Overdrive = 50 mV		50		ns
t_{TLH}	Transition time, low-to-high-level output	f = 10 kHz, C_L = 50 pF	Overdrive = 50 mV		125		ns

PARAMETER MEASUREMENT INFORMATION

The TLC3702 contains a digital output stage which, if held in the linear region of the transfer curve, can cause damage to the device. Conventional operational amplifier/comparator testing incorporates the use of a servo-loop which is designed to force the device output to a level within this linear region. Since the servo-loop method of testing cannot be used, we offer the following alternatives for measuring parameters such as input offset voltage, common-mode rejection, etc.

To verify that the input offset voltage falls within the limits specified, the limit value is applied to the input as shown in Figure 1a. With the noninverting input positive with respect to the inverting input, the output should be high. With the input polarity reversed, the output should be low.

A similar test can be made to verify the input offset voltage at the common-mode extremes. The supply voltages can be slewed as shown in Figure 1b for the V_{ICR} test, rather than changing the input voltages, to provide greater accuracy.



a. V_{IO} with V_{IC} = 0 V

b. V_{IO} with V_{IC} = 4 V

FIGURE 1. METHOD FOR VERIFYING THAT INPUT OFFSET VOLTAGE IS WITHIN SPECIFIED LIMITS

A close approximation of the input offset voltage can be obtained by using a binary search method to vary the differential input voltage while monitoring the output state. When the applied input voltage differential is equal, but opposite in polarity, to the input offset voltage, the output will change states.

PARAMETER MEASUREMENT INFORMATION

Figure 2 illustrates a practical circuit for direct d.c. measurement of input offset voltage that does not bias the comparator into the linear region. The circuit consists of a switching mode servo loop in which IC1a generates a triangular waveform of approximately 20 mV amplitude. IC1b acts as a buffer, with C2 and R4 removing any residual d.c. offset. The signal is then applied to the inverting input of the comparator under test, while the noninverting input is driven by the output of the integrator formed by IC1c through the voltage divider formed by R8 and R9. The loop reaches a stable operating point when the output of the comparator under test has a duty cycle of exactly 50%, which can only occur when the incoming triangle wave is "sliced" symmetrically or when the voltage at the noninverting input exactly equals the input offset voltage.

Voltage divider R8 and R9 provides a step-up of the input offset voltage by a factor of 100 to make measurement easier. The values of R5, R7, R8, and R9 can significantly influence the accuracy of the reading; therefore, it is suggested that their tolerance level be one percent or lower.

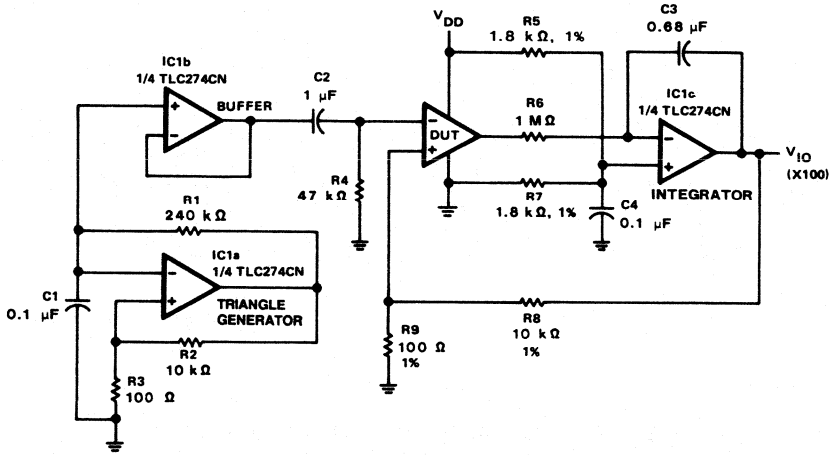


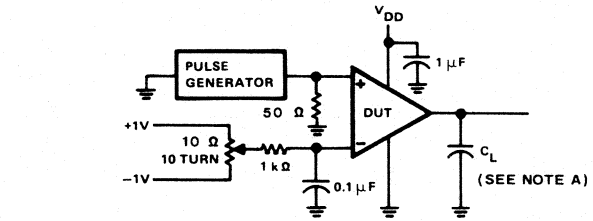
FIGURE 2. CIRCUIT FOR INPUT OFFSET VOLTAGE MEASUREMENT

Measuring the extremely low values of input current requires isolation from all other sources of leakage current and compensation for the leakage of the test socket and board. With a good picoammeter, the socket and board leakage can be measured with no device in the socket. Subsequently, this open socket leakage value can be subtracted from the measurement obtained with a device in the socket to obtain the actual input current of the device.

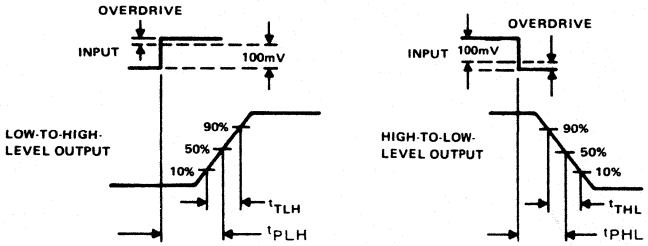
PARAMETER MEASUREMENT INFORMATION

Response time is defined as the interval between the application of an input step function and the instant when the output reaches 50% of its maximum value. Response time, low-to-high-level output is measured from the leading edge of the input pulse, while response time, high-to-low-level output, is measured from the trailing edge of the input pulse. Response time measurement at low input signal levels can be greatly affected by the input offset voltage. The offset voltage should be balanced by the adjustment at the inverting input (as shown in Figure 3) so that the circuit is just at the transition point. Then a low signal, for example 105 mV or 5 mV overdrive, will cause the output to change state.

Rise time is defined as the time required for the output to change from 10% to 90% of its final value. Similarly, fall time is defined as the time required for the output voltage to change from 90% to 10% of its final value (see Figure 3).



TEST CIRCUIT



VOLTAGE WAVEFORMS

NOTE A: C_L includes probe and jig capacitance.

FIGURE 3. RESPONSE, RISE, AND FALL TIMES CIRCUIT AND VOLTAGE WAVEFORMS

TYPICAL CHARACTERISTICS

DISTRIBUTION OF INPUT OFFSET VOLTAGE

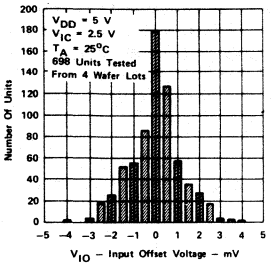


FIGURE 4

INPUT BIAS CURRENT vs FREE-AIR TEMPERATURE

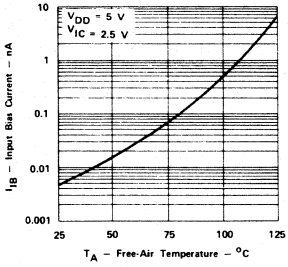


FIGURE 5

COMMON-MODE REJECTION RATIO vs FREE-AIR TEMPERATURE

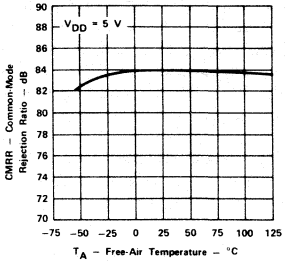


FIGURE 6

HIGH-LEVEL OUTPUT VOLTAGE vs HIGH-LEVEL OUTPUT CURRENT

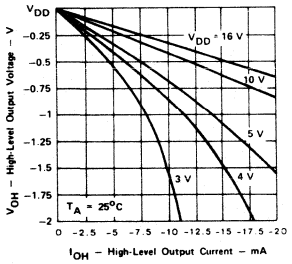


FIGURE 7

HIGH-LEVEL OUTPUT VOLTAGE vs FREE-AIR TEMPERATURE

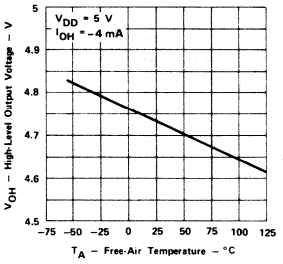


FIGURE 8

SUPPLY VOLTAGE REJECTION RATIO vs FREE-AIR TEMPERATURE

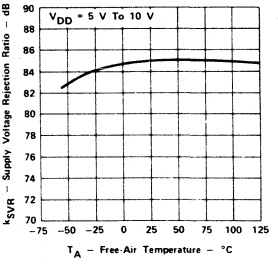


FIGURE 9

LOW-LEVEL OUTPUT VOLTAGE vs LOW-LEVEL OUTPUT CURRENT

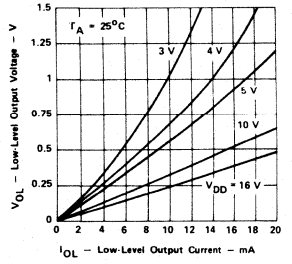


FIGURE 10

LOW-LEVEL OUTPUT VOLTAGE vs FREE-AIR TEMPERATURE

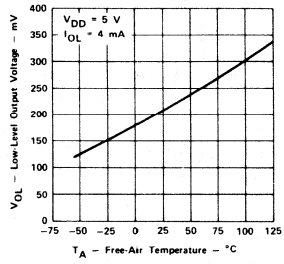


FIGURE 11

OUTPUT TRANSITION TIME vs LOAD CAPACITANCE

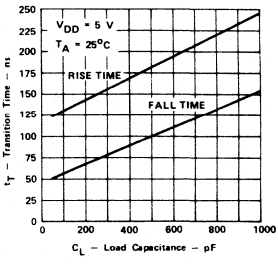


FIGURE 12

TYPICAL CHARACTERISTICS

SUPPLY CURRENT RESPONSE
TO AN OUTPUT VOLTAGE TRANSITION

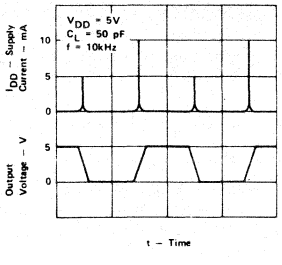


FIGURE 13

LOW-TO-HIGH LEVEL OUTPUT RESPONSE
FOR VARIOUS INPUT OVERDRIVES

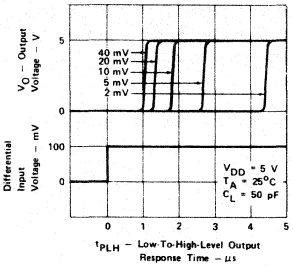


FIGURE 14

HIGH-TO-LOW-LEVEL OUTPUT RESPONSE
FOR VARIOUS INPUT OVERDRIVES

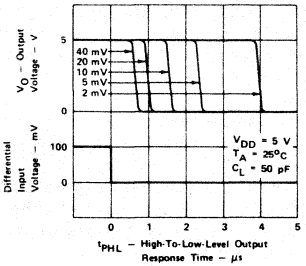


FIGURE 15

LOW-TO-HIGH LEVEL
OUTPUT RESPONSE TIME
vs
SUPPLY VOLTAGE

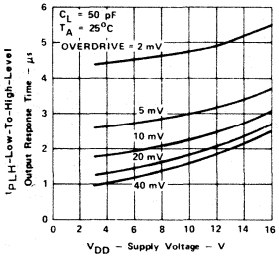


FIGURE 16

HIGH-TO-LOW LEVEL
OUTPUT RESPONSE TIME
vs
SUPPLY VOLTAGE

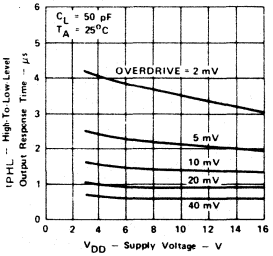


FIGURE 17

AVERAGE SUPPLY CURRENT
(PER COMPARATOR)
vs
FREQUENCY

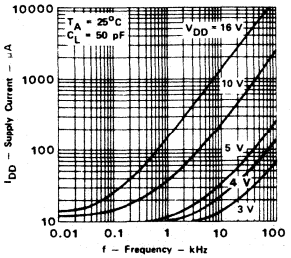


FIGURE 18

SUPPLY CURRENT
vs
SUPPLY VOLTAGE

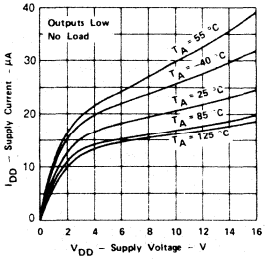


FIGURE 19

SUPPLY CURRENT
vs
FREE-AIR TEMPERATURE

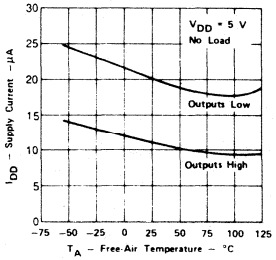


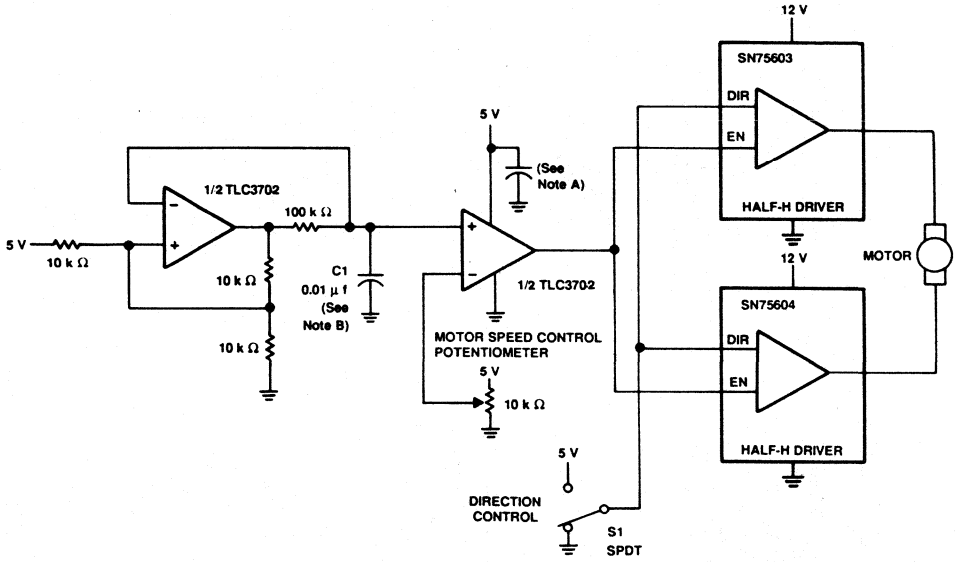
FIGURE 20

TYPICAL APPLICATION DATA

The inputs should always remain within the supply rails in order to avoid forward biasing the diodes in the electrostatic discharge (ESD) protection structure. If either input exceeds this range, the device will not be damaged as long as the input current is limited to less than 5 milliamperes. To maintain the expected output state, the inputs must remain within the common-mode range. For example, at 25°C with V_{DD} = 5 V, both inputs must remain between -0.2 V and 4 V to assure proper device operation.

To assure reliable operation, the supply should be decoupled with a capacitor (0.1 μF) positioned as close to the device as possible.

The TLC3702 has internal ESD protection circuits that will prevent functional failures at voltages up to 2000 volts as tested under MIL-STD-883C, Method 3015.2; however, care should be exercised in handling these devices as exposure to ESD may result in the degradation of the device parametric performance.

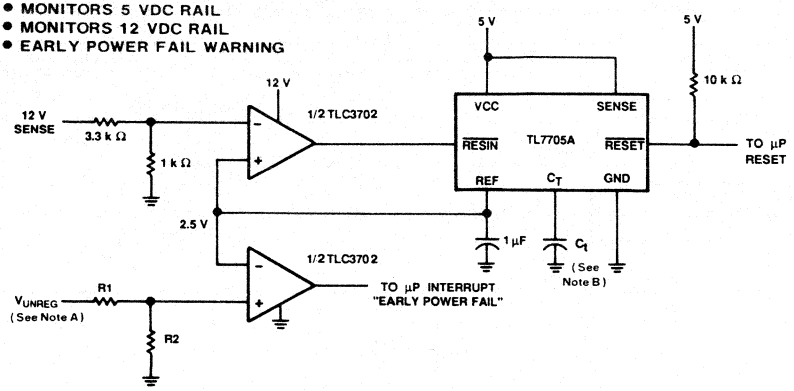


NOTES. A. The recommended minimum capacitance is 10 μF to eliminate common ground switching noise.
B. Adjust C1 for change in oscillator frenquency.

FIGURE 21. PULSE-WIDTH-MODULATED MOTOR SPEED CONTROLLER

TYPICAL APPLICATION DATA

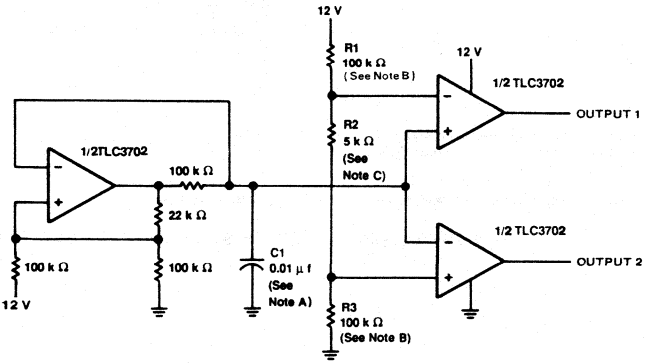
- MONITORS 5 VDC RAIL
- MONITORS 12 VDC RAIL
- EARLY POWER FAIL WARNING

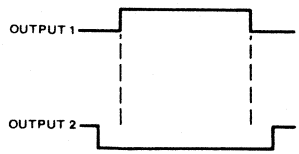


NOTES: A. $V_{UNREG} = 2.5\left(\frac{R1 + R2}{R2}\right)$

B. The value of C_t determines the time delay of reset.

FIGURE 22. ENHANCED SUPPLY SUPERVISOR

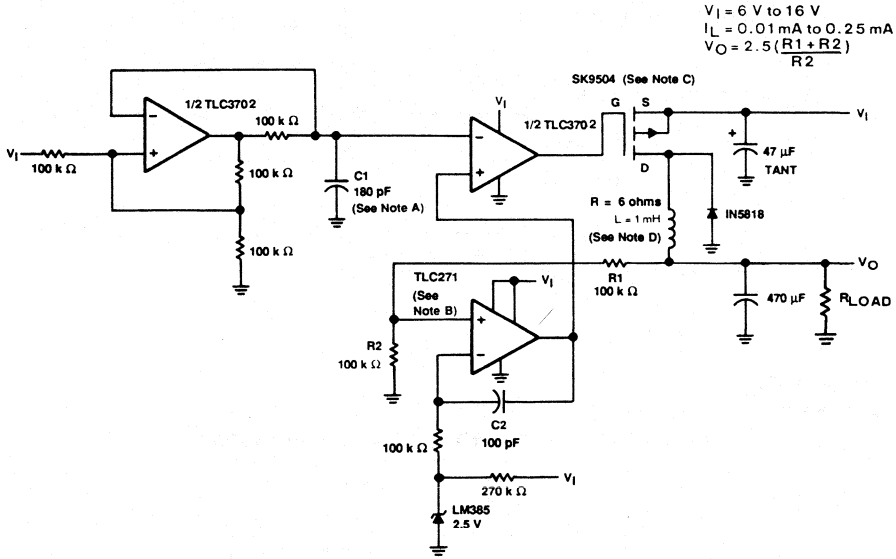




NOTES: A. Adjust C1 for a change in oscillator frequency where:
$1/f = 1.85(100\,k\Omega)C1$
B. Adjust R1 and R3 to change duty cycle
C. Adjust R2 to change deadtime

FIGURE 23. TWO-PHASE NONOVERLAPPING CLOCK GENERATOR

TYPICAL APPLICATION DATA



NOTES: A. Adjust C1 for a change in oscillator frequency
B. TLC271 — Tie pin 8 to pin 7 for low bias operation
C. SK9504 — VDS = 40 V
IDS = 1 A
D. To achieve microampere current drive, the inductance of the circuit must be increased.

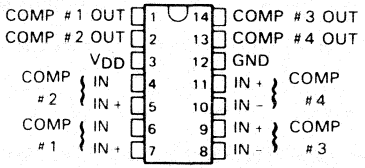
FIGURE 24. MICROPOWER SWITCHING REGULATOR

TLC3704M, TLC3704I, TLC3704C
QUADRUPLE MICROPOWER LinCMOS™ COMPARATORS

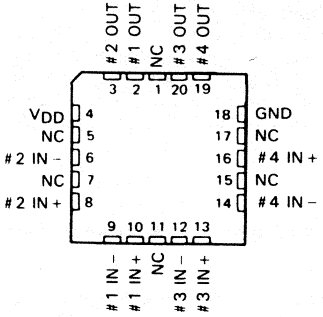
NOVEMBER 1986

- Push-Pull CMOS Output Drives Capacitive Loads without Pull-up Resistor, $I_O = \pm 8$ mA
- Very Low Power ... 200 μW Typ at 5 V
- Fast Response Time ... 2.5 μs Typ with 5 mV Overdrive
- Single Supply Operation:
  TLC3704M ... 4 V to 16 V
  TLC3704I ... 3 V to 16 V
  TLC3704C ... 3 V to 16 V
- High Input Impedance ... $10^{12}\ \Omega$ Typ
- Input Offset Voltage Change at Worst Case Input Condition Typically 0.23 μV/Month Including the First 30 Days
- On-Chip ESD Protection

TLC3704M ... J PACKAGE
TLC3704I ... D, J, OR N PACKAGE
TLC3704C ... D, J, OR N PACKAGE
(TOP VIEW)



TLC3704M ... FK PACKAGE
(TOP VIEW)

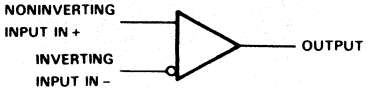


NC – No internal connection

description

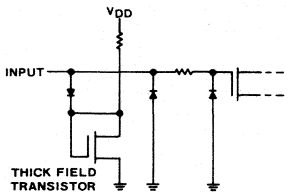
The TLC3704 consists of four independent differential-voltage comparators designed to operate from a single supply and be compatible with modern HCMOS logic systems. It is functionally similar to the LM339 but uses 1/20th the power for similar response times. The push-pull CMOS output stage will drive capacitive loads directly without a power-consuming pull-up resistor to achieve the stated response time. Eliminating the pull-up resistor not only reduces power dissipation, but also saves board space and component cost. The output stage is also fully compatible with TTL requirements.

symbol (each comparator)

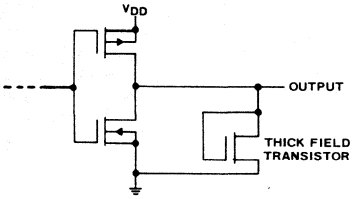


schematics of inputs and outputs

EQUIVALENT OF EACH INPUT



TYPICAL OF ALL OUTPUTS



LinCMOS is a trademark of Texas Instruments

TEXAS INSTRUMENTS

Texas Instruments LinCMOS process offers superior analog performance to standard CMOS processes. Along with the standard CMOS advantages of low power without sacrificing speed, high input impedance, and low bias currents, the LinCMOS process offers extremely stable input offset voltages, even with differential input stresses of several volts. This characteristic makes it possible to build reliable CMOS comparators.

The TLC3704M is characterized for operation over the full military temperature range of -55°C to 125°C. The TLC3704I is characterized for operation over the extended industrial temperature range of -40°C to 85°C. The TLC3704C is characterized for operation over the commercial temperature range of 0°C to 70°C.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{DD} (see Note 1) . . . . . -0.3 V to 18 V
Differential input voltage (see Note 2) . . . . . ±18 V
Input voltage, V_I . . . . . -0.3 V to V_{DD}
Output voltage, V_O . . . . . -0.3 V to V_{DD}
Input current, I_I . . . . . ±5 mA
Output current, I_O (each output) . . . . . ±20 mA
Total supply current into V_{DD} terminal . . . . . 40 mA
Total current out of ground terminal . . . . . 60 mA
Continuous total dissipation at (or below) 25°C free-air temperature (see Note 3):
D package . . . . . 950 mW
FK or J package (alloy mount) . . . . . 1375 mW
J package (glass mount) . . . . . 1025 mW
N package . . . . . 875 mW
Operating free-air temperature range: TLC3704M . . . . . -55°C to 125°C
TLC3704I . . . . . -40°C to 85°C
TLC3704C . . . . . 0°C to 70°C
Storage temperature range . . . . . -65°C to 150°C
Lead temperature 1.6 mm (1/16 inch) from case for 60 seconds: FK or J package . . . . . 300°C
Lead temperature 1.6 mm (1/16 inch) from case for 10 seconds: D or N package . . . . . 260°C

NOTES: 1. All voltage values, except differential voltages, are with respect to network ground.
2. Differential voltages are at the noninverting input with respect to the inverting input.
3. For operation above 25°C free-air temperature, refer to the Dissipation Derating Table. For TLC3704M in the J package, use the alloy mount derating factor; for TLC3704I and TLC3704C in the J package, use the glass mount derating factor.

DISSIPATION DERATING TABLE

PACKAGE	POWER RATING	DERATING FACTOR	ABOVE T_A
D	950 mW	7.6 mW/°C	25°C
FK	1375 mW	11 mW/°C	25°C
J (alloy mount)	1375 mW	11 mW/°C	25°C
J (glass mount)	1025 mW	6.6 mW/°C	25°C
N	875 mW	7 mW/°C	25°C

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage, V_{DD}	4	5	16	V
Common-mode input voltage, V_{IC}	-0.2		V_{DD}-1.5	V
High-level output current, I_{OH}		-8	-20	mA
Low-level output current, I_{OL}		8	20	mA
Operating free-air temperature, T_A	-55		125	°C

electrical characteristics at specified operating free-air temperature, V_{DD} = 5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS †		MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage	V_{IC} = V_{ICR}min, V_{DD} = 5 V to 10 V, See Note 4	25°C		1.2	5	mV
			Full range			10	
I_{IO}	Input offset current	V_{IC} = 2.5 V	25°C		1		pA
			125°C			15	nA
I_{IB}	Input bias current	V_{IC} = 2.5 V	25°C		5		pA
			125°C			30	nA
V_{ICR}	Common-mode input voltage range		25°C	0 to V_{DD}-1			V
			Full range	0 to V_{DD}-1.5			
CMRR	Common-mode rejection ratio	V_{IC} = V_{ICR}min	25°C		84		dB
			125°C		83		
			-55°C		82		
k_{SVR}	Supply voltage rejection ratio	V_{DD} = 5 V to 10 V	25°C		85		dB
			125°C		85		
			-55°C		82		
V_{OH}	High-level output voltage	V_{ID} = 1 V, I_{OH} = -4 mA	25°C	4.5	4.7		V
			125°C	4.2			
V_{OL}	Low-level output voltage	V_{ID} = -1 V, I_{OL} = 4 mA	25°C		210	300	mV
			125°C			500	
I_{DD}	Supply current (four comparators)	No load	25°C		35	80	μA
			Full range			175	

† All characteristics are measured with zero common-mode voltage unless otherwise noted. Full range is -55°C to 125°C for the TLC3704M.

NOTE 4: The offset voltage limits given are the maximum values required to drive the output up to 4.5 V or down to 0.3 V.

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage, V_{DD}	3	5	16	V
Common-mode input voltage, V_{IC}	-0.2		V_{DD}-1.5	V
High-level output current, I_{OH}		-8	-20	mA
Low-level output current, I_{OL}		8	20	mA
Operating free-air temperature, T_A	-40		85	°C

electrical characteristics at specified operating free-air temperature, V_{DD} = 5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS †		MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage	V_{IC} = V_{ICR}min, V_{DD} = 5 V to 10 V, See Note 4	25°C		1.2	5	mV
			Full range			7	
I_{IO}	Input offset current	V_{IC} = 2.5 V	25°C		1		pA
			85°C			1	nA
I_{IB}	Input bias current	V_{IC} = 2.5 V	25°C		5		pA
			85°C			2	nA
V_{ICR}	Common-mode input voltage range		25°C	0 to V_{DD}-1			V
			Full range	0 to V_{DD}-1.5			
CMRR	Common-mode rejection ratio	V_{IC} = V_{ICR}min	25°C		84		dB
			85°C		84		
			-40°C		83		
k_{SVR}	Supply voltage rejection ratio	V_{DD} = 5 V to 10 V	25°C		85		dB
			85°C		85		
			-40°C		83		
V_{OH}	High-level output voltage	V_{ID} = 1 V, I_{OH} = -4 mA	25°C	4.5	4.7		V
			85°C	4.3			
V_{OL}	Low-level output voltage	V_{ID} = -1 V, I_{OL} = 4 mA	25°C		210	300	mV
			85°C			400	
I_{DD}	Supply current (four comparators)	No load	25°C		35	80	μA
			Full range			125	

† All characteristics are measured with zero common-mode voltage unless otherwise noted. Full range is -40°C to 85°C for the TLC3704I.

NOTE 4: The offset voltage limits given are the maximum values required to drive the output up to 4.5 V or down to 0.3 V.

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage, V_{DD}	3	5	16	V
Common-mode input voltage, V_{IC}	-0.2		V_{DD}-1.5	V
High-level output current, I_{OH}		-8	-20	mA
Low-level output current, I_{OL}		8	20	mA
Operating free-air temperature, T_A	0		70	°C

electrical characteristics at specified operating free-air temperature, V_{DD} = 5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS †		MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage	V_{IC} = V_{ICR}min, V_{DD} = 5 V to 10 V, See Note 4	25°C		1.2	5	mV
			Full range			6.5	
I_{IO}	Input offset current	V_{IC} = 2.5 V	25°C		1		pA
			70°C			0.3	nA
I_{IB}	Input bias current	V_{IC} = 2.5 V	25°C		5		pA
			70°C			0.6	nA
V_{ICR}	Common-mode input voltage range		25°C	0 to V_{DD}-1			V
			Full range	0 to V_{DD}-1.5			
CMRR	Common-mode rejection ratio	V_{IC} = V_{ICR}min	25°C		84		dB
			70°C		84		
			0°C		84		
k_{SVR}	Supply voltage rejection ratio	V_{DD} = 5 V to 10 V	25°C		85		dB
			70°C		85		
			0°C		85		
V_{OH}	High-level output voltage	V_{ID} = 1 V, I_{OH} = -4 mA	25°C	4.5	4.7		V
			70°C	4.3			
V_{OL}	Low-level output voltage	V_{ID} = -1 V, I_{OL} = 4 mA	25°C		210	300	mV
			70°C			375	
I_{DD}	Supply current (four comparators)	No load	25°C		35	80	μA
			Full range			100	

† All characteristics are measured with zero common-mode voltage unless otherwise noted. Full range is 0°C to 70°C for the TLC3704C.

NOTE 4: The offset voltage limits given are the maximum values required to drive the output up to 4.5 V or down to 0.3 V.

switching charactistics, V_{DD} = 5 V, T_A = 25°C (see Figure 3)

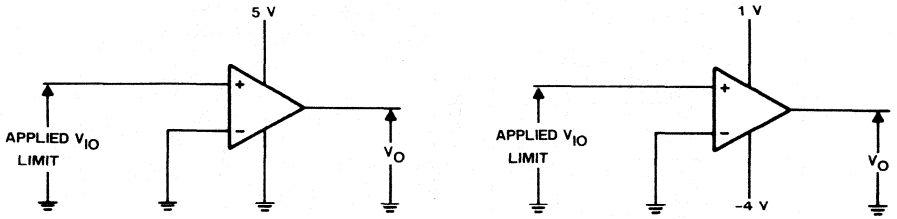
PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_{PHL}	Response time, high-to-low-level output	f = 10 kHz, C_L = 50 pF	Overdrive = 2 mV		4.0		µs
			Overdrive = 5 mV		2.3		
			Overdrive = 10 mV		1.5		
			Overdrive = 20 mV		0.95		
			Overdrive = 40 mV		0.65		
		V_I = 1.4 V step at IN+ pin			0.15		
t_{PLH}	Response time, low-to-high-level output	f = 10 kHz, C_L = 50 pF	Overdrive = 2 mV		4.5		µs
			Overdrive = 5 mV		2.7		
			Overdrive = 10 mV		1.9		
			Overdrive = 20 mV		1.4		
			Overdrive = 40 mV		1.0		
		V_I = 1.4 V step at IN+ pin			1.3		
t_{THL}	Transition time, high-to-low-level output	f = 10 kHz, C_L = 50 pF	Overdrive = 50 mV		50		ns
t_{TLH}	Transition time, low-to-high-level output	f = 10 kHz, C_L = 50 pF	Overdrive = 50 mV		125		ns

PARAMETER MEASUREMENT INFORMATION

The TLC3704 contains a digital output stage which, if held in the linear region of the transfer curve, can cause damage to the device. Conventional operational amplifier/comparator testing incorporates the use of a servo-loop which is designed to force the device output to a level within this linear region. Since the servo-loop method of testing cannot be used, we offer the following alternatives for measuring parameters such as input offset voltage, common-mode rejection, etc.

To verify that the input offset voltage falls within the limits specified, the limit value is applied to the input as shown in Figure 1a. With the noninverting input positive with respect to the inverting input, the output should be high. With the input polarity reversed, the output should be low.

A similar test can be made to verify the input offset voltage at the common-mode extremes. The supply voltages can be slewed as shown in Figure 1b for the V_{ICR} test, rather than changing the input voltages, to provide greater accuracy.



a. V_{IO} with V_{IC} = 0 V

b. V_{IO} with V_{IC} = 4 V

FIGURE 1. METHOD FOR VERIFYING THAT INPUT OFFSET VOLTAGE IS WITHIN SPECIFIED LIMITS

A close approximation of the input offset voltage can be obtained by using a binary search method to vary the differential input voltage while monitoring the output state. When the applied input voltage differential is equal, but opposite in polarity, to the input offset voltage, the output will change states.

PARAMETER MEASUREMENT INFORMATION

Figure 2 illustrates a practical circuit for direct d.c. measurement of input offset voltage that does not bias the comparator into the linear region. The circuit consists of a switching mode servo loop in which IC1a generates a triangular waveform of approximately 20 mV amplitude. IC1b acts as a buffer, with C2 and R4 removing any residual d.c. offset. The signal is then applied to the inverting input of the comparator under test, while the noninverting input is driven by the output of the integrator formed by IC1c through the voltage divider formed by R8 and R9. The loop reaches a stable operating point when the output of the comparator under test has a duty cycle of exactly 50%, which can only occur when the incoming triangle wave is "sliced" symmetrically or when the voltage at the noninverting input exactly equals the input offset voltage.

Voltage divider R8 and R9 provides a step-up of the input offset voltage by a factor of 100 to make measurement easier. The values of R5, R7, R8, and R9 can significantly influence the accuracy of the reading; therefore, it is suggested that their tolerance level be one percent or lower.

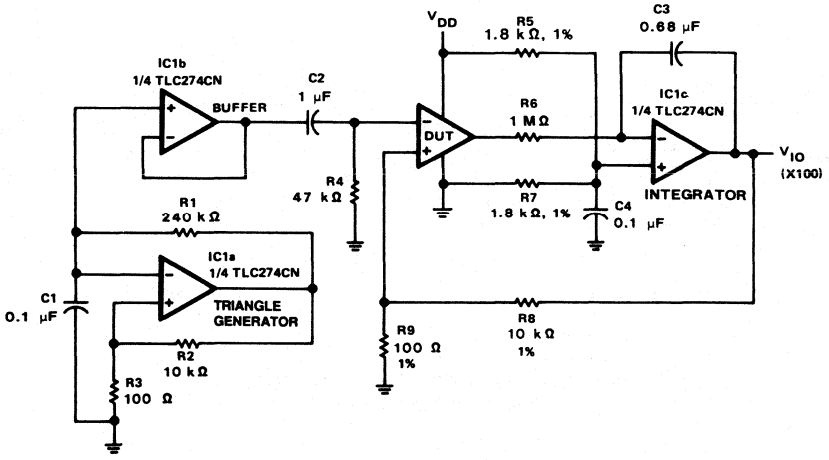


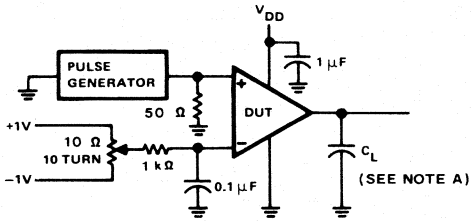
FIGURE 2. CIRCUIT FOR INPUT OFFSET VOLTAGE MEASUREMENT

Measuring the extremely low values of input current requires isolation from all other sources of leakage current and compensation for the leakage of the test socket and board. With a good picoammeter, the socket and board leakage can be measured with no device in the socket. Subsequently, this open socket leakage value can be subtracted from the measurement obtained with a device in the socket to obtain the actual input current of the device.

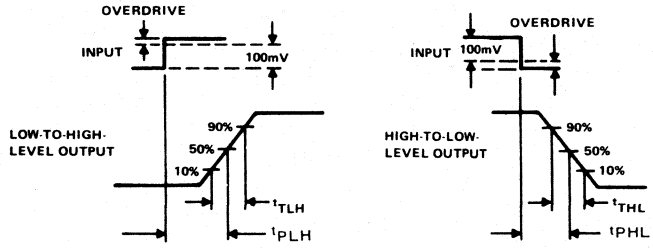
PARAMETER MEASUREMENT INFORMATION

Response time is defined as the interval between the application of an input step function and the instant when the output reaches 50% of its maximum value. Response time, low-to-high-level output is measured from the leading edge of the input pulse, while response time, high-to-low-level output, is measured from the trailing edge of the input pulse. Response time measurement at low input signal levels can be greatly affected by the input offset voltage. The offset voltage should be balanced by the adjustment at the inverting input (as shown in Figure 3) so that the circuit is just at the transition point. Then a low signal, for example 105 mV or 5 mV overdrive, will cause the output to change state.

Rise time is defined as the time required for the output to change from 10% to 90% of its final value. Similarly, fall time is defined as the time required for the output voltage to change from 90% to 10% of its final value (see Figure 3).



TEST CIRCUIT



VOLTAGE WAVEFORMS

NOTE A: C_L includes probe and jig capacitance.

FIGURE 3. RESPONSE, RISE, AND FALL TIMES
CIRCUIT AND VOLTAGE WAVEFORMS

TYPICAL CHARACTERISTICS

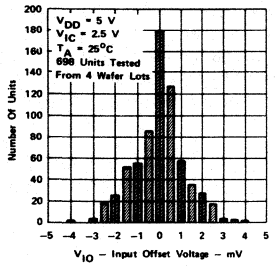


FIGURE 4

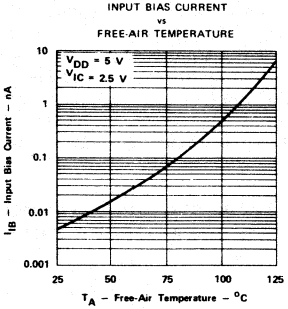


FIGURE 5

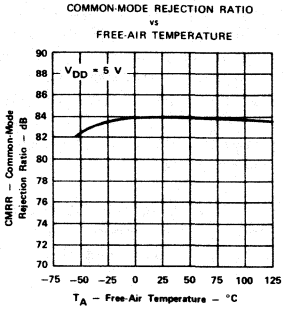


FIGURE 6

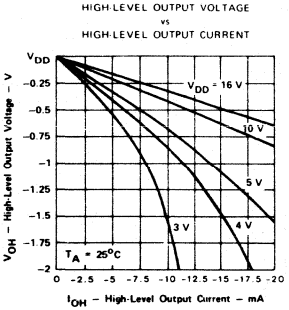


FIGURE 7

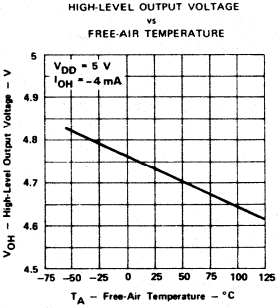


FIGURE 8

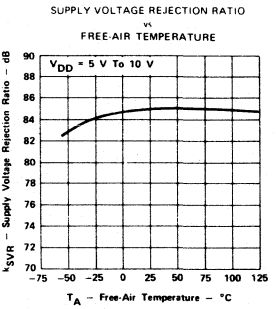


FIGURE 9

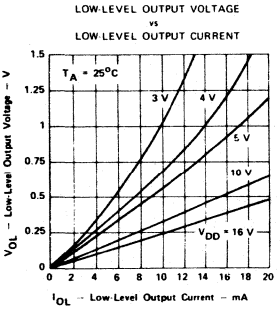


FIGURE 10

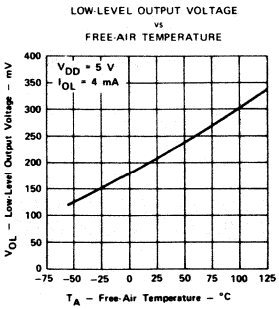


FIGURE 11

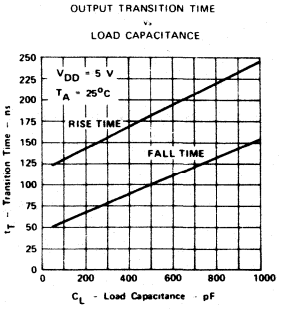


FIGURE 12

TYPICAL CHARACTERISTICS

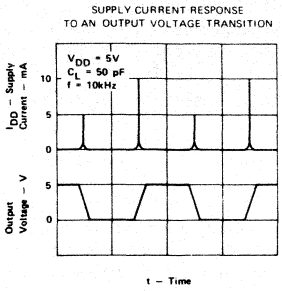


FIGURE 13

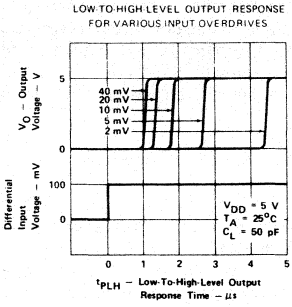


FIGURE 14

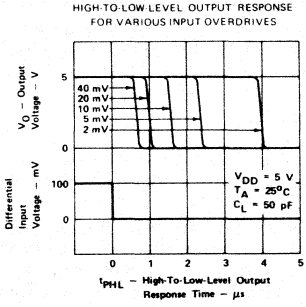


FIGURE 15

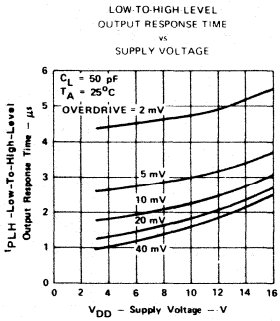


FIGURE 16

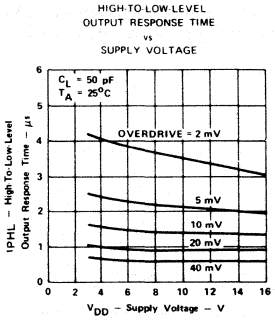


FIGURE 17

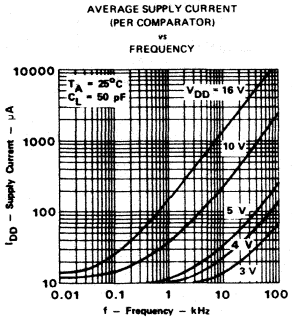


FIGURE 18

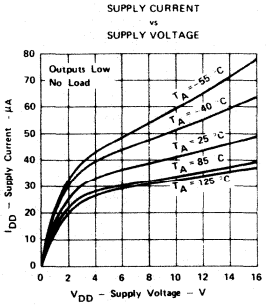


FIGURE 19

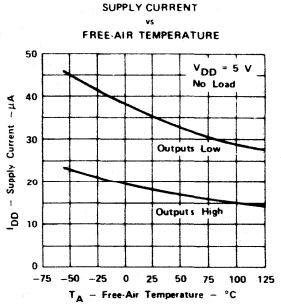


FIGURE 20

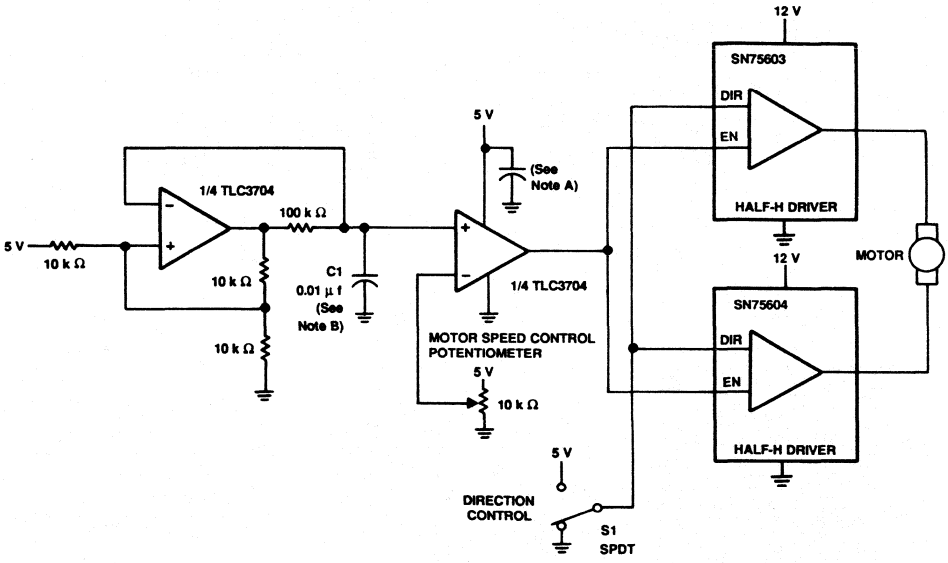
TYPICAL APPLICATION DATA

The inputs should always remain within the supply rails in order to avoid forward biasing the diodes in the electrostatic discharge (ESD) protection structure. If either input exceeds this range, the device will not be damaged as long as the input current is limited to less than 5 milliamperes. To maintain the expected output state, the inputs must remain within the common-mode range. For example, at 25°C with V_{DD} = 5 V, both inputs must remain between -0.2 V and 4 V to assure proper device operation.

To assure reliable operation, the supply should be decoupled with a capacitor (0.1 μF) positioned as close to the device as possible.

Be careful to note the output and supply current limitations since the TLC3704 does not provide current protection. For example, each output can source or sink a maximum of 20 milliamperes; however, the total current to ground can only be an absolute maximum of 60 milliamperes. This prohibits sinking 20 milliamperes from each of the four outputs simultaneously since the total current to ground would be 80 milliamperes.

The TLC3704 has internal ESD protection circuits that will prevent functional failures at voltages up to 2000 volts as tested under MIL-STD-883C, Method 3015.2; however, care should be exercised in handling these devices as exposure to ESD may result in the degradation of the device parametric performance.

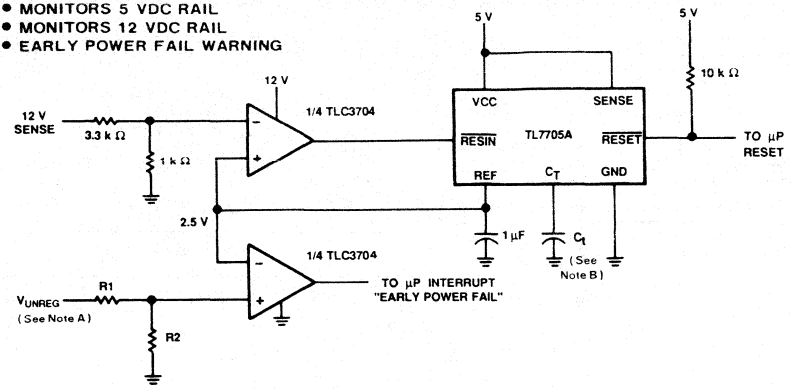


NOTES: A. The recommended minimum capacitance is 10 μF to eliminate common ground switching noise.
B. Adjust C1 for change in oscillator frequency.

FIGURE 21. PULSE-WIDTH-MODULATED MOTOR SPEED CONTROLLER

TYPICAL APPLICATION DATA

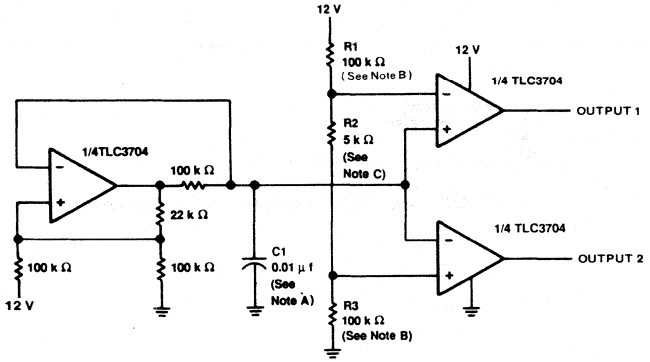
- MONITORS 5 VDC RAIL
- MONITORS 12 VDC RAIL
- EARLY POWER FAIL WARNING

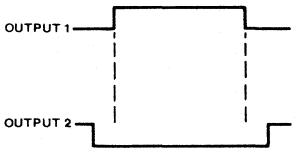


NOTES: A. $V_{UNREG} = 2.5(\frac{R1+R2}{R2})$

B. The value of C_t determines the time delay of reset.

FIGURE 22. ENHANCED SUPPLY SUPERVISOR





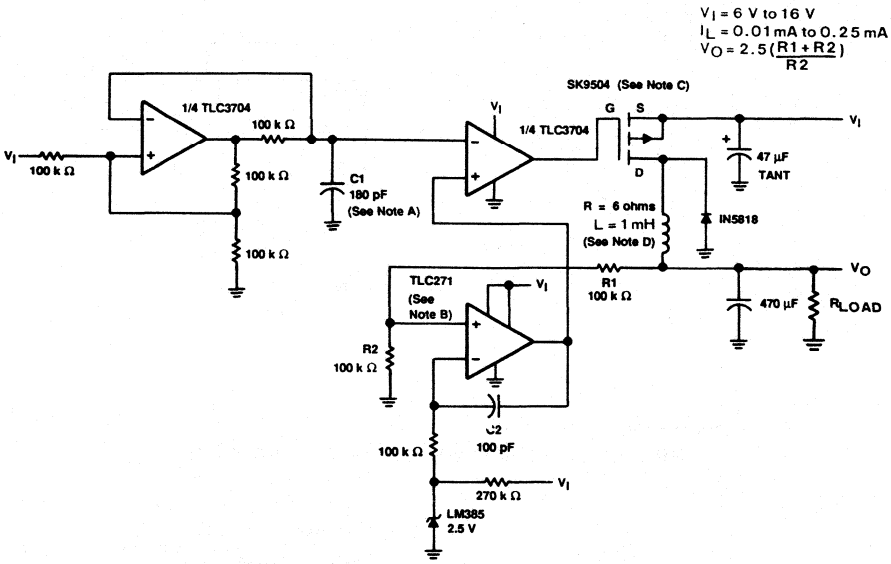
NOTES: A. Adjust C1 for a change in oscillator frequency where:
$1/f = 1.85(100\,k\Omega)C1$

B. Adjust R1 and R3 to change duty cycle

C. Adjust R2 to change deadtime

FIGURE 23. TWO-PHASE NONOVERLAPPING CLOCK GENERATOR

TYPICAL APPLICATION DATA



NOTES: A. Adjust C1 for a change in oscillator frequency
B. TLC271 — Tie pin 8 to pin 7 for low bias operation
C. SK9504 — VDS = 40 V
IDS = 1 A
D. To achieve microampere current drive, the inductance of the circuit must be increased.

FIGURE 24. MICROPOWER SWITCHING REGULATOR

General Information 1

Operational Amplifiers 2

Voltage Comparators 3

Timers 4

Analog to Digital Converters 5

Digital to Analog Converters 6

Analog Switches 7

Switched Capacitor Filters 8

Packaging Information 9

TIMERS

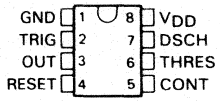
	SUPPLY CURRENT (μA)	POWER DISSIPATION (mW)	SUPPLY RANGE (V)		MAX FREQUENCY (MHZ)	MAX TIMING PERIOD	MAX TIMING ERROR	OUTPUT CURRENT (mA)	PAGE No.
			Min	Max					
Single									
TLC551	350	1	1	18	2.1	Hours	3%	+10/–100	4-5
TLC555	350	1	2(3)*	18	2.1	Hours	3%	+10/–100	4-21
Dual									
TLC552	1000	2	1	18	2.1	Hours	3%	+ 10/–100	4-13
TLC556	1000	2	2(3)*	18	2.1	Hours	3%	+ 10/–100	4-27

**Indicates for industrial Temp Range*

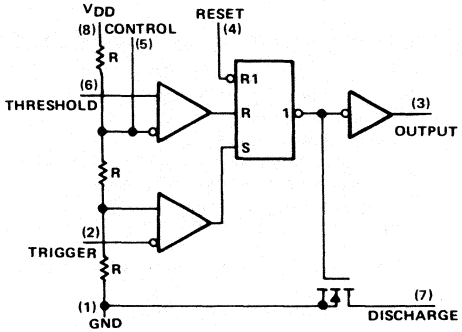
D2791, FEBRUARY 1984—REVISED OCTOBER 1985

- **Very Low Power Consumption . . . 1 mW Typ at V_{DD} = 5 V**
- **Capable of Operation in Astable Mode**
- **CMOS Output Capable of Swinging Rail to Rail**
- **High Output-Current Capability**
  . . . Sink 100 mA Typ
  . . . Source 10 mA Typ
- **Output Fully Compatible with CMOS, TTL, and MOS**
- **Low Supply Current Reduces Spikes During Output Transitions**
- **High-Impedance Inputs . . . 10^{12} Ω Typ**
- **Single-Supply Operation from 1 V to 18 V**
- **Functionally Interchangeable with the NE555; Has Same Pinout**

D OR P DUAL-IN-LINE PACKAGE
(TOP VIEW)



functional block diagram



Reset can override Trigger, which can override Threshold.

description

The TLC551 is a monolithic timing circuit fabricated using TI's LinCMOS™ process, which provides full compatibility with CMOS, TTL, and MOS logic and operation at frequencies up to 2 MHz. Accurate time delays and oscillations are possible with smaller, less-expensive timing capacitors than the NE555 because of the high input impedance. Power consumption is low across the full range of power supply voltages.

Like the NE555, the TLC551 has a trigger level approximately one-third of the supply voltage and a threshold level approximately two-thirds of the supply voltage. These levels can be altered by use of the control voltage terminal. When the trigger input falls below the trigger level, the flip-flop is set and the output goes high. If the trigger input is above the trigger level and the threshold input is above the threshold level, the flip-flop is reset and the output is low. The reset input can override all other inputs and can be used to initiate a new timing cycle. If the reset input is low, the flip-flop is reset and the output is low. Whenever the output is low, a low-impedance path is provided between the discharge terminal and ground.

While the complementary CMOS output is capable of sinking over 100 milliamperes and sourcing over 10 milliamperes, the TLC551 exhibits greatly reduced supply-current spikes during output transitions. This minimizes the need for the large decoupling capacitors required by the NE555.

These devices have internal electrostatic discharge (ESD) protection circuits that will prevent catastrophic failures at voltages up to 2000 volts as tested under MIL-STD-883C, Method 3015.2. However, care should be exercised in handling these devices as exposure to ESD may result in a degradation of the device parametric performance.

All unused inputs should be tied to an appropriate logic level to prevent false triggering.

The TLC551C is characterized for operation from 0°C to 70°C.

LinCMOS is a trademark of Texas Instruments.

FUNCTION TABLE

RESET VOLTAGE†	TRIGGER VOLTAGE†	THRESHOLD VOLTAGE†	OUTPUT	DISCHARGE SWITCH
<MIN	Irrelevant	Irrelevant	Low	On
>MAX	<MIN	Irrelevant	High	Off
>MAX	>MAX	>MAX	Low	On
>MAX	>MAX	<MIN	As previously established	

†For conditions shown as MIN or MAX, use the appropriate value specified under electrical characteristics.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{DD} (see Note 1) . . . . . 18 V
Input voltage range (any input) . . . . . −0.3 V to V_{DD}
Sink current, discharge or output . . . . . 150 mA
Source current, output . . . . . 15 mA
Continuous total dissipation at (or below) 25°C free-air temperature . . . . . 460 mW
Operating free-air temperature range . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: D or P package . . . . . 260°C

NOTE 1: All voltage values are with respect to network ground terminal.

recommended operating conditions

	MIN	MAX	UNIT
Supply voltage, V_{DD}	1	18	V
Operating free air temperature, T_A	0	70	°C

electrical characteristics at specified free-air temperature, V_{DD} = 1 V

PARAMETER	TEST CONDITIONS†		MIN	TYP	MAX	UNIT
Threshold voltage level		25°C	0.475	0.67	0.85	V
		Full range	0.45		0.875	
Threshold current		25°C		10		pA
		MAX		75		
Trigger voltage level		25°C	0.15	0.33	0.425	V
		Full range	0.1		0.45	
Trigger current		25°C		10		pA
		MAX		75		
Reset voltage level		25°C	0.4	0.7	1	V
		Full range	0.3		1	
Reset current		25°C		10		pA
		MAX		75		
Control voltage (open-circuit) as a percentage of supply voltage		MAX		66.7%		
Discharge switch on-state voltage	I_{OL} = 100 μA	25°C		0.02	0.15	V
		Full range			0.2	
Discharge switch off-state current		25°C		0.1		nA
		MAX		0.5		
Low-level output voltage	I_{OL} = 100 μA	25°C		0.03	0.2	V
		Full range			0.25	
High-level output voltage	I_{OH} = −10 μA	25°C	0.6	0.98		V
		Full range	0.6			
Supply current		25°C		15	100	μA
		Full range			150	

†Full range (MIN to MAX) is 0°C to 70°C.

electrical characteristics at specified free-air temperature, V_{DD} = 2 V

PARAMETER	TEST CONDITIONS†		MIN	TYP	MAX	UNIT
Threshold voltage level		25°C	0.95	1.33	1.65	V
		Full range	0.85		1.75	
Threshold current		25°C		10		pA
		MAX		75		
Trigger voltage level		25°C	0.4	0.67	0.95	V
		Full range	0.3		1.05	
Trigger current		25°C		10		pA
		MAX		75		
Reset voltage level		25°C	0.4	1.1	1.5	V
		Full range	0.3		1.8	
Reset current		25°C		10		pA
		MAX		75		
Control voltage (open-circuit) as a percentage of supply voltage		MAX		66.7%		
Discharge switch on-state voltage	I_{OL} = 1 mA	25°C		0.03	0.2	V
		Full range			0.25	
Discharge switch off-state current		25°C		0.1		nA
		MAX		0.5		
Low-level output voltage	I_{OL} = 1 mA	25°C		0.07	0.3	V
		Full range			0.35	
High-level output voltage	I_{OH} = −300 μA	25°C	1.5	1.9		V
		Full range	1.5			
Supply current		25°C		65	250	μA
		Full range			400	

†Full range (MIN to MAX) is 0°C to 70°C.

electrical characteristics at specified free-air temperature, V_{DD} = 5 V

PARAMETER	TEST CONDITIONS†		MIN	TYP	MAX	UNIT
Threshold voltage level		25°C	2.8	3.3	3.8	V
		Full range	2.7		3.9	
Threshold current		25°C		10		pA
		MAX		75		
Trigger voltage level		25°C	1.36	1.66	1.96	V
		Full range	1.26		2.06	
Trigger current		25°C		10		pA
		MAX		75		
Reset voltage level		25°C	0.4	1.1	1.5	V
		Full range	0.3		1.8	
Reset current		25°C		10		pA
		MAX		75		
Control voltage (open-circuit) as a percentage of supply voltage		MAX		66.7%		
Discharge switch on-state voltage	I_{OL} = 10 mA	25°C		0.14	0.5	V
		Full range			0.6	
Discharge switch off-state current		25°C		0.1		nA
		MAX		0.5		
Low-level output voltage	I_{OL} = 8 mA	25°C		0.21	0.4	V
		Full range			0.5	
	I_{OL} = 5 mA	25°C		0.13	0.3	
		Full range			0.4	
	I_{OL} = 3.2 mA	25°C		0.08	0.3	
		Full range			0.35	
High-level output voltage	I_{OH} = −1 mA	25°C	4.1	4.8		V
		Full range	4.1			
Supply current		25°C		170	350	μA
		Full range			500	

†Full range (MIN to MAX) is 0°C to 70°C.

electrical characteristics at specified free-air temperature, V_{DD} = 15 V

PARAMETER	TEST CONDITIONS†		MIN	TYP	MAX	UNIT
Threshold voltage level		25°C	9.45	10	10.55	V
		Full range	9.35		10.65	
Threshold current		25°C		10		pA
		MAX		75		
Trigger voltage level		25°C	4.65	5	5.35	V
		Full range	4.55		5.45	
Trigger current		25°C		10		pA
		MAX		75		
Reset voltage level		25°C	0.4	1.1	1.5	V
		Full range	0.3		1.8	
Reset current		25°C		10		pA
		MAX		75		
Control voltage (open-circuit) as a percentage of supply voltage		MAX		66.7%		
Discharge switch on-state voltage	I_{OL} = 100 mA	25°C		0.77	1.7	V
		Full range			1.8	
Discharge switch off-state current		25°C		0.1		nA
		MAX		0.5		
Low-level output voltage	I_{OL} = 100 mA	25°C		1.28	3.2	V
		Full range			3.6	
	I_{OL} = 50 mA	25°C		0.63	1	
		Full range			1.3	
	I_{OL} = 10 mA	25°C		0.12	0.3	
		Full range			0.4	
High-level output voltage	I_{OH} = −10 mA	25°C	12.5	14.2		V
		Full range	12.5			
	I_{OH} = −5 mA	25°C	13.5	14.6		
		Full range	13.5			
	I_{OH} = −1 mA	25°C	14.2	14.9		
		Full range	14.2			
Supply current		25°C		360	600	μA
		Full range			800	

†Full range (MIN to MAX) is 0°C to 70°C.

electrical characteristics at specified free-air temperature, V_{DD} = 18 V

PARAMETER	TEST CONDITIONS†		MIN	TYP	MAX	UNIT
Threshold voltage level		25°C	11.4	12	12.6	V
		Full range	10.9		12.7	
Threshold current		25°C		10		pA
		MAX		75		
Trigger voltage level		25°C	5.6	6	6.4	V
		Full range	5.5		6.5	
Trigger current		25°C		10		pA
		MAX		75		
Reset voltage level		25°C	0.4	1.1	1.5	V
		Full range	0.3		1.8	
Reset current		25°C		10		pA
		MAX		75		
Control voltage (open-circuit) as a percentage of supply voltage		MAX		66.7%		
Discharge switch on-state voltage	I_{OL} = 100 mA	25°C		0.72	1.5	V
		Full range			1.6	
Discharge switch off-state current		25°C		0.1		nA
		MAX		0.5		
Low-level output voltage	I_{OL} = 3.2 mA	25°C		0.04	0.3	V
		Full range			0.35	
High-level output voltage	I_{OH} = −1 mA	25°C	17.3	17.9		V
		Full range	17.3			
Supply current		25°C		420	600	μA
		Full range			800	

†Full range (MIN to MAX) is 0°C to 70°C.

operating characteristics, V_{DD} = 5 V, T_A = 25°C (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Initial error of timing interval	V_{DD} = 5 V to 15 V,		1%	3%	
Supply voltage sensitivity of timing interval	$R_A = R_B$ = 1 kΩ to 100 kΩ, C_T = 0.1 μF, See Note 2		0.1	0.5	%/V
Output pulse rise time	R_L = 10 MΩ, C_L = 10 pF		20	75	ns
Output pulse fall time			15	60	
Maximum frequency in astable mode	R_A = 470 Ω, R_B = 200 Ω, C_T = 200 pF, See Note 2	1.2	1.8		MHz

NOTE 2: R_A, R_B, and C_T are as defined in Figure 1.

TYPICAL APPLICATION DATA

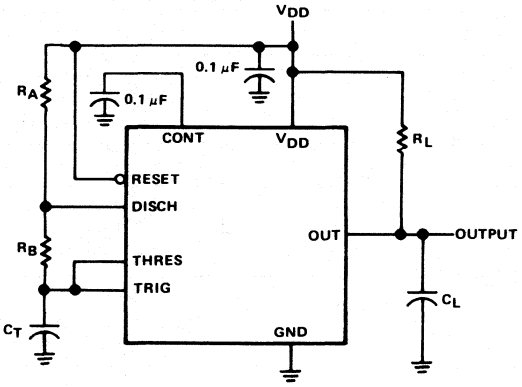


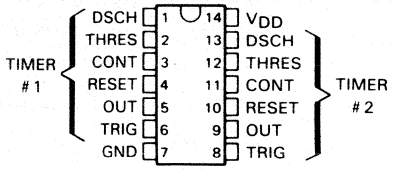
FIGURE 1. CIRCUIT FOR ASTABLE OPERATION

TLC552C
DUAL LinCMOS™ TIMER

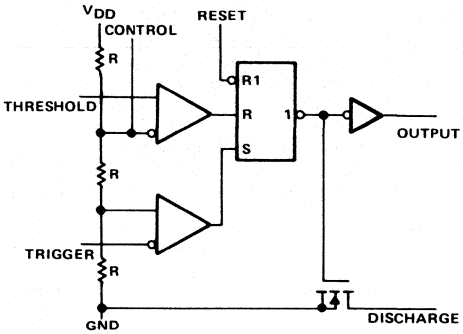
D2796, FEBRUARY 1984—REVISED OCTOBER 1985

- **Very Low Power Consumption . . . 2 mW Typ at V_{DD} = 5 V**
- **Capable of Operation in Astable Mode**
- **CMOS Output Capable of Swinging Rail to Rail**
- **High Output-Current Capability**
  . . . Sink 100 mA Typ
  . . . Source 10 mA Typ
- **Output Fully Compatible with CMOS, TTL, and MOS**
- **Low Supply Current Reduces Spikes During Output Transitions**
- **High-Impedance Inputs . . . 10^{12} Ω Typ**
- **Single-Supply Operation from 1 V to 18 V**
- **Functionally Interchangeable with the NE556; Has Same Pinout**

D OR P DUAL-IN-LINE PACKAGE
(TOP VIEW)



functional block diagram (each timer)



Reset can override Trigger and Threshold.
Trigger can override Threshold.

description

The TLC552 is a monolithic timing circuit fabricated using TI's LinCMOS™ process, which provides full compatibility with CMOS, TTL, and MOS logic and operation at frequencies up to 2 MHz. Accurate time delays and oscillations are possible with smaller, less-expensive timing capacitors than the NE555 because of the high input impedance. Power consumption is low across the full range of power supply voltages.

Like the NE556, the TLC552 has a trigger level approximately one-third of the supply voltage and a threshold level approximately two-thirds of the supply voltage. These levels can be altered by use of the control voltage terminal. When the trigger input falls below the trigger level, the flip-flop is set and the output goes high. If the trigger input is above the trigger level and the threshold input is above the threshold level, the flip-flop is reset and the output is low. The reset input can override all other inputs and can be used to initiate a new timing cycle. If the reset input is low, the flip-flop is reset and the output is low. Whenever the output is low, a low-impedance path is provided between the discharge terminal and ground.

While the complementary CMOS output is capable of sinking over 100 milliamperes and sourcing over 10 milliamperes, the TLC552 exhibits greatly reduced supply-current spikes during output transitions. This minimizes the need for the large decoupling capacitors required by the NE556.

These devices have internal electrostatic discharge (ESD) protection circuits that will prevent catastrophic failures at voltages up to 2000 volts as tested under MIL-STD-883C, Method 3015.2. However, care should be exercised in handling these devices as exposure to ESD may result in a degradation of the device parametric performance.

All unused inputs should be tied to an appropriate logic level to prevent false triggering.

The TLC552C is characterized for operation from 0°C to 70°C.

LinCMOS is a trademark of Texas Instruments.

FUNCTION TABLE

RESET VOLTAGE†	TRIGGER VOLTAGE†	THRESHOLD VOLTAGE†	OUTPUT	DISCHARGE SWITCH
<MIN	Irrelevant	Irrelevant	Low	On
>MAX	<MIN	Irrelevant	High	Off
>MAX	>MAX	>MAX	Low	On
>MAX	>MAX	<MIN	As previously established	

†For conditions shown as MIN or MAX, use the appropriate value specified under electrical characteristics.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{DD} (see Note 1) . . . . . 18 V
Input voltage range (any input) . . . . . −0.3 V to V_{DD}
Sink current, discharge or output . . . . . 150 mA
Source current, output . . . . . 15 mA
Continuous total dissipation at (or below) 25°C free-air temperature (see Note 2)
D package . . . . . 950 mW
N package . . . . . 875 mW
Operating free-air temperature range . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: D or N package . . . . . 260°C

NOTES: 1. All voltage values are with respect to network ground terminal.
2. For operation of the above 25°C free-air temperature, see Dissipation Derating Table.

DISSIPATION DERATING TABLE

PACKAGE	POWER RATING	DERATING FACTOR	ABOVE T_A
D	950 mW	7.6 mW/°C	25°C
N	875 mW	7.0 mW/°C	25°C

recommended operating conditions

	MIN	MAX	UNIT
Supply voltage, V_{DD}	1	18	V
Operating free-air temperature, T_A	0	70	°C

electrical characteristics at specified free-air temperature, V_{DD} = 1 V

PARAMETER	TEST CONDITIONS†		MIN	TYP	MAX	UNIT
Threshold voltage level		25°C	0.475	0.67	0.85	V
		Full range	0.45		0.875	
Threshold current		25°C		10		pA
		MAX		75		
Trigger voltage level		25°C	0.15	0.33	0.425	V
		Full range	0.1		1.45	
Trigger current		25°C		10		pA
		MAX		75		
Reset voltage level		25°C	0.4	0.7	1	V
		Full range	0.3		1	
Reset current		25°C		10		pA
		MAX		75		
Control voltage (open-circuit) as a percentage of supply voltage		MAX		66.7%		
Discharge switch on-state voltage	I_{OL} = 100 μA	25°C		0.02	0.15	V
		Full range			0.2	
Discharge switch off-state current		25°C		0.1		nA
		MAX		0.5		
Low-level output voltage	I_{OL} = 100 μA	25°C		0.03	0.2	V
		Full range			0.25	
High-level output voltage	I_{OH} = −10 μA	25°C	0.6	0.98		V
		Full range	0.6			
Supply current		25°C		30	200	μA
		Full range			300	

† Full range (MIN to MAX) is 0°C to 70°C.

electrical characteristics at specified free-air temperature, V_{DD} = 2 V

PARAMETER	TEST CONDITIONS†		MIN	TYP	MAX	UNIT
Threshold voltage level		25°C	0.95	1.33	1.65	V
		Full range	0.85		1.75	
Threshold current		25°C		10		pA
		MAX		75		
Trigger voltage level		25°C	0.4	0.67	0.95	V
		Full range	0.3		1.05	
Trigger current		25°C		10		pA
		MAX		75		
Reset voltage level		25°C	0.4	1.1	1.5	V
		Full range	0.3		1.8	
Reset current		25°C		10		pA
		MAX		75		
Control voltage (open-circuit) as a percentage of supply voltage		MAX		66.7%		
Discharge switch on-state voltage	I_{OL} = 1 mA	25°C		0.03	0.2	V
		Full range			0.25	
Discharge switch off-state current		25°C		0.1		nA
		MAX		0.5		
Low-level output voltage	I_{OL} = 1 mA	25°C		0.07	0.3	V
		Full range			0.35	
High-level output voltage	I_{OH} = −300 μA	25°C	1.5	1.9		V
		Full range	1.5			
Supply current		25°C		130	500	μA
		Full range			800	

† Full range (MIN to MAX) is 0°C to 70°C.

electrical characteristics at specified free-air temperature, V_{DD} = 5 V

PARAMETER	TEST CONDITIONS†		MIN	TYP	MAX	UNIT
Threshold voltage level		25°C	2.8	3.3	3.8	V
		Full range	2.7		3.9	
Threshold current		25°C		10		pA
		MAX		75		
Trigger voltage level		25°C	1.36	1.66	1.96	V
		Full range	1.26		2.06	
Trigger current		25°C		10		pA
		MAX		75		
Reset voltage level		25°C	0.4	1.1	1.5	V
		Full range	0.3		1.8	
Reset current		25°C		10		pA
		MAX		75		
Control voltage (open-circuit) as a percentage of supply voltage		MAX		66.7%		
Discharge switch on-state voltage	I_{OL} = 10 mA	25°C		0.14	0.5	V
		Full range			0.6	
Discharge switch off-state current		25°C		0.1		nA
		MAX		0.5		
Low-level output voltage	I_{OL} = 8 mA	25°C		0.21	0.4	V
		Full range			0.5	
	I_{OL} = 5 mA	25°C		0.13	0.3	
		Full range			0.4	
	I_{OL} = 3.2 mA	25°C		0.08	0.3	
		Full range			0.35	
High-level output voltage	I_{OH} = −1 mA	25°C	4.1	4.8		V
		Full range	4.1			
Supply current		25°C		340	700	μA
		Full range			1000	

† Full range (MIN to MAX) is 0°C to 70°C.

electrical characteristics at specified free-air temperature, V_{DD} = 15 V

PARAMETER	TEST CONDITIONS†		MIN	TYP	MAX	UNIT
Threshold voltage level		25°C	9.45	10	10.55	V
		Full range	9.35		10.65	
Threshold current		25°C		10		pA
		MAX		75		
Trigger voltage level		25°C	4.65	5	5.35	V
		Full range	4.55		5.45	
Trigger current		25°C		10		pA
		MAX		75		
Reset voltage level		25°C	0.4	1.1	1.5	V
		Full range	0.3		1.8	
Reset current		25°C		10		pA
		MAX		75		
Control voltage (open-circuit) as a percentage of supply voltage		MAX		66.7%		
Discharge switch on-state voltage	I_{OL} = 100 mA	25°C		0.77	1.7	V
		Full range			1.8	
Discharge switch off-state current		25°C		0.1		nA
		MAX		0.5		
Low-level output voltage	I_{OL} = 100 mA	25°C		1.28	3.2	V
		Full range			3.6	
	I_{OL} = 50 mA	25°C		0.63	1	
		Full range			1.3	
	I_{OL} = 10 mA	25°C		0.12	0.3	
		Full range			0.4	
High-level output voltage	I_{OH} = −10 mA	25°C	12.5	14.2		V
		Full range	12.5			
	I_{OH} = −5 mA	25°C	13.5	14.6		
		Full range	13.5			
	I_{OH} = −1 mA	25°C	14.2	14.9		
		Full range	14.2			
Supply current		25°C		0.72	1.2	mA
		Full range			1.6	

† Full range (MIN to MAX) is 0°C to 70°C.

electrical characteristics at specified free-air temperature, V_{DD} = 18 V

PARAMETER	TEST CONDITIONS†		MIN	TYP	MAX	UNIT
Threshold voltage level		25°C	11.4	12	12.6	V
		Full range	10.9		12.7	
Threshold current		25°C		10		pA
		MAX		75		
Trigger voltage level		25°C	5.6	6	6.4	V
		Full range	5.5		6.5	
Trigger current		25°C		10		pA
		MAX		75		
Reset voltage level		25°C	0.4	1.1	1.5	V
		Full range	0.3		1.8	
Reset current		25°C		10		pA
		MAX		75		
Control voltage (open-circuit) as a percentage of supply voltage		MAX		66.7%		
Discharge switch on-state voltage	I_{OL} = 100 mA	25°C		0.72	1.5	V
		Full range			1.6	
Discharge switch off-state current		25°C		0.1		nA
		MAX		0.5		
Low-level output voltage	I_{OL} = 3.2 mA	25°C		0.04	0.3	V
		Full range			0.35	
High-level output voltage	I_{OH} = −1 mA	25°C	17.3	17.9		V
		Full range	17.3			
Supply current		25°C		0.84	1.2	mA
		Full range			1.6	

† Full range (MIN to MAX) is 0°C to 70°C.

operating characteristics, V_{DD} = 5 V, T_A = 25°C (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Initial error of timing interval	V_{DD} = 5 V to 15 V,		1%	3%	
Supply voltage sensitivity of timing interval	$R_A = R_B$ = 1 kΩ to 100 kΩ, C_T = 0.1 μF, See Note 3		0.1	0.5	%/V
Output pulse rise time	R_L = 10 MΩ, C_L = 10 pF		20	75	ns
Output pulse fall time			15	60	
Maximum frequency in astable mode	R_A = 470 Ω, R_B = 200 Ω, C_T = 200 pF, See Note 3	1.2	2.8		MHz

NOTE 3: R_A, R_B, and C_T are as defined in Figure 1.

TYPICAL APPLICATION DATA

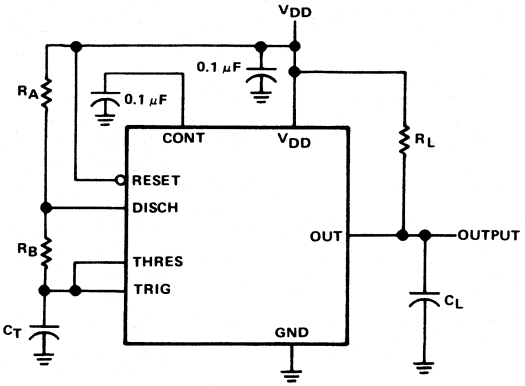
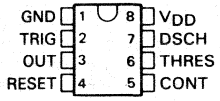


FIGURE 1. CIRCUIT FOR ASTABLE OPERATION

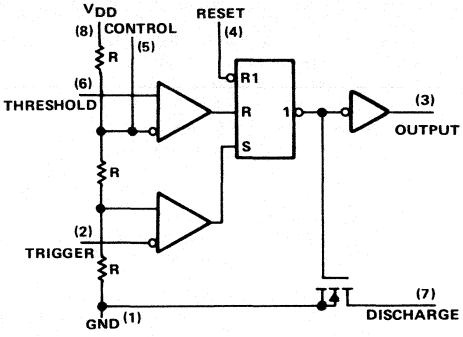
D2784, SEPTEMBER 1983 – REVISED MAY 1988

- **Very Low Power Consumption . . . 1 mW Typ at V_{DD} = 5 V**
- **Capable of Operation in Astable Mode**
- **CMOS Output Capable of Swinging Rail to Rail**
- **High Output-Current Capability**
  . . . Sink 100 mA Typ
  . . . Source 10 mA Typ
- **Output Fully Compatible with CMOS, TTL, and MOS**
- **Low Supply Current Reduces Spikes During Output Transitions**
- **High-Impedance Inputs . . . 10^{12} Ω Typ**
- **Single-Supply Operation from 2 V to 18 V (unless specified)**
- **Functionally Interchangeable with the NE555; Has Same Pinout**

TLC555M . . . JG PACKAGE
TLC555I, TLC555C . . . D or P PACKAGE
(TOP VIEW)



functional block diagram



Reset can override Trigger, which can override Threshold.

description

The TLC555 is a monolithic timing circuit fabricated using TI's LinCMOS™ process, which provides full compatibility with CMOS, TTL, and MOS logic and operation at frequencies up to 2 MHz. Accurate time delays and oscillations are possible with smaller, less-expensive timing capacitors than the NE555 because of the high input impedance. Power consumption is low across the full range of power supply voltage.

Like the NE555, the TLC555 has a trigger level approximately one-third of the supply voltage and a threshold level approximately two-thirds of the supply voltage. These levels can be altered by use of the control voltage terminal. When the trigger input falls below the trigger level, the flip-flop is set and the output goes high. If the trigger input is above the trigger level and the threshold input is above the threshold level, the flip-flop is reset and the output is low. The reset input can override all other inputs and can be used to initiate a new timing cycle. If the reset input is low, the flip-flop is reset and the output is low. Whenever the output is low, a low-impedance path is provided between the discharge terminal and ground.

While the complementary CMOS output is capable of sinking over 100 milliamperes and sourcing over 10 milliamperes, the TLC555 exhibits greatly reduced supply-current spikes during output transitions. This minimizes the need for the large decoupling capacitors required by the NE555.

These devices have internal electrostatic discharge (ESD) protection circuits that will prevent catastrophic failures at voltages up to 2000 volts as tested under MIL-STD-883B, Method 3015.1. However, care should be exercised in handling these devices as exposure to ESD may result in a degradation of the device parametric performance.

All unused inputs should be tied to an appropriate logic level to prevent false triggering.
The TLC555M is characterized for operation over the full military temperature range of –55°C to 125°C. The TLC555C is characterized for operation from 0°C to 70°C. The TLC555I is characterized for operation from –40°C to 85°C.

LinCMOS is a trademark of Texas Instruments.

FUNCTION TABLE

RESET VOLTAGE†	TRIGGER VOLTAGE†	THRESHOLD VOLTAGE†	OUTPUT	DISCHARGE SWITCH
<MIN	Irrelevant	Irrelevant	Low	On
>MAX	<MIN	Irrelevant	High	Off
>MAX	>MAX	>MAX	Low	On
>MAX	>MAX	<MIN	As previously established	

†For conditions shown as MIN or MAX, use the appropriate value specified under electrical characteristics.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{DD} (see Note 1) . . . . . 18 V
Input voltage range (any input) . . . . . −0.3 V to V_{DD}
Sink current, discharge or output . . . . . 150 mA
Source current, output . . . . . 15 mA
Continuous total dissipation (see Note 2) . . . . . 460 mW
Operating free-air temperature range: TLC555M . . . . . −55°C to 125°C
TLC555C . . . . . 0°C to 70°C
TLC555I . . . . . −40°C to 85°C
Storage temperature range . . . . . −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds: JG package . . . . . 300°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: D or P package . . . . . 260°C

NOTES: 1. All voltage values are with respect to network ground terminal.
2. For operation of the TLC555M above 95°C free-air temperature, derate linearly at the rate of 8.4 mW/°C to 210 mW at 125°C.

recommended operating conditions

		MIN	NOM	MAX	UNIT
Operating free-air temperature, T_A	TLC555M	−55		125	°C
	TLC555I	−40		85	
	TLC555C	0		70	
Supply voltage, V_{DD}	TLC555M	5		18	
	TLC555I	3		18	
	TLC555C	2		18	

electrical characteristics at specified free-air temperature, V_{DD} = 2 V

PARAMETER	TEST CONDITIONS†		TLC555C			UNIT
			MIN	TYP	MAX	
Threshold voltage level		25°C	0.95	1.33	1.65	V
		Full range	0.85		1.75	
Threshold current		25°C		10		pA
		MAX		75		
Trigger voltage level		25°C	0.4	0.67	0.95	V
		Full range	0.3		1.05	
Trigger current		25°C		10		pA
		MAX		75		
Reset voltage level		25°C	0.4	1.1	1.5	V
		Full range	0.3		2	
Reset current		25°C		10		pA
		MAX		75		
Control voltage (open-circuit) as a percentage of supply voltage		MAX		66.7%		
Discharge switch on-state voltage	I_{OL} = 1 mA	25°C		0.03	0.2	V
		Full range			0.25	
Discharge switch off-state current		25°C		0.1		nA
		MAX		0.5		
Low-level output voltage	I_{OL} = 1 mA	25°C		0.07	0.3	V
		Full range			0.35	
High-level output voltage	I_{OH} = −300 μA	25°C	1.5	1.9		V
		Full range	1.5			
Supply current		25°C			250	μA

†Full range (MIN to MAX) is 0° to 70°C for TLC555C

electrical characteristics at specified free-air temperature, V_{DD} = 5 V

PARAMETER	TEST CONDITIONS†		TLC555M			TLC555C			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
Threshold voltage level		25°C	2.8	3.3	3.8	2.8	3.3	3.8	V
		Full range	2.7		3.9	2.7		3.9	
Threshold current		25°C		10			10		pA
		MAX		5000			75		
Trigger voltage level		25°C	1.36	1.66	1.96	1.36	1.66	1.96	V
		Full range	1.26		2.06	1.26		2.06	
Trigger current		25°C		10			10		pA
		MAX		5000			75		
Reset voltage level		25°C	0.4	1.1	1.5	0.4	1.1	1.5	V
		Full range	0.3		2	0.3		2	
Reset current		25°C		10			10		pA
		MAX		5000			75		
Control voltage (open-circuit) as a percentage of supply voltage		MAX		66.7%			66.7%		
Discharge switch on-state voltage	I_{OL} = 10 mA	25°C		0.14	0.5		0.14	0.5	V
		Full range			0.6			0.6	
Discharge switch off-state current		25°C		0.1			0.1		nA
		MAX		120			0.5		
Low-level output voltage	I_{OL} = 8 mA	25°C		0.21	0.4		0.21	0.4	V
		Full range			0.6			0.5	
	I_{OL} = 5 mA	25°C		0.13	0.3		0.13	0.3	
		Full range			0.45			0.4	
	I_{OL} = 3.2 mA	25°C		0.08	0.3		0.08	0.3	
		Full range			0.4			0.35	
High-level output voltage	I_{OH} = −1 mA	25°C	4.1	4.8		4.1	4.8		V
		Full range	4.1			4.1			
Supply current		25°C		170	350		170	350	μA

† Full range (MIN to MAX) is −55°C to 125°C for TLC555M, 0°C to 70°C for TLC555C, and −40°C to 85°C for TLC555I

electrical characteristics at specified free-air temperature, V_{DD} = 15 V

PARAMETER	TEST CONDITIONS†		TLC555M			TLC555C			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
Threshold voltage level		25°C	9.45	10	10.55	9.45	10	10.55	V
		Full range	9.35		10.65	9.35		10.65	
Threshold current		25°C		10			10		pA
		MAX		5000			75		
Trigger voltage level		25°C	4.65	5	5.35	4.65	5	5.35	V
		Full range	4.55		5.45	4.55		5.45	
Trigger current		25°C		10			10		pA
		MAX		5000			75		
Reset voltage level		25°C	0.4	1.1	1.5	0.4	1.1	1.5	V
		Full range	0.3		2	0.3		2	
Reset current		25°C		10			10		pA
		MAX		5000			75		
Control voltage (open-circuit) as a percentage of supply voltage		MAX		66.7%			66.7%		
Discharge switch on-state voltage	I_{OL} = 100 mA	25°C		0.77	1.7		0.77	1.7	V
		Full range			1.8			1.8	
Discharge switch off-state current		25°C		0.1			0.1		nA
		MAX		120			0.5		
Low-level output voltage	I_{OL} = 100 mA	25°C		1.28	3.2		1.28	3.2	V
		Full range			3.8			3.6	
	I_{OL} = 50 mA	25°C		0.63	1		0.63	1	
		Full range			1.5			1.3	
	I_{OL} = 10 mA	25°C		0.12	0.3		0.12	0.3	
		Full range			0.45			0.4	
High-level output voltage	I_{OH} = −10 mA	25°C	12.5	14.2		12.5	14.2		V
		Full range	12.5			12.5			
	I_{OH} = −5 mA	25°C	13.5	14.6		13.5	14.6		
		Full range	13.5			13.5			
	I_{OH} = −1 mA	25°C	14.2	14.9		14.2	14.9		
		Full range	14.2			14.2			
Supply current		25°C		360	600		360	600	μA

†Full range (MIN to MAX) is −55°C to 125°C for TLC555M, 0°C to 70°C for TLC555C, and −40°C to +85°C for TLC555I

electrical characteristics at specified free-air temperature, V_{DD} = 18 V

PARAMETER	TEST CONDITIONS†		TLC555M			TLC555C			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
Threshold voltage level		25°C	11.4	12	12.6	11.4	12	12.6	V
		Full range	10.9		12.7	10.9		12.7	
Threshold current		25°C		10			10		pA
		MAX		5000			75		
Trigger voltage level		25°C	5.6	6	6.4	5.6	6	6.4	V
		Full range	5.5		6.5	5.5		6.5	
Trigger current		25°C		10			10		pA
		MAX		5000			75		
Reset voltage level		25°C	0.4	1.1	1.5	0.4	1.1	1.5	V
		Full range	0.3		2	0.3		2	
Reset current		25°C		10			10		pA
		MAX		5000			75		
Control voltage (open-circuit) as a percentage of supply voltage		MAX		66.7%			66.7%		
Discharge switch on-state voltage	I_{OL} = 100 mA	25°C		0.72	1.5		0.72	1.5	V
		Full range			1.6			1.6	
Discharge switch off-state current		25°C		0.1			0.1		nA
		MAX		120			0.5		
Low-level output voltage	I_{OL} = 3.2 mA	25°C		0.04	0.3		0.04	0.3	V
		Full range			0.4			0.35	
High-level output voltage	I_{OH} = −1 mA	25°C	17.3	17.9		17.3	17.9		V
		Full range	17.3			17.3			
Supply current		25°C			600			600	μA

†Full range (MIN to MAX) is −55°C to 125°C for TLC555M, 0°C to 70°C for TLC555C, and −40°C to +85°C for TLC555I

operating characteristics, V_{DD} = 5 V, T_A = 25°C (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Initial error of timing interval	V_{DD} = 5 V to 15 V,		1%	3%	
Supply voltage sensitivity of timing interval	$R_A = R_B$ = 1 kΩ to 100 kΩ, C_T = 0.1 μF, See Note 3		0.1	0.5	%/V
Output pulse rise time	R_L = 10 MΩ, C_L = 10 pF		20	75	ns
Output pulse fall time			15	60	
Maximum frequency in astable mode	R_A = 470 Ω, R_B = 200 Ω, C_T = 200 pF, See Note 3	1.2	2.1		MHz

NOTE 3: R_A, R_B, and C_T are as defined in Figure 1.

TYPICAL APPLICATION DATA

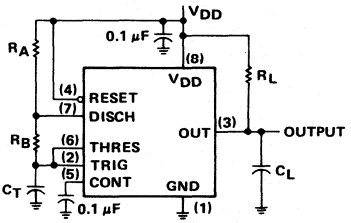


FIGURE 1. CIRCUIT FOR ASTABLE OPERATION

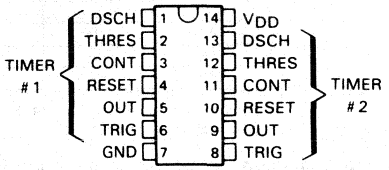
TEXAS INSTRUMENTS

TLC556M, TLC556I, TLC556C
DUAL LinCMOS™ TIMERS

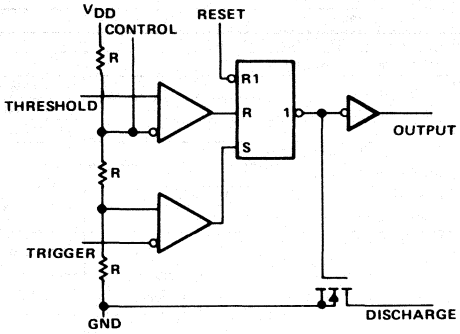
D2796, FEBRUARY 1984 – REVISED MAY 1988

- **Very Low Power Consumption . . . 2 mW Typ at V_{DD} = 5 V**
- **Capable of Operation in Astable Mode**
- **CMOS Output Capable of Swinging Rail to Rail**
- **High Output-Current Capability**
  Sink 100 mA Typ
  Source 10 mA Typ
- **Output Fully Compatible with CMOS, TTL, and MOS**
- **Low Supply Current Reduces Spikes During Output Transitions**
- **High-Impedance Inputs . . . 10^{12} Ω Typ**
- **Single-Supply Operation from 2 V to 18 V (unless specified)**
- **Functionally Interchangeable with the NE556; Has Same Pinout**

TLC556M . . . J DUAL-IN-LINE PACKAGE
TLC556I, TLC556C . . . D OR N DUAL-IN-LINE PACKAGE
(TOP VIEW)



functional block diagram (each timer)



Reset can override Trigger and Threshold.
Trigger can override Threshold.

description

The TLC556 is a monolithic timing circuit fabricated using TI's LinCMOS™ process, which provides full compatibility with CMOS, TTL, and MOS logic and operation at frequencies up to 2 MHz. Accurate time delays and oscillations are possible with smaller, less-expensive timing capacitors than the NE556 because of the high input impedance. Power consumption is low across the full range of power supply voltages.

Like the NE556, the TLC556 has a trigger level approximately one-third of the supply voltage and a threshold level approximately two-thirds of the supply voltage. These levels can be altered by use of the control voltage terminal. When the trigger input falls below the trigger level, the flip-flop is set and the output goes high. If the trigger input is above the trigger level and the threshold input is above the threshold level, the flip-flop is reset and the output is low. The reset input can override all other inputs and can be used to initiate a new timing cycle. If the reset input is low, the flip-flop is reset and the output is low. Whenever the output is low, a low-impedance path is provided between the discharge terminal and ground.

While the CMOS output is capable of sinking over 100 milliamperes and sourcing over 10 milliamperes, the TLC556 exhibits greatly reduced supply-current spikes during output transitions. This minimizes the need for the large decoupling capacitors required by the NE556.

These devices have internal electrostatic discharge (ESD) protection circuits that will prevent catastrophic failures at voltages up to 2000 volts as tested under MIL-STD-883C, Method 3015.2. However, care should be exercised in handling these devices as exposure to ESD may result in a degradation of the device parametric performance.

All unused inputs should be tied to an appropriate logic level to prevent false triggering.

The TLC556M is characterized for operation over the full military temperature range of −55°C to 125°C. The TLC556I is characterized for operation from −40°C to 85°C. The TLC556C is characterized for operation from 0°C to 70°C.

LinCMOS is a trademark of Texas Instruments.

TEXAS INSTRUMENTS

FUNCTION TABLE

RESET VOLTAGE†	TRIGGER VOLTAGE†	THRESHOLD VOLTAGE†	OUTPUT	DISCHARGE SWITCH
<MIN	Irrelevant	Irrelevant	Low	On
>MAX	<MIN	Irrelevant	High	Off
>MAX	>MAX	>MAX	Low	On
>MAX	>MAX	<MIN	As previously established	

† For conditions shown as MIN or MAX, use the appropriate value specified under electrical characteristics.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

		TLC556M	TLC556I	TLC556C	UNIT
Supply voltage (see Note 1)		18	18	18	V
Input voltage		−0.3 to V_{DD}	−0.3 to V_{DD}	−0.3 to V_{DD}	V
Sink current, discharge or output		150	150	150	mA
Source current, output		15	15	15	mA
Continuous total power dissipation at (or below) 25°C free-air temperature (see Note 2)	D package		950	950	mW
	J package	1375			
	N package		875	875	
Operating free-air temperature		−55 to 125	−40 to 85	0 to 70	°C
Storage temperature range		−65 to 150	−65 to 150	−65 to 150	°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	D or N package		260	260	°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds	J package	300			

NOTES: 1. All voltage values are with respect to network ground terminal.
2. For operation above 25°C, see the Dissipation Derating Table.

DISSIPATION DERATING TABLE

PACKAGE	POWER RATING	DERATING FACTOR	ABOVE T_A
D	950 mW	7.6 mW/°C	25°C
J (alloy mount)	1375 mW	11.0 mW/°C	25°C
N	875 mW	7.0 mW/°C	25°C

recommended operating conditions

		MIN	NOM	MAX	UNIT
Operating free-air temperature, T_A	TLC556M	−55		125	°C
	TLC556I	−40		85	
	TLC556C	0		70	
Supply voltage, V_{DD}	TLC556M	5		18	
	TLC556I	3		18	
	TLC556C	2		18	

electrical characteristics at specified free-air temperature, V_{DD} = 2 V

PARAMETER	TEST CONDITIONS†		TLC556C			UNIT
			MIN	TYP	MAX	
Threshold voltage level		25°C	0.95	1.33	1.65	V
		Full range	0.85		1.75	
Threshold current		25°C		10		pA
		MAX		75		
Trigger voltage level		25°C	0.4	0.67	0.95	V
		Full range	0.3		1.05	
Trigger current		25°C		10		pA
		MAX		75		
Reset voltage level		25°C	0.4	1.1	1.5	V
		Full range	0.3		1.8	
Reset current		25°C		10		pA
		MAX		75		
Control voltage (open-circuit) as a percentage of supply voltage		MAX		66.7%		
Discharge switch on-state voltage	I_{OL} = 1 mA	25°C		0.04	0.2	V
		Full range			0.25	
Discharge switch off-state current		25°C		0.1		nA
		MAX		0.5		
Low-level output voltage	I_{OL} = 1 mA	25°C		0.07	0.3	V
		Full range			0.35	
High-level output voltage	I_{OH} = −300 μA	25°C	1.5	1.9		V
		Full range	1.5			
Supply current	See Note 3	25°C		130	500	μA
		Full range			800	

† Full range (MIN to MAX) is 0°C to 70°C for TLC556C.

NOTE 3: These values apply for the expected operating configurations in which the Threshold terminal is connected directly to the Discharge terminal or to the Trigger terminal.

electrical characteristics at specified free-air temperature, V_{DD} = 5 V

PARAMETER	TEST CONDITIONS†		TLC556M			TLC556I			TLC556C			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
Threshold voltage level		25°C	2.8	3.3	3.8	2.8	3.3	3.8	2.8	3.3	3.8	V
		Full range	2.7		3.9	2.7		3.9	2.7		3.9	
Threshold current		25°C		10			10			10		pA
		MAX		5000			150			75		
Trigger voltage level		25°C	1.36	1.66	1.96	1.36	1.66	1.96	1.36	1.66	1.96	V
		Full range	1.26		2.06	1.26		2.06	1.26		2.06	
Trigger current		25°C		10			10			10		pA
		MAX		5000			150			75		
Reset voltage level		25°C	0.4	1.1	1.5	0.4	1.1	1.5	0.4	1.1	1.5	V
		Full range	0.3		1.8	0.3		1.8	0.3		1.8	
Reset current		25°C		10			10			10		pA
		MAX		5000			150			75		
Control voltage (open-circuit) as a percentage of supply voltage		MAX		66.7%			66.7%			66.7%		
Discharge switch on-state voltage	I_{OL} = 10 mA	25°C		0.15	0.5		0.15	0.5		0.15	0.5	V
		Full range			0.6			0.6			0.6	
Discharge switch off-state current		25°C		0.1			0.1			0.1		nA
		MAX		120			2			0.5		
Low-level output voltage	I_{OL} = 8 mA	25°C		0.21	0.4		0.21	0.4		0.21	0.4	
		Full range			0.6			0.5			0.5	
	I_{OL} = 5 mA	25°C		0.13	0.3		0.13	0.3		0.13	0.3	V
		Full range			0.45			0.4			0.4	
	I_{OL} = 3.2 mA	25°C		0.08	0.3		0.08	0.3		0.08	0.3	
		Full range			0.4			0.35			0.35	
High-level output voltage	I_{OH} = −1 mA	25°C	4.1	4.8		4.1	4.8		4.1	4.8		V
		Full range	4.1			4.1			4.1			
Supply current	See Note 3	25°C		340	700		340	700		340	700	μA
		Full range			1400			1200			1000	

† Full range (MIN to MAX) is −55°C to 125°C for TLC556M, −40°C to 85°C for TLC556I, and 0°C to 70°C for TLC556C.

NOTE 3: These values apply for the expected operating configuration in which the Threshold terminal is connected directly to the Discharge terminal or to the Trigger terminal.

electrical characteristics at specified free-air temperature, V_{DD} = 15 V

PARAMETER	TEST CONDITIONS†		TLC556M			TLC556I			TLC556C			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
Threshold voltage level		25°C	9.45	10	10.55	9.45	10	10.55	9.45	10	10.55	V
		Full range	9.35		10.65	9.35		10.65	9.35		10.65	
Threshold current		25°C		10			10			10		pA
		MAX		5000			150			75		
Trigger voltage level		25°C	4.65	5	5.35	4.65	5	5.35	4.65	5	5.35	V
		Full range	4.55		5.45	4.55		5.45	4.55		5.45	
Trigger current		25°C		10			10			10		pA
		MAX		5000			150			75		
Reset voltage level		25°C	0.4	1.1	1.5	0.4	1.1	1.5	0.4	1.1	1.5	V
		Full range	0.3		1.8	0.3		1.8	0.3		1.8	
Reset current		25°C		10			10			10		pA
		MAX		5000			150			75		
Control voltage (open-circuit) as a percentage of supply voltage		MAX		66.7%			66.7%			66.7%		
Discharge switch on-state voltage	I_{OL} = 100 mA	25°C		0.8	1.7		0.8	1.7		0.8	1.7	V
		Full range			1.8			1.8			1.8	
Discharge switch off-state current		25°C		0.1			0.1			0.1		nA
		MAX		120			2			0.5		
Low-level output voltage	I_{OL} = 100 mA	25°C		1.28	3.2		1.28	3.2		1.28	3.2	V
		Full range			3.8			3.7			3.6	
	I_{OL} = 50 mA	25°C		0.63	1		0.63	1		0.63	1	
		Full range			1.5			1.4			1.3	
	I_{OL} = 10 mA	25°C		0.12	0.3		0.12	0.3		0.12	0.3	
		Full range			0.45			0.4			0.4	
High-level output voltage	I_{OH} = −10 mA	25°C	12.5	14.2		12.5	14.2		12.5	14.2		V
		Full range	12.5			12.5			12.5			
	I_{OH} = −5 mA	25°C	13.5	14.6		13.5	14.6		13.5	14.6		
		Full range	13.5			13.5			13.5			
	I_{OH} = −1 mA	25°C	14.2	14.9		14.2	14.9	14.2	14.9			
		Full range	14.2			14.2			14.2			
Supply current	See Note 3	25°C		0.72	1.2		0.72	1.2		0.72	1.2	mA
		Full range			2			1.8			1.6	

† Full range (MIN to MAX) is −55°C to 125°C for TLC556M, −40°C to 85°C for TLC556I, and 0°C to 70°C for TLC556C.

NOTE 3: These values apply for the expected operating configurations in which the Threshold terminal is connected directly to the Discharge terminal or to the Trigger terminal.

electrical characteristics at specified free-air temperature, V_{DD} = 18 V

PARAMETER	TEST CONDITIONS†		TLC556M			TLC556I			TLC556C			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
Threshold voltage level		25°C	11.4	12	12.6	11.4	12	12.6	11.4	12	12.6	V
		Full range	10.9		12.7	10.9		12.7	10.9		12.7	
Threshold current		25°C		10			10			10		pA
		MAX		5000			150			75		
Trigger voltage level		25°C	5.6	6	6.4	5.6	6	6.4	5.6	6	6.4	V
		Full range	5.5		6.5	5.5		6.5	5.5		6.5	
Trigger current		25°C		10			10			10		pA
		MAX		5000			150			75		
Reset voltage level		25°C	0.4	1.1	1.5	0.4	1.1	1.5	0.4	1.1	1.5	V
		Full range	0.3		1.8	0.3		1.8	0.3		1.8	
Reset current		25°C		10			10			10		pA
		MAX		5000			150			75		
Control voltage (open-circuit) as a percentage of supply voltage		MAX		66.7%			66.7%			66.7%		
Discharge switch on-state voltage	I_{OL} = 100 mA	25°C		0.73	1.5		0.73	1.5		0.73	1.5	V
		Full range			1.6			1.6			1.6	
Discharge switch off-state current		25°C		0.1			0.1			0.1		nA
		MAX		120			2			0.5		
Low-level output voltage	I_{OL} = 3.2 mA	25°C		0.04	0.3		0.04	0.3		0.04	0.3	V
		Full range			0.4			0.35			0.35	
High-level output voltage	I_{OH} = −1 mA	25°C	17.3	17.9		17.3	17.9		17.3	17.9		V
		Full range	17.3			17.3			17.3			
Supply current	See Note 3	25°C			1.2			1.2			1.2	mA
		Full range			2			1.8			1.6	

† Full range (MIN to MAX) is −55°C to 125°C for TLC556M, −40°C to 85°C for TLC556I, and 0°C to 70°C for TLC556C.

NOTE 3: These values apply for the expected operating configurations in which the Threshold terminal is connected directly to the Discharge terminal or to the Trigger terminal.

operating characteristics, V_{DD} = 5 V, T_A = 25°C (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Initial error of timing interval	V_{DD} = 5 V to 15 V, $R_A = R_B$ = 1 kΩ to 100 kΩ, C_T = 0.1 μF, See Note 4		1%	3%	
Supply voltage sensitivity of timing interval			0.1	0.5	%/V
Output pulse rise time	R_L = 10 MΩ, C_L = 10 pF		20	75	ns
Output pulse fall time			15	60	
Maximum frequency in astable mode	R_A = 470 Ω, R_B = 200 Ω, C_T = 200 pF, See Note 3	1.2	2.1		MHz

NOTE 4: R_A, R_B, and C_T are as defined in Figure 3.

TYPICAL CHARACTERISTICS

DISCHARGE SWITCH ON-STATE RESISTANCE
vs
FREE-AIR TEMPERATURE

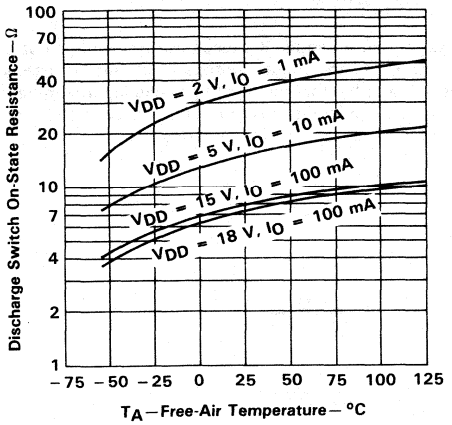
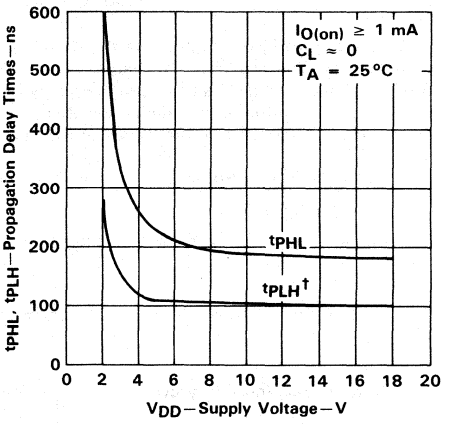


FIGURE 1

PROPAGATION DELAY TIMES TO DISCHARGE OUTPUT
FROM TRIGGER AND THRESHOLD SHORTED TOGETHER
vs
SUPPLY VOLTAGE



†The effects of the load resistance on these values must be taken into account separately.

FIGURE 2

TYPICAL APPLICATION DATA

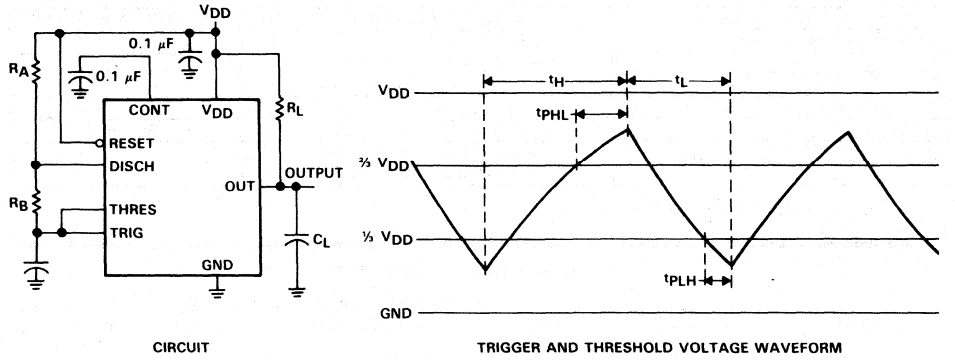


FIGURE 3. ASTABLE OPERATION

Connecting the trigger input to the threshold input as shown in Figure 3 causes the timer to run as a multivibrator. The capacitor C_T charges through R_A and R_B to the trigger voltage level (approximately $0.67V_{DD}$) and then discharges through R_B only to the value of the threshold voltage level (approximately $0.33V_{DD}$). The output is high during the charging cycle (t_H) and low during the discharge cycle (t_L). The duty cycle is controlled by the values of R_A, R_B, and C_T as shown in the equations below.

$$t_H \approx C_T (R_A + R_B) \ln 2 \qquad (\ln 2 = 0.693)$$

$$t_L \approx C_T R_B \ln 2$$

$$\text{Period} = t_H + t_L \approx C_T (R_A + 2R_B) \ln 2$$

$$\text{Output driver duty cycle} = \frac{t_L}{t_H + t_L} \approx 1 - \frac{R_B}{R_A + 2R_B}$$

$$\text{Output waveform duty cycle} = \frac{t_H}{t_H + t_L} \approx \frac{R_B}{R_A + 2R_B}$$

The 0.1-μF capacitor at the control pin in Figure 3 decreases the period by about 10%.

The formulas shown above do not allow for any propagation delay from the trigger and threshold inputs to the discharge output. These delay times add directly to the period and create differences between calculated and actual values that increase with frequency. In addition, the discharge output resistance r_{on} adds to R_B to provide another source of error in the calculation when R_B is very low or r_{on} is very high.

The equations below provide much better agreement with measured values.

$$t_H = C_T (R_A + R_B) \ln \left[3 - \exp\left(\frac{-t_{PLH}}{C_T (R_B + r_{on})} \right) \right] + t_{PHL}$$

$$t_L = C_T (R_B + r_{on}) \ln \left[3 - \exp\left(\frac{-t_{PHL}}{C_T (R_A + R_B)} \right) \right] + t_{PLH}$$

The similarity between the equations above and those given earlier in that a time constant is multiplied by the logarithm of a number or function can be seen. The effect of the propagation times on the timing can also be seen. The limit values of the logarithmic terms must be between ln 2 at low frequencies and ln 3 at extremely high frequencies. For a duty cycle close to 50%, an appropriate constant for the logarithmic terms can be substituted with good results. Duty cycles less than 50% $\left(\frac{t_H}{t_H + t_L}\right)$ will require that $\frac{t_H}{t_L} < 1$ and possibly $R_A \leq r_{on}$. These conditions can be difficult to obtain.

In monostable applications, the trip point of the trigger input can be set by a voltage applied to the control pin. An input voltage between 10% and 80% of the supply voltage from a resistor divider with at least 500 μA bias provides good results.

General Information 1

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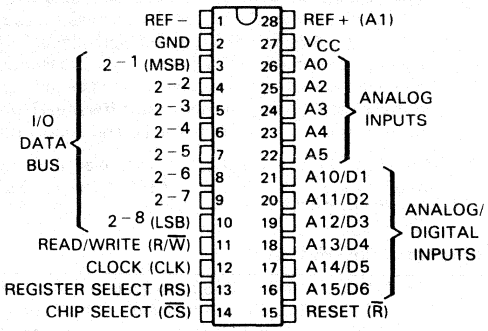
ANALOG TO DIGITAL CONVERTERS

	NUMBER OF INPUTS	RESOLUTION	SAMPLES PER SECOND	MAX ACCESS + CONVERSION TIME (μS)	TOTAL UNADJUSTED ERROR	TYPE POWER DISSIPATION (mW)	MAX SUPPLY CURRENT (mA)	PAGE No.
Serial Interface								
TLC549	1	8 Bits	40000	25	± 0.5 LSB	6.0	2.5	5-41
TLC548	1	8 Bits	45500	22	± 0.5 LSB	6.0	2.5	5-41
TLC540	11	8 Bits	75180	13.3	± 0.5 LSB	6.0	2.5	5-15
TLC541	11	8 Bits	40000	25	± 0.5 LSB	6.0	2.5	5-15
TLC545	19	8 Bits	76000	13	± 0.5 LSB	6.0	2.5	5-23
TLC546	19	8 Bits	40000	25	± 0.5 LSB	6.0	2.5	5-23
TLC1541	11	10 Bits	32258	31	± 1.0 LSB	6.0	2.5	5-77
TLC1540	11	10 Bits	32258	31	± 0.5 LSB	6.0	2.5	5-77
Parallel								
TLC532A	11*	8 Bits	66000	15	± 0.5 LSB	6.5	2.0	5-5
TLC533A	11*	8 Bits	33000	30	± 0.5 LSB	6.5	2.0	5-5
TLC7135	1	$4\frac{1}{2}$ Digits	—	—	± 1 Count	9.2	6.0	5-65
TLC0820	1	8 Bits		2.5	± 0.5 LSB	50	15.0	5-31
TLC1225	1	12 Bits	50500	10.2	± 0.5 LSB	4.5	9.0	5-49
TLC1205	1	12 Bits	50500	10.2	± 0.5 LSB	4.5	9.0	5-49

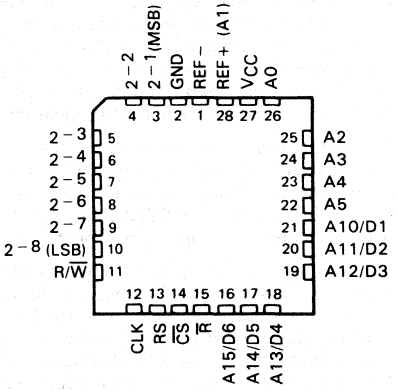
**5 Analog Inputs and 6 Multipurpose (Analog or Digital) inputs.*

- LinCMOS™ Technology
- 8-Bit Resolution
- Total Unadjusted Error . . . ±0.5 LSB Max
- Ratiometric Conversion
- Access Plus Conversion Time:
  TLC532A . . . 15 μs Max
  TLC533A . . . 30 μs Max
- 3-State, Bidirectional I/O Data Bus
- 5 Analog and 6 Dual-Purpose Inputs
- On-Chip 12-Channel Analog Multiplexer
- Three On-Chip 16-Bit Data Registers
- Software Compatible with Larger TL530 and TL531 (21-Input Versions)
- On-Chip Sample-and-Hold Circuit
- Single 5-V Supply Operation
- Low Power Consumption . . . 6.5 mW Typ
- Improved Direct Replacements for Texas Instruments TL532 and TL533, National Semiconductor ADC0829, and Motorola MC14442

N DUAL-IN-LINE PACKAGE
(TOP VIEW)



FN CHIP CARRIER PACKAGE
(TOP VIEW)



description

The TLC532A and TLC533A are monolithic LinCMOS™ peripheral integrated circuits each designed to interface a microprocessor for analog data acquisition. These devices are complete peripheral data acquisition systems on a single chip and can convert analog signals to digital data from up to 11 external analog terminals. Each device features operation from a single 5-volt supply. Each contains a 12-channel analog multiplexer, an 8-bit ratiometric analog-to-digital (A/D) converter, a sample-and-hold, three 16-bit registers, and microprocessor-compatible control circuitry. Additional features include a built-in self-test, six multipurpose (analog or digital) inputs, five external analog inputs, and an 8-pin input/output (I/O) data port. The three on-chip data registers store the control data, the conversion results, and the input digital data that can be accesssed via the microprocessor data bus in two 8-bit bytes (most-significant byte first). In this manner, a microprocessor can access up to 11 external analog inputs or 6 digital signals and the positive reference voltage that may be used for self-test.

FUNCTION TABLE

ADDRESS/CONTROL					DESCRIPTION
R/W	RS	CS	R	CLK	
X	X	X	L†		Reset
L	H	L	H	↓	Write bus data to control register
H	L	L	H	↑	Read data from analog conversion register
H	H	L	H	↑	Read data from ditigal data register
X	X	H	H	X	No response

H = High-level, L = Low-level, X = Irrelevant
↓ = High-to-low transition, ↑ = Low-to-high transition
†For proper operation, Reset must be low for at least three clock cycles.

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description (continued)

The A/D conversion uses the successive-approximation technique and switched-capacitor circuitry. This method eliminates the possibility of missing codes, nonmonotonicity, and a need for zero or full-scale adjustment. Any one of 11 analog inputs (or self-test) can be converted to an 8-bit digital word and stored in 10 microseconds (TLC532A) or 20 microseconds (TLC533A) after instructions from the microprocessor have been recognized. The on-chip sample-and-hold functions automatically to minimize errors due to noise on the analog inputs. Furthermore, differential high-impedance reference inputs are available to help isolate the analog circuitry from the logic and supply noises while easing ratiometric conversion and scaling.

The TLC532AM and TLC533AM are available in both the N and FN plastic packages and are characterized for operation from −55°C to 125°C. The TLC532AI and TLC533AI are characterized for operation from −40°C to 85°C.

functional description

The TLC532A and TLC533A provide direct interface to a microprocessor-based system. Control of the TLC532A and TLC533A is handled via the 8-line TTL-compatible 3-state data bus, the three control inputs (Read/Write, Register Select, and Chip Select), and the Clock input. Each device contains three 16-bit internal registers. These registers are the control register, the analog conversion data register, and the digital data register.

A high level at the Read/Write input and a low level at the Chip Select input set the device to output data on the 8-line data bus for the processor to read. A low level at the Read/Write input and a low level at the Chip Select input set the device to receive instructions into the internal control register on the 8-line data bus from the processor. When the device is in the read mode and the Register Select input is low, the processor will read the data contained in the analog conversion data register. However, when the Register Select input is high, the processor reads the data contained in the digital data register.

The control register is a write-only register into which the microprocessor writes command instructions for the device to start A/D conversion and to select the analog channel to be converted. The analog conversion data register is a read-only register that contains the current converter status and most recent conversion results. The digital data register is also a read-only register that holds the digital input logic levels from the six dual-purpose inputs.

Internally each device contains a byte pointer that selects the appropriate byte during two cycles of the Clock input in a normal 16-bit microprocessor instruction. The internal pointer will automatically point to the most-significant (MS) byte after the first complete clock cycle any time that the Chip Select is at the high level for at least one clock cycle. This causes the device to treat the next signal on the 8-line data bus as the MS byte. A low level at the Chip Select input activates the inputs and outputs and an internal function decoder. However, no data is transferred until the Clock goes high. The internal byte pointer first points to the MS byte of the selected register during the first clock cycle. After the first clock cycle in which the MS byte is accessed, the internal pointer switches to the LS byte and remains there for as long as Chip Select is low. The MS byte of any register may be accessed by either an 8-bit or a 16-bit microprocessor instruction; however, the LS byte may only be accessed by a 16-bit microprocessor instruction.

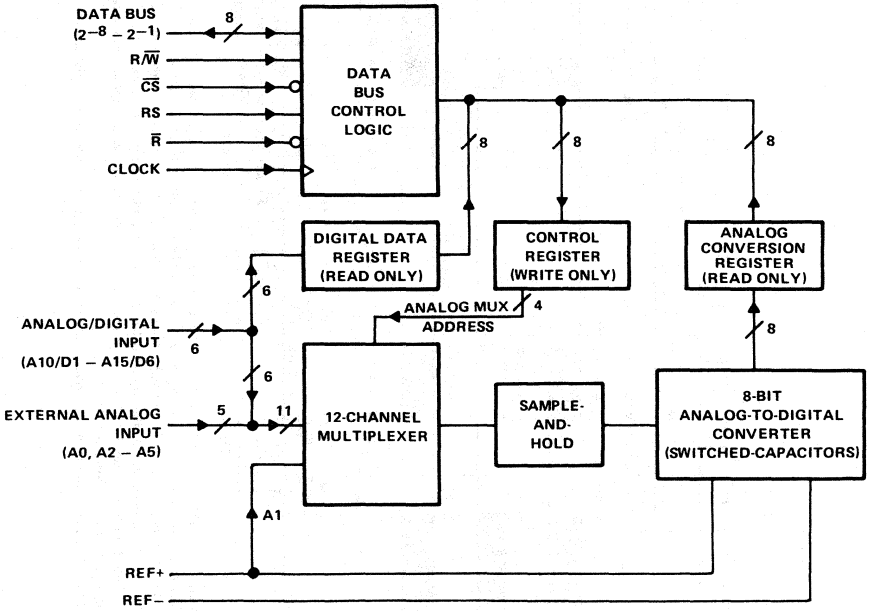
Normally, a two-byte word is written into or read from the controlling processor, but a single byte can be read by the processor by proper manipulation of the Chip Select input. This can be used to read conversion status from the analog conversion data register or the digital multipurpose input levels from the digital data register. The format and content of each two-byte word is shown in Figures 1 through 3.

functional description (continued)

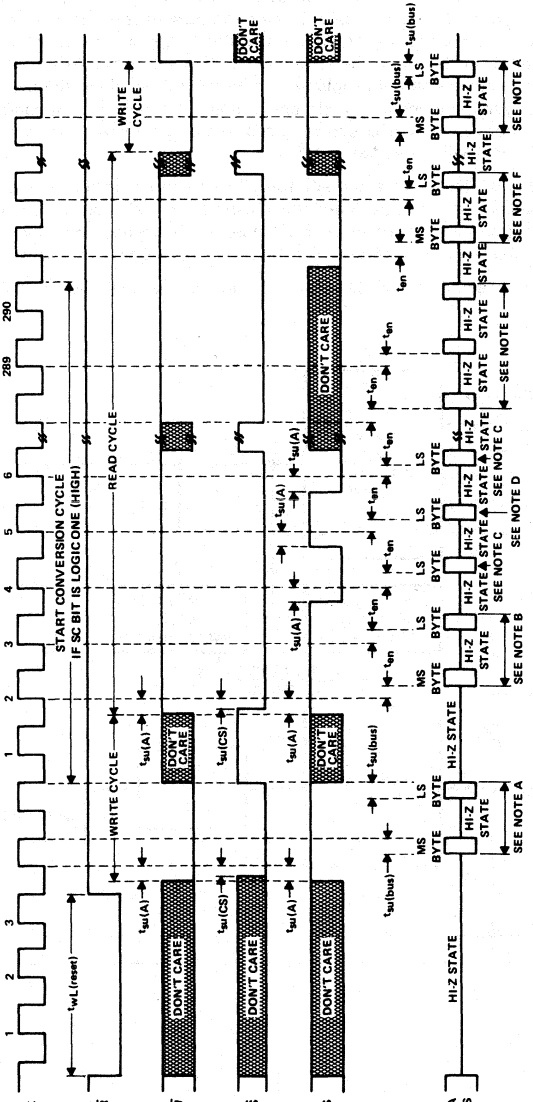
A conversion cycle is started after a two-byte instruction is written into the control register and the start conversion (SC) bit is a logic high. This two-byte instruction also selects the input analog channel to be converted. The status (EOC) bit in the analog conversion data register is reset and it remains reset until the conversion is completed, at that time the status bit is then set again. After conversion, the results are loaded into the analog conversion data register. These results remain in the analog conversion data register until the next conversion cylce is completed. If a new conversion command is entered into the control register while the conversion cycle is in progress, the on-going conversion will be aborted and a new channel acquisition cycle will immediately begin.

The Reset input allows the device to be externally forced to a known state. When a low level is applied to the Reset input for a minimum of three clock periods, the start conversion bit is cleared. The A/D converter is then idled and all the outputs are placed in the high-impedance off-state. However, the content of the analog conversion data register is not affected by the Reset input going to a low level.

Detailed information on interfacing to most popular microprocessors is readily available from the factory.

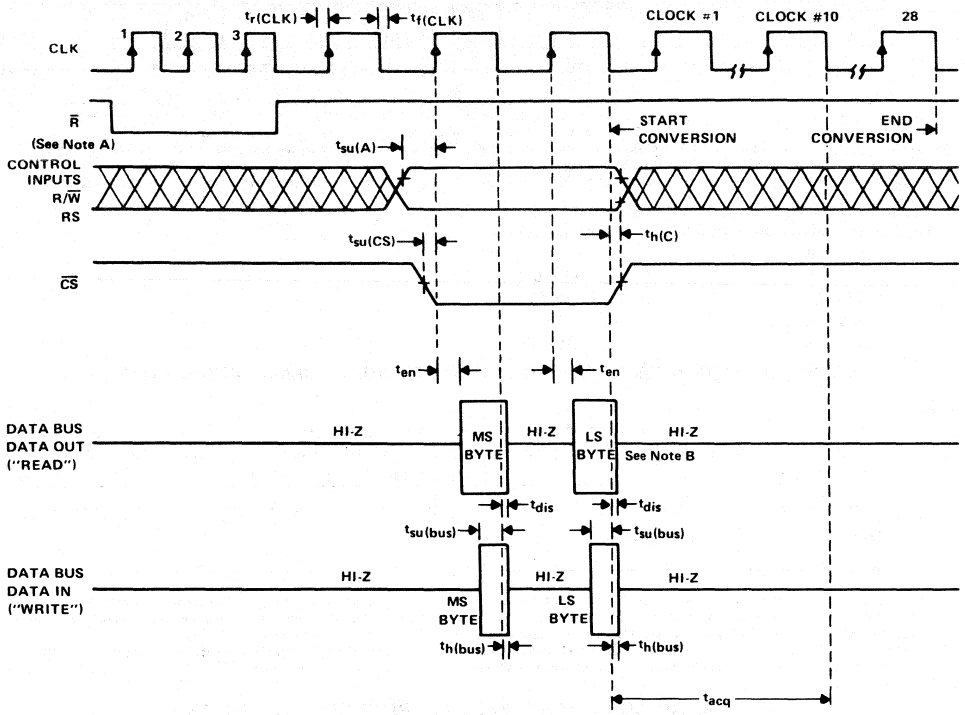


typical operating sequence



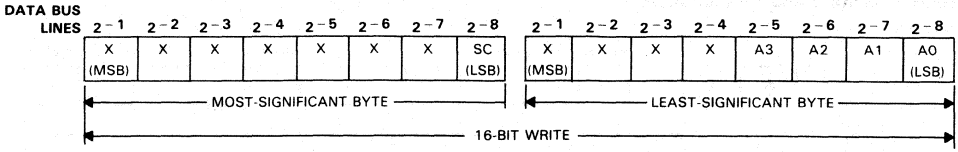
NOTES:
A. This is a 16-bit input instruction from the microprocessor being sent to the control data register.
B. This is the 2-byte (16-bit) content of the digital data register being sent to the microprocessor.
C. This is the LS byte (8-bit) content of the analog conversion data register being sent to the microprocessor.
D. This is the LS byte (8-bit) content of the digital data register being sent to the microprocessor.
E. These are MS byte (8-bit), LS byte (8-bit), and LS byte (8-bit) content of the analog conversion data register or digital data register being sent to the microprocessor.
F. This is the 2-byte (16-bit) content of the analog conversion data register being sent to the microprocessor.

read or write cycle time sequence



NOTES: A. The reset pulse ($\overline{R}$ low) is required only during power-up.

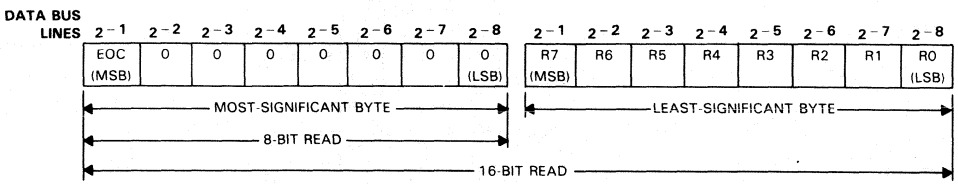
B. The most-significant byte output of Data Out occurs when CLK is high. When CLK is low, Data Out is in the high-impedance (off) state. When CLK goes high again, the least-significant byte is placed on the data bus. At this point, the least-significant byte will remain on the bus for as long as CLK is kept high.



Unused Bits (X)— The MS byte bits 2^{-1} through 2^{-7} and LS byte bits 2^{-1} through 2^{-4} of the control register are not used internally.
Start Conversion (SC)— When the SC bit in the MS byte is set to a logical 1 (high level), analog-to-digital conversion of the specified analog channel will begin immediately after the completion of the control register write.
Analog Multiplex Address (A0-A3)— These four address bits are decoded by the analog multiplexer and used to select the appropriate analog channel as shown below:

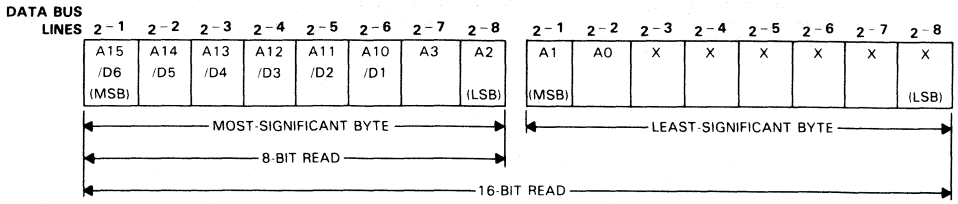
Hexadecimal Address (A3 = MSB)	Channel Select
0	A0
1	REF+ (A1)
2-5	A2-A5
6-9 (not used)	
A-F	A10-A15

FIGURE 1. CONTROL REGISTER TWO-BYTE WRITE WORD FORMAT AND CONTENT



A/D Status (EOC)— The A/D status end-of-conversion (EOC) bit is set whenever an analog-to-digital conversion is successfully completed by the A/D converter. The status bit is cleared by a 16-bit write from the microprocessor to the control register. The remainder of the bits in the MS byte of the analog conversion data register are always reset to logical 0 to simplify microprocessor interrogation of the A/D converter status.
A/D Result (R0-R7)— The LS byte of the analog conversion data register contains the result of the analog-to-digital conversion. Result bit R7 is the MSB and the converter follows the standard convention of assigning a code of all ones (11111111) to a full-scale analog voltage. There are no special overflow or underflow indications.

FIGURE 2. ANALOG CONVERSION DATA REGISTER ONE-BYTE AND TWO-BYTE READ WORD FORMAT AND CONTENT



Shared Digital Port (A10/D1-A15/D6)— The voltage present on these pins is interpreted as a digital signal and the corresponding states are read from these bits. A digital value will be given for each pin even if some or all of these pins are being used as analog inputs.
Analog Multiplexer Address (A0-A3)— The address of the selected analog channel presently addressed is given by these bits.
Unused Bits (X)— LS byte bits 2^{-3} through 2^{-8} of the digital data register are not used.

FIGURE 3. DIGITAL DATA REGISTER ONE-BYTE AND TWO-BYTE READ WORD FORMAT AND CONTENT

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . −0.3 V to 6.5 V
Input voltage range: Positive reference voltage . . . . . V_{REF-} to V_{CC} + 0.3 V
Negative reference voltage . . . . . −0.3 V to V_{REF+}
All other inputs . . . . . −0.3 V to V_{CC} + 0.3 V
Input current, I_I (any input) . . . . . ±10 mA
Total input current, (all inputs) . . . . . ±20 mA
Operating free-air temperature range: TLC532AM, TLC533AM . . . . . −55°C to 125°C
TLC532AI, TLC533AI . . . . . −40°C to 85°C
Storage temperature range . . . . . −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: N package . . . . . 260°C
Case temperature for 10 seconds: FN package . . . . . 260°C

NOTE 1: All voltage values are with respect to network ground terminal.

recommended operating conditions

		TLC532A			TLC533A			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}		4.75	5	5.5	4.75	5	5.5	V
Positive reference voltage, V_{REF+} (see Note 2)		2.5	V_{CC}	$V_{CC}+0.1$	2.5	V_{CC}	$V_{CC}+0.1$	V
Negative reference voltage, V_{REF-} (see Note 2)		−0.1	0	2.5	−0.1	0	2.5	V
Differential reference voltage, $V_{REF+} - V_{REF-}$		1	V_{CC}	$V_{CC}+0.2$	1	V_{CC}	$V_{CC}+0.2$	V
High-level input voltage, V_{IH}	Clock input	$V_{CC}-0.8$			$V_{CC}-0.8$			V
	All other digital inputs	2			2			
Low-level input voltage, V_{IL}	Any digital input			0.8			0.8	V
Clock frequency, f_{CLK}		0.1	2	2.048	0.1	1.048	1.06	MHz
CS setup time, $t_{su(CS)}$		75			100			ns
Address (R/W and RS) setup time, $t_{su(A)}$		100			145			ns
Data bus input setup time, $t_{su(bus)}$		140			185			ns
Control (R/W, RS, and CS) hold time, $t_{h(C)}$		10			20			ns
Data bus input hold time, $t_{h(bus)}$		15			20			ns
Pulse duration of control during read, $t_{w(C)}$		305			575			ns
Pulse duration, reset low, $t_{wL(reset)}$		3			3			Clock Cycles
Pulse duration of clock high, $t_{wH(CLK)}$		230			440			ns
Pulse duration of clock low, $t_{wL(CLK)}$		200			410			ns
Clock rise time, $t_{r(CLK)}$				15			25	ns
Clock fall time, $t_{f(CLK)}$				16			30	ns
Operating free-air temperature, T_A	TLC_ _AM	−55		125	−55		125	°C
	TLC_ _AI	−40		85	−40		85	

NOTE 2: Analog input voltages greater than or equal to that applied to the REF+ terminal convert to all ones (11111111), while input voltages equal to or less than that applied to the REF− terminal convert to all zeros (00000000). For proper operation, the positive reference voltage, V_{REF+}, must be at least 1-volt greater than the negative reference voltage, V_{REF-}. In addition, unadjusted errors may increase as the differential reference voltage, $V_{REF+} - V_{REF-}$, falls below 4.75 volts.

electrical characteristics over recommended operating free-air temperature range, V_{REF+} = V_{CC}, V_{REF-} at ground, f_{CLK} = 2 MHz (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP†	MAX	UNIT
V_{OH}	High-level output voltage		I_{OH} = −1.6 mA	2.4			V
V_{OL}	low-level output voltage		I_{OL} = 1.6 mA			0.4	V
I_{IH}	High-level input current	Any digital or Clock input	V_{IH} = 5.5 V			10	μA
		Any control input				1	
I_{IL}	Low-level input current	Any digital or Clock input	V_{IL} = 0			−10	μA
		Any control input				−1	
I_{OZ}	Off-state (high impedance-state) output current		$V_O = V_{CC}$			10	μA
			V_O = 0			−10	
I_I	Analog input current (see Note 3)		V_I = 0 to V_{CC}			±500	nA
	Leakage current between selected channel and all other analog channels		V_I = 0 to V_{CC}, Clock input at 0 V			±400	nA
C_i	Input capacitance	Digital pins 3 thru 10			4	30	pF
		Any other input pin			2	15	
$I_{CC} + I_{REF+}$	Supply current plus reference current		V_{CC} = V_{REF+} = 5.5 V, Outputs open		1.5	3	mA
I_{CC}	Supply current		V_{CC} = 5.5 V		1.4	2	mA

NOTE 3: Analog input current is an average of the current flowing into a selected analog channel input during one full conversion cycle.

operating characteristics over recommended operating free-air temperature range, V_{REF+} = V_{CC}, V_{REF-} at ground, f_{CLK} = 2 MHz (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP†	MAX	UNIT
	Linearity error		See Note 4			±0.5	LSB
	Zero error		See Note 5			±0.5	LSB
	Full-scale error		See Note 5			±0.5	LSB
	Total unadjusted error		See Note 6			±0.5	LSB
	Absolute accuracy error		See Note 7			±1	LSB
t_{conv}	Conversion time (including channel acquisition time)				30		Clock Cycles
t_{acq}	Channel acquisition time prior to starting conversion				10		Clock Cycles
t_{en}	Data output enable time (see Note 8)		C_L = 50 pF, R_L = 3 kΩ,			250	ns
t_{dis}	Data output disable time		C_L = 50 pF, R_L = 3 kΩ	10			ns
$t_{r(bus)}$	Data bus output rise time	High-impedance to high-level	C_L = 50 pF, R_L = 3 kΩ			150	ns
		Low to high-level				300	
$t_{f(bus)}$	Data bus output fall time	High-impedance to low-level	C_L = 50 pF, R_L = 3 kΩ			150	ns
		High to low-level				300	

†Typical values are at V_{CC} = 5 V, T_A = 25°C.

NOTES: 4. Linearity error is the deviation from the best straight line through the A/D transfer characteristics.
5. Zero error is the difference between 00000000 and the converted output for zero input voltage; full-scale error is the difference between 11111111 and the converted output for full-scale input voltage.
6. Total unadjusted error is the sum of linearity, zero, and full-scale errors.
7. Absolute accuracy error is the maximum difference between an analog value and the nominal midstep value within any step. This includes all errors including inherent quantization error, which is the ±0.5 LSB uncertainty caused by the A/D converters finite resolution.
8. If chip-select setup time, $t_{su(CS)}$, is less than 0.14 microseconds, the effective data output enable time, t_{en}, may extend such that $t_{su(CS)} + t_{en}$ is equal to a maximum of 0.475 microseconds.

electrical characteristics over recommended ranges V_{CC}, V_{REF+}, and operating free-air temperature, V_{REF-} at ground, f_{CLK} = 1.048 MHz (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP†	MAX	UNIT
V_{OH}	High-level output voltage		I_{OH} = −1.6 mA	2.4			V
V_{OL}	Low-level output voltage		I_{OL} = 1.6 mA			0.4	V
I_{IH}	High-level input current	Any digital or Clock input	V_{IH} = 5.5 V			10	μA
		Any control input				1	
I_{IL}	Low-level input current	Any digital or Clock input	V_{IL} = 0			−10	μA
		Any control input				−1	
I_{OZ}	Off-state (high impedance-state) output current		$V_O = V_{CC}$			10	μA
			V_O = 0			−10	
I_I	Analog input current (see Note 3)		V_I = 0 to V_{CC}			±500	nA
	Leakage current between selected channel and all other analog channels		V_I = 0 to V_{CC}, Clock input at 0 V			±400	nA
C_i	Input capacitance	Digital pins 3 thru 10			4	30	pF
		Any other input pin			2	15	
$I_{CC}+I_{REF+}$	Supply current plus reference current		V_{CC} = V_{REF+} = 5.5 V, Outputs open		1.3	3	mA
I_{CC}	Supply current		V_{CC} = 5.5 V		1.2	2	mA

NOTE 3: Analog input current is an average of the current flowing into a selected analog channel input during one full conversion cycle.

operating characteristics over recommended ranges V_{CC}, V_{REF+}, and operating free-air temperature, V_{REF-} at ground, f_{clock} = 1.048 MHz (unless otherwise noted)

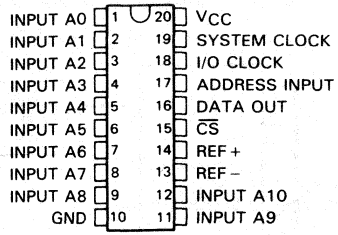
PARAMETER			TEST CONDITIONS	MIN	TYP†	MAX	UNIT
	Linearity error		See Note 4			±0.5	LSB
	Zero error		See Note 5			±0.5	LSB
	Full-scale error		See Note 5			±0.5	LSB
	Total unadjusted error		See Note 6			±0.5	LSB
	Absolute accuracy error		See Note 7			±1	LSB
t_{conv}	Conversion time (including channel acquisition time)				30		Clock Cycles
t_{acq}	Channel acquisition time prior to starting conversion				10		Clock Cycles
t_{en}	Data output enable time (see Note 8)		C_L = 50 pF, R_L = 3 kΩ,			335	ns
t_{dis}	Data output disable time		C_L = 50 pF, R_L = 3 kΩ	10			ns
$t_{r(bus)}$	Data bus output rise time	High-impedance to high-level	C_L = 50 pF, R_L = 3 kΩ			150	ns
		Low to high-level				300	
$t_{f(bus)}$	Data bus output fall time	High-impedance to low-level	C_L = 50 pF, R_L = 3 kΩ			150	ns
		High to low-level				300	

†Typical values are at V_{CC} = 5 V, T_A = 25°C.

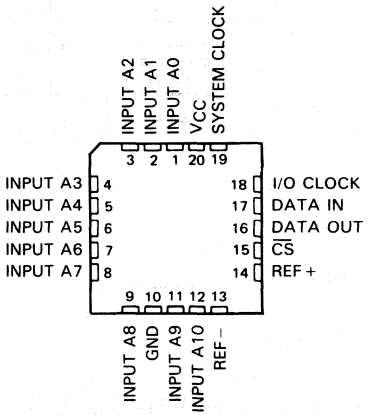
NOTES: 4. Linearity error is the deviation from the best straight line through the A/D transfer characteristics.
5. Zero error is the difference between 00000000 and the converted output for zero input voltage; full-scale error is the difference between 11111111 and the converted output for full-scale input voltage.
6. Total unadjusted error is the sum of linearity, zero, and full-scale errors.
7. Absolute accuracy error is the maximum difference between an analog value and the nominal midstep value within any step. This includes all errors including inherent quantization error, which is the ±0.5 LSB uncertainty caused by the A/D converters finite resolution.
8. If chip-select setup time, $t_{su(CS)}$, is less than 0.14 microseconds, the effective data output enable time, t_{en}, may extend such that $t_{su(CS)}$ + t_{en} is equal to a maximum of 0.475 microseconds.

- LinCMOS™ Technology
- 8-Bit Resolution A/D Converter
- Microprocessor Peripheral or Stand-Alone Operation
- On-Chip 12-Channel Analog Multiplexer
- Built-In Self-Test Mode
- Software-Controllable Sample and Hold
- Total Unadjusted Error . . . ±0.5 LSB Max
- TLC541 is Direct Replacement for Motorola MC145040 and National Semiconductor ADC0811. TLC540 is Capable of Higher Speed
- Pinout and Control Signals Compatible with TLC1540 Family of 10-Bit A/D Converters

N DUAL-IN-LINE PACKAGE
(TOP VIEW)



FN CHIP CARRIER PACKAGE
(TOP VIEW)



TYPICAL PERFORMANCE	TLC540	TLC541
Channel Acquisition Sample Time	2 μs	3.6 μs
Conversion Time	9 μs	17 μs
Samples per Second	75 × 10^3	40 × 10^3
Power Dissipation	6 mW	6 mW

description

The TLC540 and TLC541 are LinCMOS™ A/D peripherals built around an 8-bit switched-capacitor successive-approximation A/D converter. They are designed for serial interface to a microprocessor or peripheral via a three-state output with up to four control inputs [including independent System Clock, I/O Clock, Chip Select ($\overline{CS}$), and Address Input]. A 4-megahertz system clock for the TLC540 and a 2.1-megahertz system clock for the TLC541 with a design that includes simultaneous read/write operation allow high-speed data transfers and sample rates of up to 75,180 samples per second for the TLC540 and 40,000 samples per second for the TLC541. In addition to the high-speed converter and versatile control logic, there is an on-chip 12-channel analog multiplexer that can be used to sample any one of 11 inputs or an internal "self-test" voltage, and a sample-and-hold that can operate automatically or under microprocessor control. Detailed information on interfacing to most popular microprocessors is readily available from the factory.

The converters incorporated in the TLC540 and TLC541 feature dproofifferential high-impedance reference inputs that facilitate ratiometric conversion, scaling, and analog circuitry isolation from logic and supply noises. A switched-capacitor design allows guaranteed low-error (±0.5 LSB) conversion in 9 microseconds for the TLC540 and 17 microseconds for the TLC541 over the full operating temperature range.

The TLC540 and the TLC541 are available in both the N and FN plastic packages. The M-suffix versions are characterized for operation from −55°C to 125°C. The I-suffix versions are characterized for operation from −40°C to 85°C.

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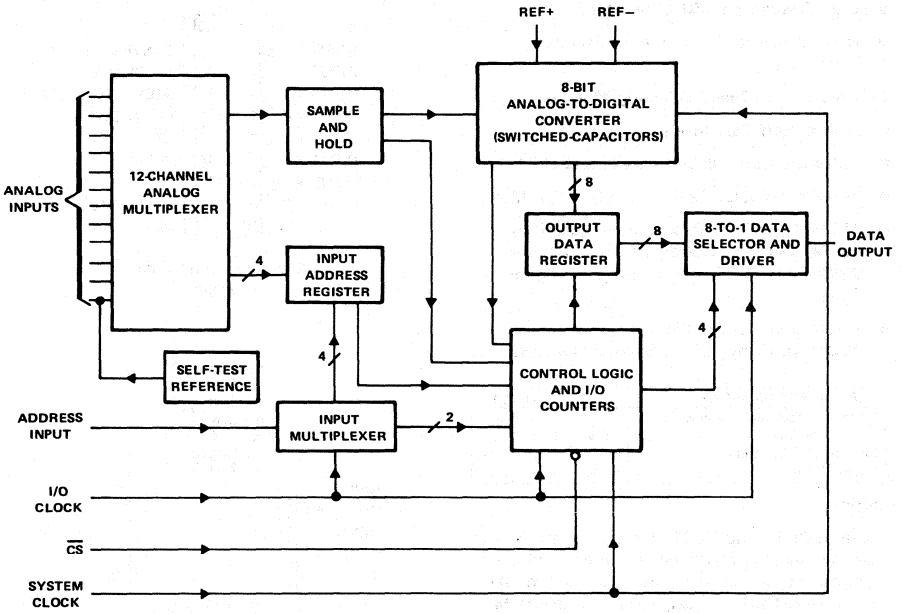
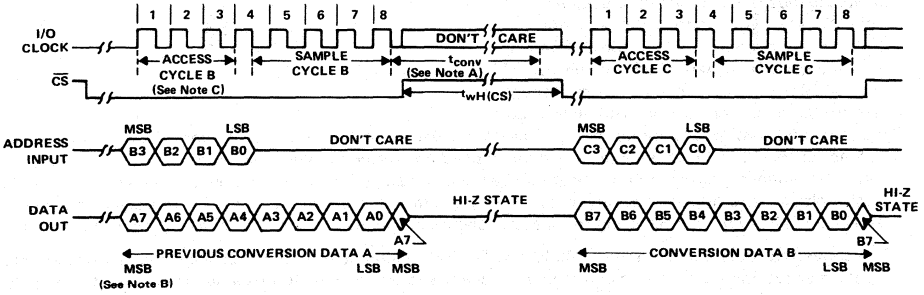
functional block diagram



operating sequence



NOTES: A. The conversion cycle, which requires 36 System Clock periods, is initiated on the 8th falling edge of the I/O Clock after $\overline{CS}$ goes low for the channel whose address exists in memory at that time. If $\overline{CS}$ is kept low during conversion, the I/O Clock must remain low for at least 36 System Clock cycles to allow conversion to be completed.

B. The most significant bit (MSB) will automatically be placed on the DATA OUT bus after $\overline{CS}$ is brought low. The remaining seven bits (A6-A0) will be clocked out on the first seven I/O Clock falling edges.

C. To minimize errors caused by noise at the $\overline{CS}$ input, the internal circuitry waits for three System Clock cycles (or less) after a chip select falling edge is detected before responding to control input signals. Therefore, no attempt should be made to clock-in address data until the minimum chip-select setup time has elapsed.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 6.5 V
Input voltage range (any input) . . . . . −0.3 V to V_{CC} + 0.3 V
Output voltage range . . . . . −0.3 V to V_{CC} + 0.3 V
Peak input current range (any input) . . . . . ±10 mA
Peak total input current (all inputs) . . . . . ±30 mA
Operating free-air temperature range: TLC540I, TLC541I . . . . . −40°C to 85°C
TLC540M, TLC541M . . . . . −55°C to 125°C
Storage temperature range . . . . . −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds . . . . . 260°C

NOTE 1: All voltage values are with respect to digital ground with REF− and GND wired together (unless otherwise noted).

recommended operating conditions

			TLC540			TLC541			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}			4.75	5	5.5	4.75	5	5.5	V
Positive reference voltage, V_{REF+} (see Note 2)			2.5	V_{CC}	$V_{CC}+0.1$	2.5	V_{CC}	$V_{CC}+0.1$	V
Negative reference voltage, V_{REF-} (see Note 2)			−0.1	0	2.5	0.1	0	2.5	V
Differential reference voltage, $V_{REF+} - V_{REF-}$ (see Note 2)			1	V_{CC}	$V_{CC}+0.2$	1	V_{CC}	$V_{CC}+0.2$	V
Analog input voltage (see Note 2)			0		V_{CC}	0		V_{CC}	V
High-level control input voltage, V_{IH}			2			2			V
Low-level control input voltage, V_{IL}					0.8			0.8	V
Setup time, address bits at data input before I/O CLK↑, $t_{su(A)}$			200			400			ns
Hold time, address bits after I/O CLK↑, $t_{h(A)}$			0			0			ns
Setup time, $\overline{CS}$ low before clocking in first address bit, $t_{su(CS)}$ (see Note 3)			3			3			System clock cycles
$\overline{CS}$ high during conversion, $t_{wH(CS)}$			36			36			System clock cycles
Input/Output clock frequency, $f_{CLK(I/O)}$			0		2.048	0		1.1	MHz
System clock frequency, $f_{CLK(SYS)}$			$f_{CLK(I/O)}$		4	$f_{CLK(I/O)}$		2.1	MHz
System clock high, $t_{wH(SYS)}$			110			210			ns
System clock low, $t_{wL(SYS)}$			100			190			ns
Input/Output clock high, $t_{wH(I/O)}$			200			404			ns
Input/Output clock low, $t_{wL(I/O)}$			200			404			ns
Clock transition time (see Note 4)	System	$f_{CLK(SYS)} \le 1048$ kHz			30			30	ns
		$f_{CLK(SYS)} > 1048$ kHz			20			20	
	I/O	$f_{CLK(I/O)} \le 525$ kHz			100			100	ns
		$f_{CLK(I/O)} > 525$ kHz			40			40	
Operating free-air temperature, T_A		TLC540M, TLC541M	−55		125	−55		125	°C
		TLC540I, TLC541I	−40		85	−40		85	

NOTES: 2. Analog input voltages greater than that applied to REF+ convert as all "1"s (11111111), while input voltages less than that applied to REF− convert as all "0"s (00000000). For proper operation, REF+ voltage must be at least 1 volt higher than REF− voltage. Also, the total unadjusted error may increase as this differential reference voltage falls below 4.75 volts.

3. To minimize errors caused by noise at the chip select input, the internal circuitry waits for three System Clock cycles (or less) after a chip select falling edge is detected before responding to control input signals. Therefore, no attempt should be made to clock-in an address until the minimum chip select setup time has elapsed.

4. This is the time required for the clock input signal to fall from V_{IH} min to V_{IL} max or to rise from V_{IL} max to V_{IH} min. In the vicinity of normal room temperature, the devices function with input clock transition time as slow as 2 microseconds for remote data acquisition applications where the sensor and the A/D converter are placed several feet away from the controlling microprocessor.

electrical characteristics over recommended operating temperature range, V_{CC} = V_{REF+} = 4.75 V to 5.5 V (unless otherwise noted), $f_{CLK(I/O)}$ = 2.048 MHz for TLC540 or $f_{CLK(I/O)}$ = 1.1 MHz for TLC541

PARAMETER			TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{OH}	High-level output voltage (pin 16)		V_{CC} = 4.75 V,	I_{OH} = 360 μA	2.4			V
V_{OL}	Low-level output voltage		V_{CC} = 4.75 V,	I_{OL} = 1.6 mA			0.4	V
I_{OZ}	Off-state (high-impedance state) output current		V_O = V_{CC},	$\overline{CS}$ at V_{CC}			10	μA
			V_O = 0,	$\overline{CS}$ at V_{CC}			−10	
I_{IH}	High-level input current		V_I = V_{CC}			0.005	2.5	μA
I_{IL}	Low-level input current		V_I = 0			−0.005	−2.5	μA
I_{CC}	Operating supply current		$\overline{CS}$ at 0 V			1.2	2.5	mA
	Selected channel leakage current		Selected channel at V_{CC}, Unselected channel at 0 V			0.4	1	μA
			Selected channel at 0 V, Unselected channel at V_{CC}			−0.4	−1	
I_{CC} + I_{REF}	Supply and reference current		V_{REF+} = V_{CC},	$\overline{CS}$ at 0 V		1.3	3	mA
C_i	Input capacitance	Analog inputs				7	55	pF
		Control inputs				5	15	

†All typical values are at T_A = 25°C.

5

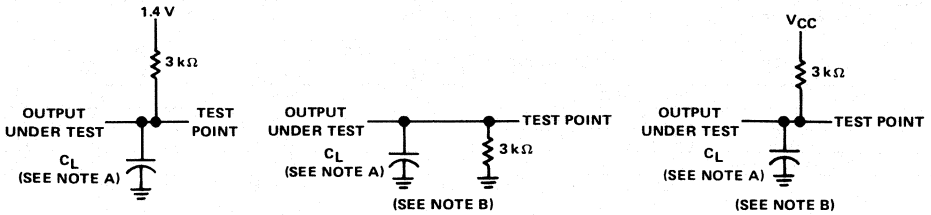
Analog to Digital Converters

operating characteristics over recommended operating free-air temperature range, V_{CC} = V_{REF+} = 4.75 V to 5.5 V, $f_{CLK(I/O)}$ = 2.048 MHz for TLC540 or 1.1 MHz for TLC541, $f_{CLK(SYS)}$ = 4 MHz for TLC540 or 2.1 MHz for TLC541.

	PARAMETER	TEST CONDITIONS	TLC540			TLC541			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
	Linearity error	See Note 5			±0.5			±0.5	LSB
	Zero error	See Notes 2 and 6			±0.5			±0.5	LSB
	Full-scale error	See Notes 2 and 6			±0.5			±0.5	LSB
	Total unadjusted error	See Note 7			±0.5			±0.5	LSB
	Self-test output code	Input A11 address = 1011 (See Note 8)	01111101 (125)		10000011 (131)	01111101 (125)		10000011 (131)	
t_{conv}	Conversion time	See Operating Sequence			9			17	μs
	Total access and conversion time	See Operating Sequence			13.3			25	μs
t_{acq}	Channel acquisition time (sample cycle)	See Operating Sequence			4			4	I/O clock cycles
t_v	Time output data remains valid after I/O clock↓		10			10			ns
t_d	Delay time, I/O clock↓ to data output valid	See Parameter Measurement Information			300			400	ns
t_{en}	Output enable time				150			150	ns
t_{dis}	Output disable time				150			150	ns
$t_{r(bus)}$	Data bus rise time				300			300	ns
$t_{f(bus)}$	Data bus fall time				300			300	ns

NOTES: 2. Analog input voltages greater than that applied to REF+ convert to all "1"s (11111111), while input voltages less than that applied to REF− convert to all"0"s (00000000). For proper operation, REF+ voltage must be at least 1 volt higher than REF− voltage. Also, the total unadjusted error may increase as this differential reference voltage falls below 4.75 volts.
5. Linearity error is the maximum deviation from the best straight line through the A/D transfer characteristics.
6. Zero error is the difference between 00000000 and the converted output for zero input voltage; full-scale error is the difference between 11111111 and the converted for full-scale input voltage.
7. Total unadjusted error is the sum of linearity, zero, and full-scale errors.
8. Both the input address and the output codes are expressed in positive logic. The A11 analog input signal is internally generated and is used for test purposes.

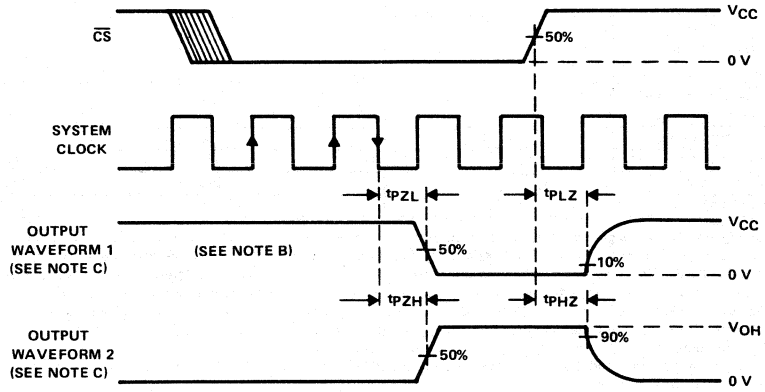
PARAMETER MEASUREMENT INFORMATION



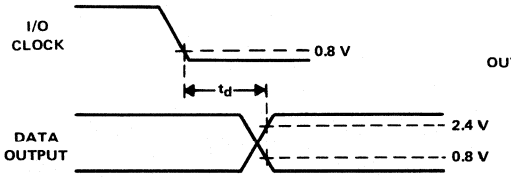
LOAD CIRCUIT FOR t_d, t_r, AND t_f

LOAD CIRCUIT FOR t_{PZH} AND t_{PHZ}

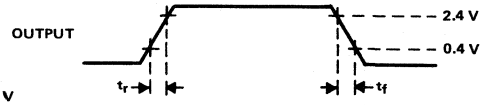
LOAD CIRCUIT FOR t_{PZL} AND t_{PLZ}



VOLTAGE WAVEFORMS FOR ENABLE AND DISABLE TIMES



VOLTAGE WAVEFORM FOR DELAY TIME



VOLTAGE WAVEFORM FOR RISE AND FALL TIMES

NOTES: A. C_L = 50 pF for TLC540 and 100 pF for TLC541.
B. t_{en} = t_{PZH} or t_{PZL}, t_{dis} = t_{PHZ} or t_{PLZ}.
C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.

principles of operation

The TLC540 and TLC541 are each complete data acquisition systems on a single chip. They include such functions as analog multiplexer, sample-and-hold, 8-bit A/D converter, data and control registers, and control logic. For flexibility and access speed, there are four control inputs [two clocks, chip select ($\overline{CS}$), and address]. These control inputs and a TTL-compatible 3-state output are intended for serial communications with a microprocessor or microcomputer. With judicious interface timing, with TLC540 a conversion can be completed in 9 microseconds, while complete input-conversion-output cycles can be repeated every 13 microseconds. With TLC541 a conversion can be completed in 17 microseconds, while complete input-conversion-output cycles are repeated every 25 microseconds. Furthermore, this fast conversion can be executed on any of 11 inputs or its built-in "self-test," and in any order desired by the controlling processor.

The System and I/O Clocks are normally used independently and do not require any special speed or phase relationships between them. This independence simplifies the hardware and software control tasks for the device. Once a clock signal within the specification range is applied to the System Clock input, the control hardware and software need only be concerned with addressing the desired analog channel, reading the previous conversion result, and starting the conversion by using the I/O Clock. The System Clock will drive the "conversion crunching" circuitry so that the control hardware and software need not be concerned with this task.

When $\overline{CS}$ is high, the Data Output pin is in a three-state condition and the Address Input and I/O Clock pins are disabled. This feature allows each of these pins, with the exception of the $\overline{CS}$ pin, to share a control logic point with their counterpart pins on additional A/D devices when additional TLC540/541 devices are used. In this way, the above feature serves to minimize the required control logic pins when using multiple A/D devices.

The control sequence has been designed to minimize the time and effort required to initiate conversion and obtain the conversion result. A normal control sequence is:

1. $\overline{CS}$ is brought low. To minimize errors caused by noise at the $\overline{CS}$ input, the internal circuitry waits for two rising edges and then a falling edge of the System Clock after a low $\overline{CS}$ transition, before the low transition is recognized. This technique is used to protect the device against noise when the device is used in a noisy environment. The MSB of the previous conversion result will automatically appear on the Data Out pin.
2. A new positive-logic multiplexer address is shifted in on the first four rising edges of the I/O Clock. The MSB of the address is shifted in first. The negative edges of these four I/O clock pulses shift out the second, third, fourth, and fifth most significant bits of the previous conversion result. The on-chip sample-and-hold begins sampling the newly addressed analog input after the fourth falling edge. The sampling operation basically involves the charging of internal capacitors to the level of the analog input voltage.
3. Three clock cycles are then applied to the I/O pin and the sixth, seventh, and eighth conversion bits are shifted out on the negative edges of these clock cycles.
4. The final eighth clock cycle is applied to the I/O Clock pin. The falling edge of this clock cycle completes the analog sampling process and initiates the hold function. Conversion is then performed during the next 36 System Clock cycles. After this final I/O Clock cycle, $\overline{CS}$ must go high or the I/O Clock must remain low for at least 36 System Clock cycles to allow for the conversion function.

$\overline{CS}$ can be kept low during periods of multiple conversion. Also, if $\overline{CS}$ is taken high it must remain high until the end of the conversion. Otherwise, a valid falling edge of $\overline{CS}$ will cause a reset condition, which will abort the conversion in progress.

A new conversion may be started and the ongoing conversion simultaneously aborted by performing steps 1 through 4 before the 36 System Clock cycles occur. Such action will yield the conversion result of the previous conversion and not the ongoing conversion.

principles of operation (continued)

It is possible to connect the System and I/O Clock pins together in special situations in which controlling circuitry points must be minimized. In this case, the following special points must be considered in addition to the requirements of the normal control sequence previously described.

1. When $\overline{CS}$ is recognized by the device to be at a low level, the common clock signal is used as an I/O Clock. When $\overline{CS}$ is recognized by the device to be at a high level, the common clock signal is used to drive the "conversion crunching" circuitry.
2. The device will recognize a $\overline{CS}$ low transition only when the $\overline{CS}$ input changes and subsequently the System Clock pin receives two positive edges and then a negative edge. For this reason, after a $\overline{CS}$ negative edge, the first two clock cycles will not shift in the address because a low $\overline{CS}$ must be recognized before the I/O Clock can shift in an analog channel address. Also, upon shifting in the address, $\overline{CS}$ must be raised after the sixth I/O Clock pulse that has been recognized by the device, so that a $\overline{CS}$ low level will be recognized upon the lowering of the eighth I/O Clock signal that is recognized by the device. Otherwise, additional common clock cycles will be recognized as I/O Clock pulses and will shift in an erroneous address.

For certain applications, such as strobing applications, it is necessary to start conversion at a specific point in time. This device will accommodate these applications. Although the on-chip sample-and-hold begins sampling upon the negative edge of the fourth I/O Clock cycle, the hold function is not initiated until the negative edge of the eighth I/O Clock cycle. Thus, the control circuitry can leave the I/O Clock signal in its high state during the eighth I/O Clock cycle until the moment at which the analog signal must be converted. The TLC540/TLC541 will continue sampling the analog input until the eighth falling edge of the I/O Clock. The control circuitry or software will then immediately lower the I/O Clock signal and hold the analog signal at the desired point in time and start conversion.

Detailed information on interfacing to most popular microprocessors is readily available from the factory.

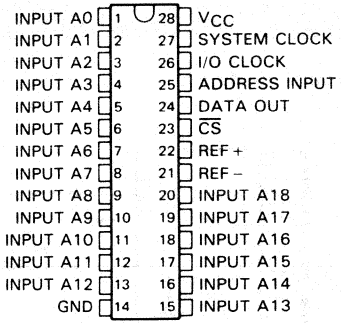
TLC545M, TLC545I, TLC546M, TLC546I
LinCMOS™ 8-BIT ANALOG-TO-DIGITAL PERIPHERALS WITH SERIAL CONTROL AND 19 INPUTS

D2850, DECEMBER 1985

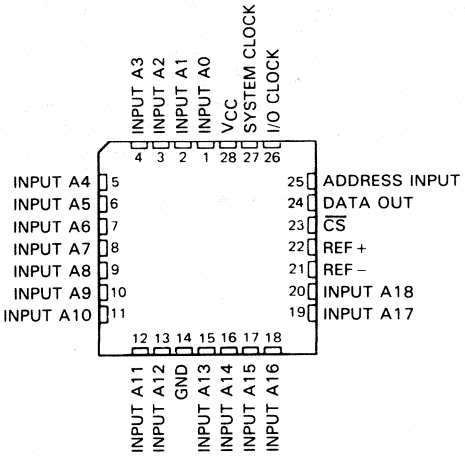
- **LinCMOS™ Technology**
- **8-Bit Resolution A/D Converter**
- **Microprocessor Peripheral or Stand-Alone Operation**
- **On-Chip 20-Channel Analog Multiplexer**
- **Built-In Self-Test Mode**
- **Software-Controllable Sample and Hold**
- **Total Unadjusted Error . . . ±0.5 LSB Max**
- **Timing and Control Signals Compatible with 8-Bit TLC540 and 10-Bit TLC1540 A/D Converter Families**

TYPICAL PERFORMANCE	TL545	TL546
Channel Acquisition Time	1.5 μs	2.7 μs
Conversion Time	9 μs	17 μs
Sampling Rate	76 × 10^3	40 × 10^3
Power Dissipation	6 mW	6 mW

N DUAL-IN-LINE PACKAGE
(TOP VIEW)



FN CHIP CARRIER PACKAGE
(TOP VIEW)



description

The TLC545 and TLC546 are LinCMOS™ A/D peripherals built around an 8-bit switched-capacitor successive-approximation A/D converter. They are designed for serial interface to a microprocesor or peripheral via a three-state output with up to four control inputs [including independent System Clock, I/O Clock, Chip Select ($\overline{CS}$), and Address Input]. A 4-megahertz system clock for the TLC545 and a 2.1-megahertz system clock for the TLC546 with a design that includes simultaneous read/write operation allow high-speed data transfers and sample rates of up to 76,923 samples per second for the TLC545, and 40,000 samples per second for the TLC546. In addition to the high-speed converter and versatile control logic, there is an on-chip 20-channel analog multiplexer that can be used to sample any one of 19 inputs or an internal "self-test" voltage, and a sample-and-hold that can operate automatically or under microprocessor control.

The converters incorporated in the TLC545 and TLC546 feature differential high-impedance reference inputs that facilitate ratiometric conversion, scaling, and analog circuitry isolation from logic and supply noises. A totally switched-capacitor design allows guaranteed low-error (±0.5 LSB) conversion in 9 microseconds for

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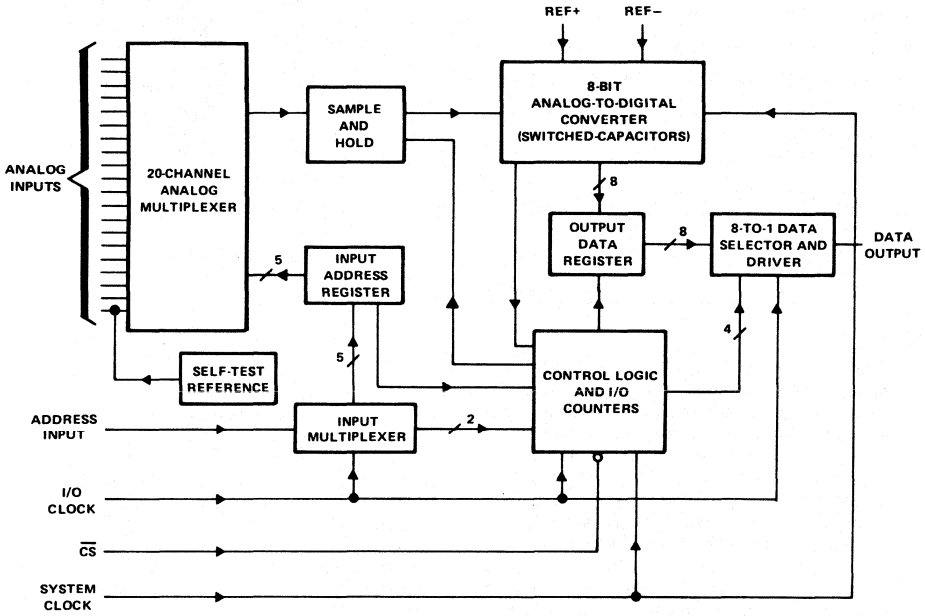
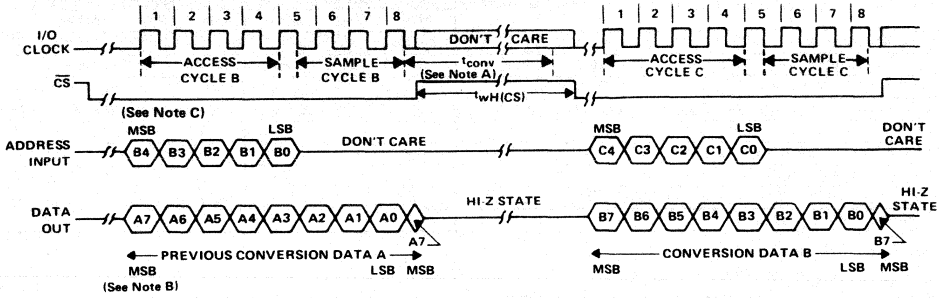
the TLC545, and 17 microseconds for the TLC546 over the full operating temperature range. Detailed information on interfacing to most popular microprocessors is readily available from the factory.

The TLC545M and the TLC546M are characterized for operation from −55°C to 125°C. The TLC545I and the TLC546I are characterized for operation from −40°C to 85°C.

functional block diagram



operating sequence



NOTES: A. The conversion cycle, which requires 36 system clock periods, is initiated with the 8th I/O clock↓ after CS↓ for the channel whose address exists in memory at that time.

B. The most significant bit (MSB) will automatically be placed on the DATA OUT bus after $\overline{CS}$ is brought low. The remaining seven bits (A6-A0) will be clocked out on the first seven I/O clock falling edges.

C. To minimize errors caused by noise at the $\overline{CS}$ input, the internal circuitry waits for three system clock cycles (or less) after a chip select transition before responding to control input signals. Therefore, no attempt should be made to clock-in address data until the minimum chip-select setup time has elapsed.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1)	6.5 V
Input voltage range (any input)	−0.3 V to V_{CC} +0.3 V
Output voltage range	−0.3 V to V_{CC} +0.3 V
Peak input current range (any input)	±10 mA
Peak total input current (all inputs)	±30 mA
Operating free-air temperature range: TLC545I, TLC546I	−40°C to 85°C
TLC545M, TLC546M	−55°C to 125°C
Storage temperature range	−65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	260°C

NOTE 1: All voltage values are with respect to network ground terminal.

recommended operating conditions

			TLC545			TLC546			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}			4.75	5	5.5	4.75	5	5.5	V
Positive reference voltage, V_{REF+} (see Note 2)			2.5	V_{CC}	$V_{CC}+0.1$	2.5	V_{CC}	$V_{CC}+0.1$	V
Negative reference voltage, V_{ref-} (see Note 2)			−0.1	0	$V_{CC}-2.5$	−0.1	0	$V_{CC}-2.5$	V
Differential reference voltage, $V_{REF+} - V_{REF-}$ (see Note 2)			1	V_{CC}	$V_{CC}+0.2$	1	V_{CC}	$V_{CC}+0.2$	V
Analog input voltage (see Note 2)			0		V_{CC}	0		V_{CC}	V
High-level control input voltage, V_{IH}			2			2			V
Low-level control input voltage, V_{IL}					0.8			0.8	V
Setup time, address bits at data input before I/O CLK↑, $t_{su(A)}$			200			400			ns
Address hold time, t_h			0			0			ns
Setup time, $\overline{CS}$ low before clocking in first address bit, $t_{su(CS)}$ (see Note 3)			3			3			System clock cycles
Chip select high during conversion, $t_{wH(CS)}$			36			36			System clock cycles
Input/Output clock frequency, $f_{CLK(I/O)}$			0		2.048	0		1.1	MHz
System clock frequency, $f_{CLK(SYS)}$			$f_{CLK(I/O)}$		4	$f_{CLK(I/O)}$		2.1	MHz
System clock high, $t_{wH(SYS)}$			110			210			ns
System clock low, $t_{wL(SYS)}$			100			190			ns
Input/Output clock high, $t_{wH(I/O)}$			200			404			ns
Input/Output clock low, $t_{wL(I/O)}$			200			404			ns
Clock transition time (see Note 4)	System	$f_{CLK(SYS)} \leq 1048$ kHz			30			30	ns
		$f_{CLK(SYS)} > 1048$ kHz			20			20	
	I/O	$f_{CLK(I/O)} \leq 525$ kHz			100			100	ns
		$f_{CLK(I/O)} > 525$ kHz			40			40	
Operating free-air temperature, T_A		TLC545M, TLC546M	−55		125	−55		125	°C
		TLC545I, TLC546I	−40		85	−40		85	

NOTES: 2. Analog input voltages greater than that applied to REF+ convert as all "1"s (11111111), while input voltages less than that applied to REF− convert as all "0"s (00000000). For proper operation, REF+ voltage must be at least 1 volt higher than REF− voltage. Also, total unadjusted errors may increase as this differential reference voltage falls below 4.75 volts.

3. To minimize errors caused by noise at the Chip Select input, the internal circuitry waits for three system clock cycles (or less) after a chip select falling edge or rising edge is detected before responding to control input signals. Therefore, no attempt should be made to clock-in address data until the minimum chip select setup time has elapsed.

4. This is the time required for the clock input signal to fall from V_{IH} min to V_{IL} max or to rise from V_{IL} max to V_{IH} min. In the vicinity of normal room temperature, the devices function with input clock transition time as slow as 2 microseconds for remote data acquisition applications where the sensor and the A/D converter are placed several feet away from the controlling microprocessor.

electrical characteristics over recommended operating temperature range, V_{CC} = V_{REF+} = 4.75 V to 5.5 V (unless otherwise noted), $f_{CLK(I/O)}$ = 2.048 MHz for TLC545 or $f_{CLK(I/O)}$ = 1.1 MHz for TLC546

PARAMETER			TEST CONDITIONS	MIN	TYP†	MAX	UNIT
V_{OH}	High-level output voltage (pin 24)		V_{CC} = 4.75 V, I_{OH} = 360 μA	2.4			V
V_{OL}	Low-level output voltage		V_{CC} = 4.75 V, I_{OL} = 3.2 mA			0.4	V
I_{OZ}	Off-state (high-impedance state) output current		V_O = V_{CC}, $\overline{CS}$ at V_{CC}			10	μA
			V_O = 0, $\overline{CS}$ at V_{CC}			−10	
I_{IH}	High-level input current		V_I = V_{CC}		0.005	2.5	μA
I_{IL}	Low-level input current		V_I = 0		−0.005	−2.5	μA
I_{CC}	Operating supply current		$\overline{CS}$ at 0 V		1.2	2.5	mA
	Selected channel leakage current		Selected channel at V_{CC}, Unselected channel at 0 V		0.4	1	μA
			Selected channel at 0 V, Unselected channel at V_{CC}		−0.4	−1	
I_{CC} + I_{REF}	Supply and reference current		V_{REF+} = V_{CC}, $\overline{CS}$ at 0 V		1.3	3	mA
C_i	Input capacitance	Analog inputs			7	55	pF
		Control inputs			5	15	

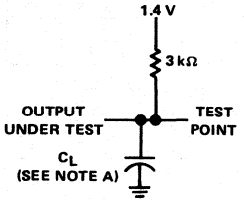
†All typical values are at T_A = 25°C.

operating characteristics over recommended operating free-air temperature range, V_{CC} = V_{REF+} = 4.75 V to 5.5 V, $f_{CLK(I/O)}$ = 2.048 MHz for TLC545 or 1.1 MHz for TLC546, $f_{CLK(SYS)}$ = 4 MHz for TLC545 or 2.1 MHz for TLC546

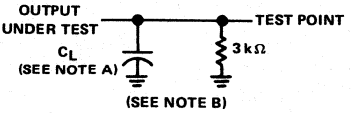
PARAMETER		TEST CONDITIONS	TLC545			TLC546			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
	Linearity error	See Note 5			±0.5			±0.5	LSB
	Zero error	See Note 6			±0.5			±0.5	LSB
	Full-scale error	See Note 6			±0.5			±0.5	LSB
	Total unadjusted error	See Note 7			±0.5			±0.5	LSB
	Self-test output code	Input A19 address = 10011 (See Note 8)	01111101 (125)		10000011 (131)	01111101 (125)		10000011 (131)	
t_{conv}	Conversion time	See Operating Sequence			9			17	μs
	Total access and conversion time	See Operating Sequence			13			25	μs
t_{acq}	Channel acquisition time (sample cycle)	See Operating Sequence			3			3	I/O clock cycles
t_v	Time output data remains valid after I/O clock↓		10			10			ns
t_d	Delay time, I/O clock↓ to data output valid	See Parameter Measurement Information			300			400	ns
t_{en}	Output enable time				150			150	ns
t_{dis}	Output disable time				150			150	ns
$t_{r(bus)}$	Data bus rise time				300			300	ns
$t_{f(bus)}$	Data bus fall time				300			300	ns

NOTES: 5. Linearity error is the maximum deviation from the best straight line through the A/D transfer characteristics.
6. Zero error is the difference between 00000000 and the converted output for zero input voltage; full-scale error is the difference between 11111111 and the converted for full-scale input voltage.
7. Total unadjusted error is the sum of linearity, zero, and full-scale errors.
8. Both the input address and the output codes are expressed in positive logic. The A19 analog input signal is internally generated and is used for test purposes.

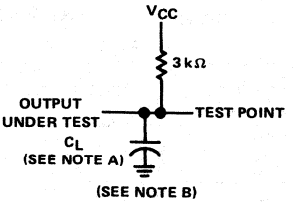
PARAMETER MEASUREMENT INFORMATION



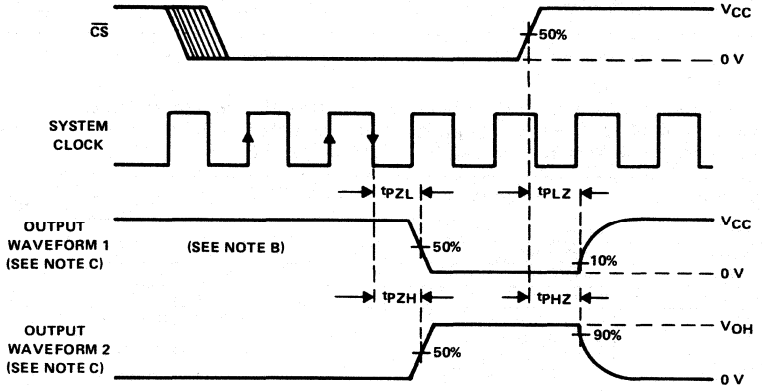
LOAD CIRCUIT FOR t_d, t_r, AND t_f



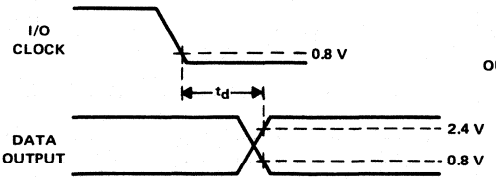
LOAD CIRCUIT FOR t_{PZH} AND t_{PHZ}



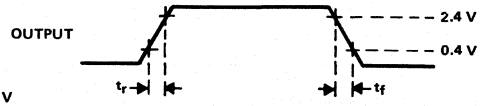
LOAD CIRCUIT FOR t_{PZL} AND t_{PLZ}



VOLTAGE WAVEFORMS FOR ENABLE AND DISABLE TIMES



VOLTAGE WAVEFORM FOR DELAY TIME



VOLTAGE WAVEFORM FOR RISE AND FALL TIMES

NOTES: A. C_L = 50 pF for TLC545 and 100 pF for TLC546
B. t_{en} = t_{PZH} or t_{PZL}, t_{dis} = t_{PHZ} or t_{PLZ}
C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.

principles of operation

The TLC545 and TLC546 are both complete data acquisition systems on single chips. Each includes such functions as system clock, sample-and-hold, 8-bit A/D converter, data and control registers, and control logic. For flexibility and access speed, there are four control inputs; Chip Select ($\overline{CS}$), Address Input, I/O clock, and System clock. These control inputs and a TTL-compatible 3-state output facilitate serial communications with a microprocessor or microcomputer. The TLC545 and TLC546 can complete conversions in a maximum of 9 and 17 microseconds respectively, while complete input-conversion-output cycles can be repeated at a mixmum of 13 and 25 microseconds, respectively.

The System and I/O clocks are normally used independently and do not require any special speed or phase relationships between them. This independence simplifies the hardware and software control tasks for the device. Once a clock signal within the specification range is applied to the System clock input, the control hardware and software need only be concerned with addressing the desired analog channel, reading the previous conversion result, and starting the conversion by using the I/O clock. The System clock will drive the "conversion crunching" circuitry so that the control hardware and software need not be concerned with this task.

When $\overline{CS}$ is high, the Data Output pin is in a high-impedance condition, and the Address Input and I/O Clock pins are disabled. This feature allows each of these pins, with the exception of the $\overline{CS}$, to share a control logic point with their counterpart pins on additional A/D devices when additional TLC545/TLC546 devices are used. Thus, the above feature serves to minimize the required control logic pins when using multiple A/D devices.

The control sequence has been designed to minimize the time and effort required to initiate conversion and obtain the conversion result. A normal control sequence is:

1. $\overline{CS}$ is brought low. To minimize errors caused by noise at the $\overline{CS}$ input, the internal circuitry waits for two rising edges and then a falling edge of the System clock after a $\overline{CS}$ transition before the transition is recognized. The MSB of the previous conversion result will automatically appear on the Data Out pin.
2. A new positive-logic multiplexer address is shifted in on the first five rising edges of the I/O clock. The MSB of the address is shifted in first. The negative edges of these five I/O clocks shift out the 2nd, 3rd, 4th, 5th, and 6th most significant bits of the previous conversion result. The on-chip sample-and hold begins sampling the newly addressed analog input after the 5th falling edge. The sampling operation basically involves the charging of internal capacitors to the level of the analog input voltage.
3. Two clock cycles are then applied to the I/O pin and the 7th and 8th conversion bits are shifted out on the negative edges of these clock cycles.
4. The final 8th clock cycle is applied to the I/O clock pin. The falling edge of this clock cycle completes the analog sampling process and initiates the hold function. Conversion is then performed during the next 36 system clock cycles. After this final I/O clock cycle, $\overline{CS}$ must go high or the I/O clock must remain low for at least 36 system clock cycles to allow for the conversion function.

   $\overline{CS}$ can be kept low during periods of multiple conversion. Also, if $\overline{CS}$ is taken high, it must remain high until the end of conversion. Otherwise, a valid falling edge of $\overline{CS}$ will cause a reset condition, which will abort the conversion in progress.

A new conversion may be started and the ongoing conversion simultaneously aborted by performing steps 1 through 4 before the 36 system clock cycles occur. Such action will yield the conversion result of the previous conversion and not the ongoing conversion.

It is possible to connect the system and I/O clocks together in special situations in which controlling circuitry points must be minimized. In this case, the following special points must be considered in addition to the requirements of the normal control sequence previously described.

1. When $\overline{CS}$ is recognized by the device to be at a low level, the common clock signal is used as an I/O clock. When the $\overline{CS}$ is recognized by the device to be at a high level, the common clock signal is used to drive the "conversion crunching" circuitry.
2. The device will recognize a $\overline{CS}$ transition only when the $\overline{CS}$ input changes and subsequently the system clock pin receives two positive edges and then a negative edge. For this reason, after a $\overline{CS}$ negative edge, the first two clock cycles will not shift in the address because a low $\overline{CS}$ must be recognized before the I/O clock can shift in an analog channel address. Also, upon shifting in the address, $\overline{CS}$ must be raised after the 6th I/O clock, which has been recognized by the device, so that a $\overline{CS}$ low level will be recognized upon the lowering of the 8th I/O clock signal recognized by the device. Otherwise, additional common clock cycles will be recognized as I/O clocks and will shift in an erroneous address.

For certain applications, such as strobing applications, it is necessary to start conversion at a specific point in time. This device will accommodate these applications. Although the on-chip sample-and-hold begins sampling upon the negative edge of the 5th I/O clock cycle, the hold function is not initiated until the negative edge of the 8th I/O clock cycle. Thus, the control circuitry can leave the I/O clock signal in its high state during the 8th I/O clock cycle, until the moment at which the analog signal must be converted. The TLC545/546 will continue sampling the analog input until the 8th falling edge of the I/O clock. The control circuitry or software must then immediately lower the I/O clock signal to initiate the hold function at the desired point in time and to start conversion.

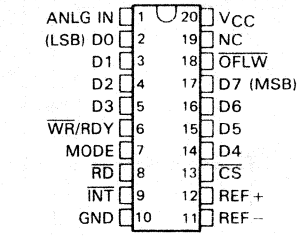
Detailed information on interfacing to most popular microprocesors is readily available from the factory.

ADVANCED LinCMOS™ HIGH-SPEED 8-BIT ANALOG-TO-DIGITAL CONVERTERS USING MODIFIED "FLASH" TECHNIQUES

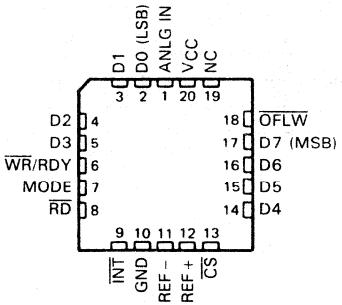
D2873, SEPTEMBER 1986 – REVISED DECEMBER 1987

- **Advanced LinCMOS™ Silicon-Gate Technology**
- **8-Bit Resolution**
- **Differential Reference Inputs**
- **Parallel Microprocessor Interface**
- **Conversion and Access Time Over Temperature Range**
  Write-Read Mode . . . 1.18 μs and 1.92 μs
  Read Mode . . . 2.6 μs Max
- **No External Clock or Oscillator Components Required**
- **On-Chip Track-and-Hold**
- **Low Power Consumption . . . 50 mW Typ**
- **Single 5-V Supply**
- **TLC0820B is Direct Replacement for National Semiconductor ADC0820B/BC and Analog Devices AD7820L/C/U; TLC0820A is Direct Replacement for National Semiconductor ADC0820C/CC and Analog Devices AD7820K/B/T**

TLC0820AM, TLC0820BM . . . DW, J OR N PACKAGE
TLC0820AI, TLC0820BI . . . DW OR N PACKAGE
TLC0820AC, TLC0820BC . . . DW OR N PACKAGE
(TOP VIEW)



TLC0820AM, TLC0820BM . . . FK PACKAGE
TLC0820AI, TLC0820BI . . . FN PACKAGE
TLC0820AC, TLC0820BC . . . FN PACKAGE
(TOP VIEW)



NC – No internal connection

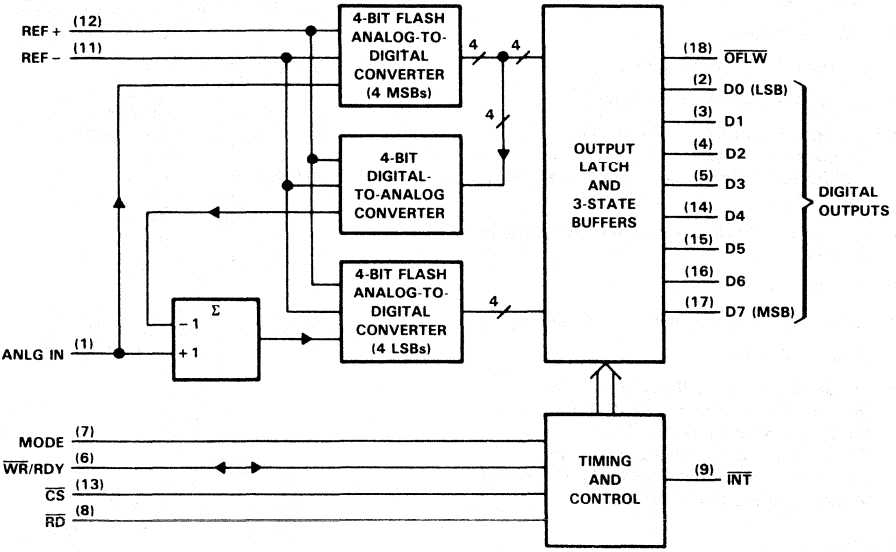
description

The TLC0820A and TLC0820B are Advanced LinCMOS™ 8-bit analog-to-digital converters each consisting of two 4-bit "flash" converters, a 4-bit digital-to-analog converter, a summing (error) amplifier, control logic, and a result latch circuit. The modified "flash" technique allows low-power integrated circuitry to complete an 8-bit conversion in 1.18 microseconds over temperature. The on-chip track-and-hold circuit has a 100-nanosecond sample window and allows the TLC0820A and TLC0820B to convert continuous analog signals having slew rates of up to 100 millivolts per microsecond without external sampling components. TTL-compatible three-state output drivers and two modes of operation allow interfacing to a variety of microprocessors. Detailed information on interfacing to most popular microprocessors is readily available from the factory.

The TLC0820AM and TLC0820BM are available in the DW or N plastic and the J ceramic packages and are characterized for operation over the full military temperature range of −55°C to 125°C. The TLC0820AI and TLC0820BI are characterized for operation from −40°C to 85°C. The TLC0820AC and TLC0820BC are characterized for operation from 0°C to 70°C.

Advanced LinCMOS is a trademark of Texas Instruments Incorporated.

functional block diagram



PIN NAME	PIN NUMBER	DESCRIPTION
ANLG IN	1	Analog input
$\overline{CS}$	13	This input must be low in order for $\overline{RD}$ or $\overline{WR}$ to be recognized by the ADC.
D0	2	Three-state data output, bit 1 (LSB)
D1	3	Three-state data output, bit 2
D2	4	Three-state data output, bit 3
D3	5	Three-state data output, bit 4
D4	14	Three-state data output, bit 5
D5	15	Three-state data output, bit 6
D6	16	Three-state data output, bit 7
D7	17	Three-state data output, bit 8 (MSB)
GND	10	Ground
$\overline{INT}$	9	In the WRITE-READ mode, the interrupt output, $\overline{INT}$, going low indicates that the internal count-down delay time, $t_{d(int)}$, is complete and the data result is in the output latch. $t_{d(int)}$ is typically 800 ns starting after the rising edge of the $\overline{WR}$ input (see operating characteristics and Figure 3). If $\overline{RD}$ goes low prior to the end of $t_{d(int)}$, $\overline{INT}$ goes low at the end of t_{dRIL} and the conversion results are available sooner (see Figure 2). $\overline{INT}$ is reset by the rising edge of either $\overline{RD}$ or $\overline{CS}$.
MODE	7	Mode-selection input. It is internally tied to GND through a 50-uA current source, which acts like a pull-down resistor. READ mode: Occurs when this input is low. WRITE-READ mode: Occurs when this input is high.
NC	19	No internal connection
$\overline{OFLW}$	18	Normally the $\overline{OFLW}$ output is a logical high. However, if the analog input is higher than the V_{REF+}, $\overline{OFLW}$ will be low at the end of conversion. It can be used to cascade 2 or more devices to improve resolution (9 or 10-bits).
$\overline{RD}$	8	In the WRITE-READ mode with $\overline{CS}$ low, the 3-state data outputs D0 through D7 are activated when $\overline{RD}$ goes low. $\overline{RD}$ can also be used to increase the conversion speed by reading data prior to the end of the internal count-down delay time. As a result, the data transferred to the output latch is latched after the falling edge of $\overline{RD}$. In the READ mode with $\overline{CS}$ low, the conversion starts with $\overline{RD}$ going low. $\overline{RD}$ also enables the three-state data outputs upon completion of the conversion. The RDY output going into the high-impedance state and $\overline{INT}$ going low indicates completion of the conversion.
REF−	11	This input voltage is placed on the bottom of the resistor ladder.
REF+	12	This input voltage is placed on the top of the resistor ladder.
V_{CC}	20	Power supply voltage
$\overline{WR}$/RDY	6	In the WRITE-READ mode with $\overline{CS}$ low, the conversion is started on the falling edge of the $\overline{WR}$ input signal. The result of the conversion is strobed into the output latch after the internal count-down delay time, $t_{d(int)}$, provided that the $\overline{RD}$ input does not go low prior to this time. $t_{d(int)}$ is approximately 800 ns. In the READ mode, RDY (an open-drain output) will go low after the falling edge of $\overline{CS}$, and will go into the high-impedance state when the conversion is strobed into the output latch. It is used to simplify the interface to a microprocessor system.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

	TLC0820AM TLC0820BM	TLC0820AI TLC0820BI	TLC0820AC TLC0820BC	UNIT
Supply voltage, V_{CC} (see Note 1)	10	10	10	V
Input voltage range, all inputs (see Note 1)	−0.2 to V_{CC}+0.2	−0.2 to V_{CC}+0.2	−0.2 to V_{CC}+0.2	V
Output voltage range, all outputs (see Note 1)	−0.2 to V_{CC}+0.2	−0.2 to V_{CC}+0.2	−0.2 to V_{CC}+0.2	V
Operating free-air temperature range	−55 to 125	−40 to 85	0 to 70	°C
Storage temperature range	−65 to 150	−65 to 150	−65 to 150	°C
Case temperature for 60 seconds: FK package	260			°C
Case temperature for 10 seconds: FN package		260	260	°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds: J package	300			°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: DW or N package	260	260	260	°C

NOTE 1: All voltages are with respect to network ground terminal, pin 10.

recommended operating conditions

			TLC0820AM TLC0820BM			TLC0820AI TLC0820BI			TLC0820AC TLC0820BC			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}			4.5	5	8	4.5	5	8	4.5	5	8	V
Analog input voltage			−0.1		V_{CC}+0.1	−0.1		V_{CC}+0.1	−0.1		V_{CC}+0.1	V
Positive reference voltage, V_{REF+}			V_{REF-}		V_{CC}	V_{REF-}		V_{CC}	V_{REF-}		V_{CC}	V
Negative reference voltage, V_{REF-}			GND		V_{REF+}	GND		V_{REF+}	GND		V_{REF+}	V
High-level input voltage, V_{IH}	V_{CC} = 4.75 V to 5.25 V	$\overline{CS}$, $\overline{WR}$/RDY, $\overline{RD}$	2			2			2			V
		MODE	3.5			3.5			3.5			
Low-level input voltage, V_{IL}	V_{CC} = 4.75 V to 5.25 V	$\overline{CS}$, $\overline{WR}$/RDY, $\overline{RD}$			0.8			0.8			0.8	V
		MODE			1.5			1.5			1.5	
Delay to next conversion, $t_{d(NC)}$ (see Figures 1, 2, 3, and 4)			500			500			500			ns
Delay time from $\overline{WR}$ to $\overline{RD}$ in write-read mode, t_{dWR} (see Figure 2)			0.4			0.4			0.4			μs
Write-pulse duration in write-read mode, t_{wW} (see Figures 2, 3, and 4)			0.5		50	0.5		50	0.5		50	μs
Operating free-air temperature, T_A			−55		125	−40		85	0		70	°C

electrical characteristics over recommended operating free-air temperature range, V_{CC} = 5 V (unless otherwise noted)

PARAMETER			TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{OH}	High-level output voltage	Any D, $\overline{INT}$, or $\overline{OFLW}$	V_{CC} = 4.75 V,	I_{OH} = −360 μA	2.4			V
			V_{CC} = 4.75 V,	I_{OH} = −10 μA	4.5			
V_{OL}	Low-level output voltage	Any D, $\overline{OFLW}$, $\overline{INT}$, or $\overline{WR}$/RDY	V_{CC} = 5.25 V,	I_{OL} = 1.6 mA			0.4	V
I_{IH}	High-level input current	$\overline{CS}$ or $\overline{RD}$	V_{IH} = 5 V			0.005	1	μA
		$\overline{WR}$/RDY				0.1	3	
		MODE				50	200	
I_{IL}	Low-level input current	$\overline{CS}$, $\overline{WR}$/RDY, $\overline{RD}$, or MODE	V_{IL} = 0			−0.005	−1	μA
I_{OZ}	Off-state (high-impedance state) output current	Any D or $\overline{WR}$/RDY	V_O = 5 V			0.1	3	μA
			V_O = 0			−0.1	−3	
I_I	Analog input current		$\overline{CS}$ at 5 V,	V_I = 5 V			3	μA
			$\overline{CS}$ at 5 V,	V_I = 0			−3	
I_{OS}	Short-circuit output current	Any D, $\overline{OFLW}$, $\overline{INT}$, or $\overline{WR}$/RDY	V_O = 5 V		7	14		mA
		Any D or $\overline{OFLW}$	V_O = 0		−6	−12		
		$\overline{INT}$			−4.5	−9		
R_{ref}	Reference resistance				1.25	2.3	6	kΩ
I_{CC}	Supply current		$\overline{CS}$, $\overline{WR}$/RDY, and $\overline{RD}$ at 0 V			7.5	15	mA
C_i	Input capacitance	Any digital				5		pF
		Analog (pin 1)				45		
C_o	Output capacitance	Any digital					5	pF

† All typical values are at T_A = 25°C.

operating characteristics, V_{CC} = 5 V, V_{REF+} = 5 V, V_{REF-} = 0, $t_r = t_f$ = 20 ns, T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS		TLC0820A			TLC0820B			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
k_{SVS}	Supply voltage sensitivity	V_{CC} = 5 V ± 5%, T_A = MIN to MAX			±1/16	±1/4		±1/16	±1/4	LSB
	Total unadjusted error†	MODE pin at 0 V, T_A = MIN to MAX				1			1/2	LSB
t_{convR}	Read mode conversion time	MODE pin at 0 V, See Figure 1			1.6	2.5		1.6	2.5	μs
$t_{d(int)}$	Internal count-down delay time	MODE pin at 5 V, See Figures 3 and 4	C_L = 50 pF,		800	1300		800	1300	ns
t_{aR}	Access time from $\overline{RD}$↓	MODE pin at 0 V, See Figure 1			t_{convR} +20	t_{convR} +50		t_{convR} +20	t_{convR} +50	ns
t_{aR1}	Access time from $\overline{RD}$↓	MODE pin at 5 V, $t_{dWR} < t_{d(int)}$, See Figure 2	C_L = 15 pF		190	280		190	280	ns
			C_L = 100 pF		210	320		210	320	
t_{aR2}	Access time from $\overline{RD}$↓	MODE pin at 5 V, $t_{dWR} > t_{d(int)}$ See Figure 3	C_L = 15 pF		70	120		70	120	ns
			C_L = 100 pF		90	150		90	150	
t_{aINT}	Access time from $\overline{INT}$↓	MODE pin at 5 V, See Figure 4			20	50		20	50	ns
t_{dis}	Disable time from $\overline{RD}$↑	R_L = 1 kΩ, See Figures 1, 2, 3, and 5	C_L = 10 pF,		70	95		70	95	ns
t_{dRDY}	Delay time from $\overline{CS}$↓ to RDY↓	MODE pin at 0 V, See Figure 1	C_L = 50 pF,		50	100		50	100	ns
t_{dRIH}	Delay time from $\overline{RD}$↑ to $\overline{INT}$↑	C_L = 50 pF, See Figures 1, 2, and 3			125	225		125	225	ns
t_{dRIL}	Delay time from $\overline{RD}$↓ to $\overline{INT}$↓	MODE pin at 5 V, See Figure 2	$t_{dWR} < t_{d(int)}$,		200	290		200	290	ns
t_{dWIH}	Delay time from $\overline{WR}$↑ to $\overline{INT}$↑	MODE pin at 5 V, See Figure 4	C_L = 50 pF,		175	270		175	270	ns
	Slew rate tracking				0.1			0.1		V/μs

† Total unadjusted error includes offset, full-scale, and linearity errors.

PARAMETER MEASUREMENT INFORMATION

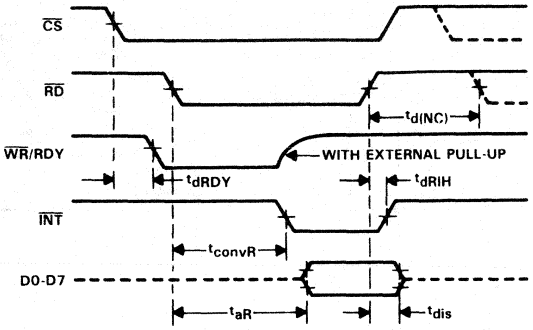


FIGURE 1. READ MODE WAVEFORMS (MODE PIN LOW)

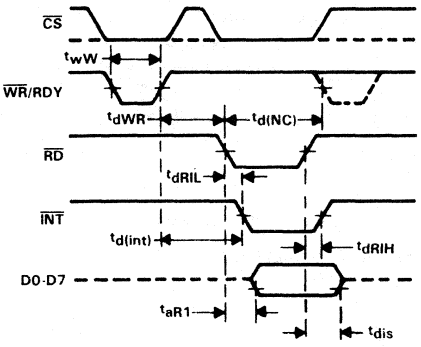


FIGURE 2. WRITE-READ MODE WAVEFORMS
[MODE PIN HIGH AND $t_{dWR} < t_{d(int)}$]

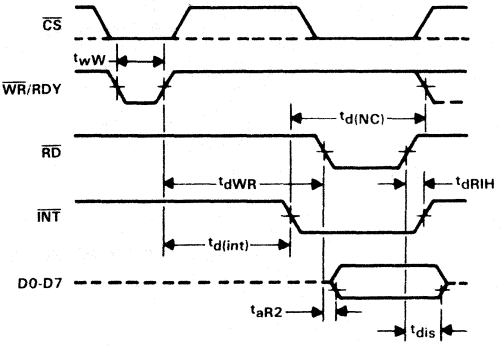


FIGURE 3. WRITE-READ WAVEFORMS
[MODE PIN HIGH AND $t_{dWR} > t_{d(int)}$]

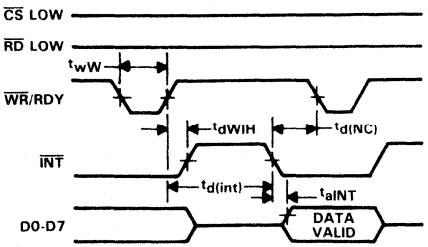


FIGURE 4. WRITE-READ MODE WAVEFORMS
(STAND-ALONE OPERATION, MODE PIN HIGH, AND RD LOW)

PARAMETER MEASUREMENT INFORMATION

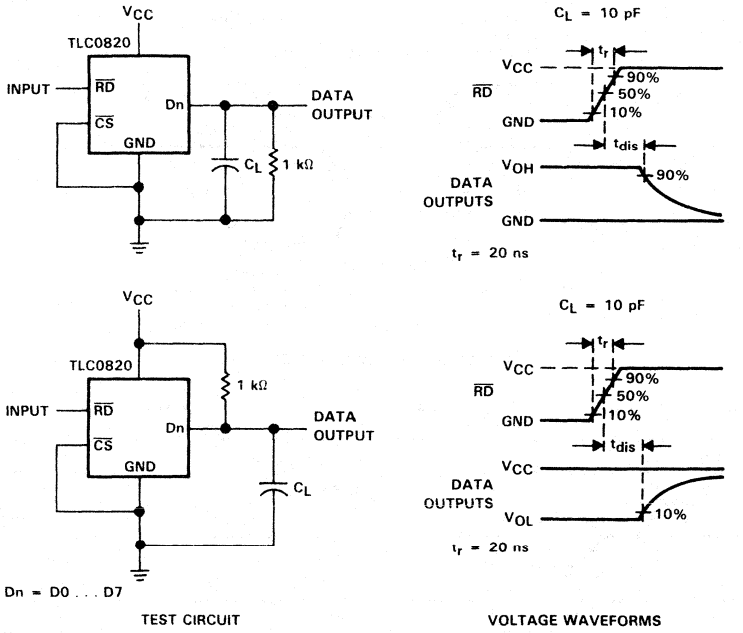


FIGURE 5. TEST CIRCUIT AND VOLTAGE WAVEFORMS

PRINCIPLES OF OPERATION

The TLC0820A and TLC0820B each employ a combination of "sampled-data" comparator techniques and "flash" techniques common to many high-speed converters. Two 4-bit "flash" analog-to-digital conversions are used to give a full 8-bit output.

The recommended analog input voltage range for conversion is -0.1 V to $V_{CC}+0.1$ V. Analog input signals that are less than V_{REF-} + ½ LSB or greater than V_{REF+} − ½ LSB convert to 00000000 or 11111111 respectively. The reference inputs are fully differential with common-mode limits defined by the supply rails. The reference input values define the full-scale range of the analog input. This allows the gain of the ADC to be varied for ratiometric conversion by changing the V_{REF+} and V_{REF-} voltages.

The device operates in two modes, read (only) and write-read, which are selected by the MODE pin (pin 7). The converter is set to the read (only) mode when pin 7 is low. In the read mode, the $\overline{WR}$/RDY pin is used as an output and is referred to as the "ready" pin. In this mode, a low on the "ready" pin while $\overline{CS}$ is low indicates that the device is busy. Conversion starts on the falling edge of $\overline{RD}$ and is completed no more than 2.5 microseconds later when $\overline{INT}$ falls and the "ready" pin returns to a high-impedance state. Data outputs also change from high-impedance to active states at this time. After the data is read, $\overline{RD}$ is taken high, $\overline{INT}$ returns high, and the data outputs return to their high-impedance states.

The converter is set to the write-read mode when pin 7 is high and $\overline{WR}$/RDY is referred to as the "write" pin. Taking $\overline{CS}$ and the "write" pin low selects the converter and initiates measurement of the input signal. Approximately 600 nanoseconds after the "write" pin returns high, the conversion is completed. Conversion starts on the rising edge of $\overline{WR}$/RDY in the write-read mode.

The high-order 4-bit "flash" ADC measures the input by means of 16 comparators operating simultaneously. A high precision 4-bit DAC then generates a discrete analog voltage from the result of that conversion. After a time delay, a second bank of comparators does a low-order conversion on the analog difference between the input level and the high-order DAC output. The results from each of these conversions enter an 8-bit latch and are output to the three-state buffers on the falling edge of $\overline{RD}$.

TYPICAL APPLICATION DATA

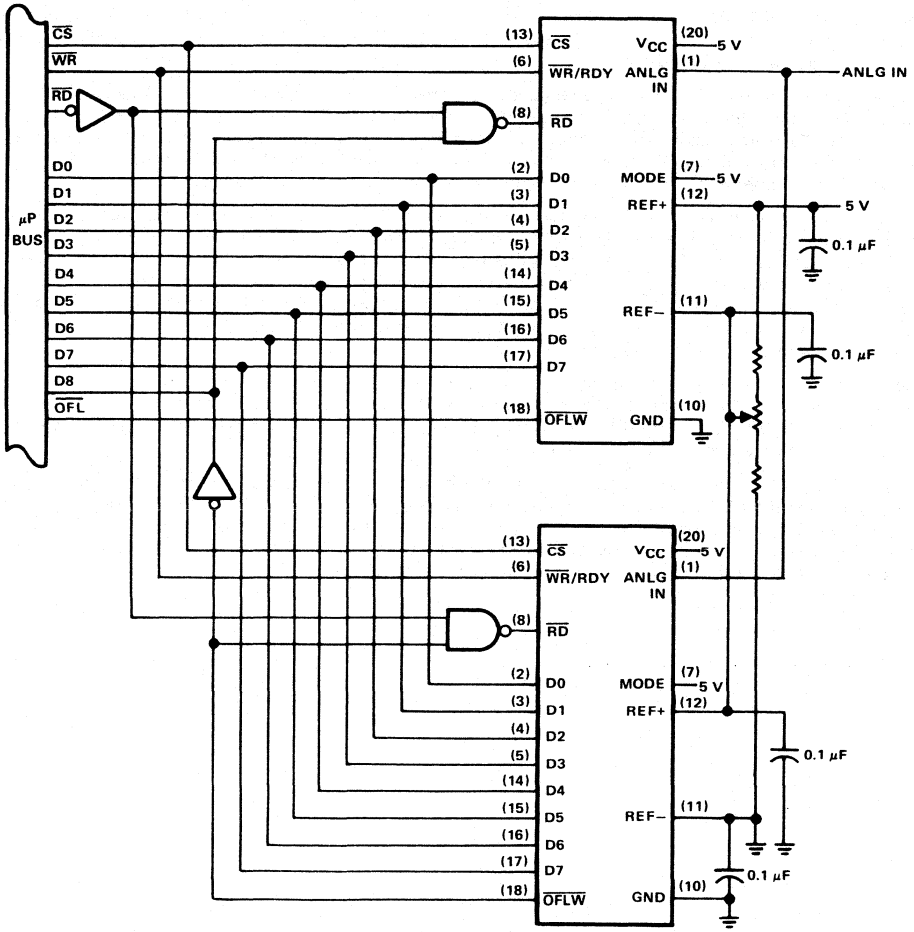
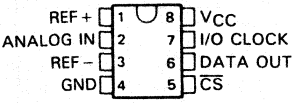


FIGURE 6. CONFIGURATION FOR 9-BIT RESOLUTION

- LinCMOS™ Technology
- Microprocessor Peripheral or Stand-Alone Operation
- 8-Bit Resolution A/D Converter
- Differential Reference Input Voltages
- Conversion Time . . . 17 μs Max
- Total Access and Conversion Cycles Per Second
  TLC548 . . . up to 45,500
  TLC549 . . . up to 40,000
- On-Chip Software-Controllable Sample-and-Hold
- Total Unadjusted Error . . . ±0.5 LSB Max
- 4-MHz Typical Internal System Clock
- Wide Supply Range . . . 3 V to 6 V
- Low Power Consumption . . . 6 mW Typ
- Ideal for Cost-Effective, High-Performance Applications Including Battery-Operated Portable Instrumentation
- Pinout and Control Signals Compatible with the TLC540 and TLC545 8-Bit A/D Converters and with the TLC1540 10-Bit A/D Converter

TLC548M, TLC549M . . . D OR P PACKAGE
TLC548I, TLC549I . . . D OR P PACKAGE
TLC548C, TLC549C . . . D PACKAGE
(TOP VIEW)



description

The TLC548 and TLC549 are LinCMOS™ A/D peripheral integrated circuits built around an 8-bit switched-capacitor successive-approximation ADC. They are designed for serial interface with a microprocessor or peripheral through a 3-state data output and an analog input. The TLC548 and TLC549 use only the Input/Output Clock (I/O Clock) input along with the Chip Select ($\overline{CS}$) input for data control. The maximum I/O clock input frequency of the TLC548 is guaranteed up to 2.048 megahertz, and the I/O clock input frequency of the TLC549 is guaranteed to 1.1 megahertz. Detailed information on interfacing to most popular microprocessors is readily available from the factory.

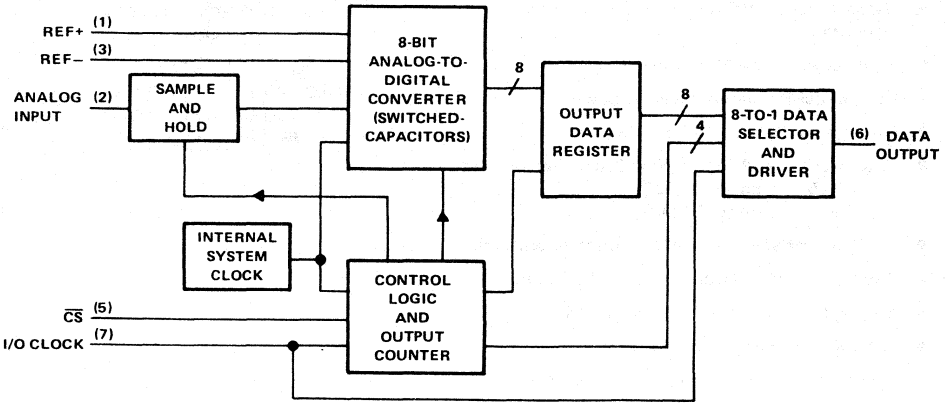
Operation of the TLC548 and the TLC549 is very similar to that of the more complex TLC540 and TLC541 devices; however, the TLC548 and TLC549 provide an on-chip system clock that operates typically at 4 megahertz and requires no external components. The on-chip system clock allows internal device operation to proceed independently of serial input/output data timing and permits manipulation of the TLC548 and TLC549 as desired for a wide range of software and hardware requirements. The I/O Clock together with the internal system clock allow high-speed data transfer and conversion rates of 45,500 conversions per second for the TLC548, and 40,000 conversions per second for the TLC549.

Additional TLC548 and TLC549 features include versatile control logic, an on-chip sample-and-hold circuit that can operate automatically or under microprocessor control, and a high-speed converter with differential high-impedance reference voltage inputs that ease ratiometric conversion, scaling, and circuit isolation from logic and supply noises. Design of the totally switched-capacitor successive-approximation converter circuit allows conversion with a maximum total error of ±0.5 least significant bit (LSB) in less than 17 microseconds.

The TLC548M and TLC549M are available in the D or P plastic package and are characterized for operation over the temperature range of −55°C to 125°C. The TLC548I and TLC549I are characterized for operation from −40°C to 85°C. The TLC548C and TLC549C are characterized for operation from 0°C to 70°C.

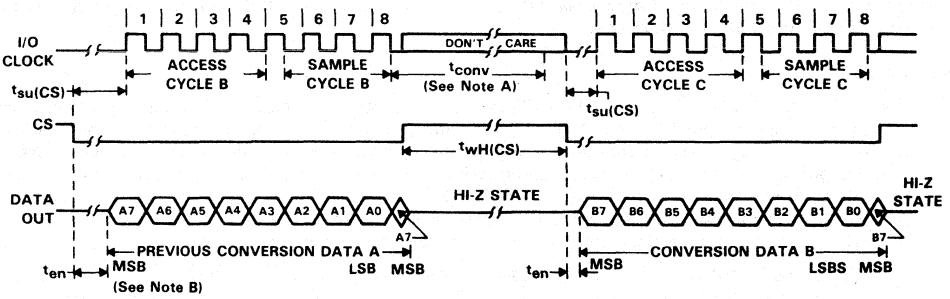
LinCMOS is a trademark of Texas Instruments.

functional block diagram



5

operating sequence



NOTES: A. The conversion cycle, which requires 36 internal system clock periods (17 μs maximum), is initiated with the 8th I/O clock pulse trailing edge after $\overline{CS}$ goes low for the channel whose address exists in memory at the time.

B. The most significant bit (A7) will automatically be placed on the DATA OUT bus after $\overline{CS}$ is brought low. The remaining seven bits (A6-A0) will be clocked out on the first seven I/O clock falling edges. B7-B0 will follow in the same manner.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 6.5 V
Input voltage range at any input . . . . . −0.3 V to V_{CC} + 0.3 V
Output voltage range . . . . . −0.3 V to V_{CC} + 0.3 V
Peak input current range (any input) . . . . . ±10 mA
Peak total input current range (all inputs) . . . . . ±30 mA
Operating free-air temperature range (see Note 2): TLC548M, TLC549M . . . . . −55°C to 125°C
TLC548I, TLC549I . . . . . −40°C to 85°C
TLC548C, TLC549C . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds . . . . . 260°C

NOTES: 1. All voltage values are with respect to the network ground terminal with the REF− and GND terminal pins connected together, unless otherwise noted.
2. The D package is not guaranteed below −40°C.

recommended operating conditions

		TLC548			TLC549			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}		3	5	6	3	5	6	V
Positive reference voltage, V_{REF+} (see Note 3)		2.5	V_{CC}	$V_{CC}+0.1$	2.5	V_{CC}	$V_{CC}+0.1$	V
Negative reference voltage, V_{REF-} (see Note 3)		−0.1	0	2.5	−0.1	0	2.5	V
Differential reference voltage, V_{REF+}, V_{REF-} (see Note 3)		1	V_{CC}	$V_{CC}+0.2$	1	V_{CC}	$V_{CC}+0.2$	V
Analog input voltage (see Note 3)		0		V_{CC}	0		V_{CC}	V
High-level control input voltage, V_{IH} (for V_{CC} = 4.75 V to 5.5 V)		2			2			V
Low-level control input voltage, V_{IL} (for V_{CC} = 4.75 V to 5.5 V)				0.8			0.8	V
Input/output clock frequency, $f_{CLK(I/O)}$ (for V_{CC} = 4.75 V to 5.5 V)		0		2.048	0		1.1	MHz
Input/output clock high, $t_{wH(I/O)}$ (for V_{CC} = 4.75 V to 5.5 V)		200			404			ns
Input/output clock low, $t_{wL(I/O)}$ (for V_{CC} = 4.75 V to 5.5 V)		200			404			ns
Input/output clock transition time, $t_{t(I/O)}$ (see Note 4) (for V_{CC} = 4.75 V to 5.5 V)				100			100	ns
Duration of $\overline{CS}$ input high state during conversion, $t_{wH(CS)}$ (for V_{CC} = 4.75 V to 5.5 V)		17			17			μs
Setup time, $\overline{CS}$ low before first I/O clock, $t_{su(CS)}$ (for V_{CC} = 4.75 V to 5.5 V) (see Note 5)		1.4			1.4			μs
Operating free-air temperature, T_A	TLC548M, TLC549M	−55		125	−55		125	°C
	TLC548I, TLC549I	−40		85	−40		85	
	TLC548C, TLC549C	0		70	0		70	

NOTES: 3. Analog input voltages greater than that applied to REF+ convert to all ones (11111111), while input voltages less than that applied to REF− convert to all zeros (00000000). For proper operation, the positive reference voltage V_{REF+} must be at least 1 volt greater than the negative reference voltage V_{REF-}. In additon, unadjusted errors may increase as the differential reference voltage $V_{REF+} - V_{REF-}$ falls below 4.75 V.
4. This is the time required for the input/output clock input signal to fall from V_{IH} min to V_{IL} max or to rise from V_{IL} max to V_{IH} min. In the vicinity of normal room temperature, the devices function with input clock transition time as slow as 2 μs for remote data acquisition applications in which the sensor and the ADC are placed several feet away from the controlling microprocessor.
5. To minimize errors caused by noise at the $\overline{CS}$ input, the internal circuitry waits for two rising edges and one falling edge of internal system clock after $\overline{CS}$↓ before responding to control input signals. This $\overline{CS}$ set-up time is given by the t_{en} and $t_{su(CS)}$ specifications.

electrical characteristics over recommended operating free-air temperature range, V_{CC} = V_{REF+} = 4.75 V to 5.5 V (unless otherwise noted), $f_{CLK(I/O)}$ = 2.048 MHz for TLC548 or 1.1 MHz for TLC549

PARAMETER			TEST CONDITIONS	MIN	TYP†	MAX	UNIT
V_{OH}	High-level output voltage		V_{CC} = 4.75 V, I_{OH} = −360 μA	2.4			V
V_{OL}	Low-level output voltage		V_{CC} = 4.75 V, I_{OL} = 3.2 mA			0.4	V
I_{OZ}	Off-state (high-impedance state) output current		V_O = V_{CC}, $\overline{CS}$ at V_{CC}			10	V
			V_O = 0, $\overline{CS}$ at V_{CC}			−10	
I_{IH}	High-level input current, control inputs		V_I = V_{CC}		0.005	2.5	μA
I_{IL}	Low-level input current, control inputs		V_I = 0		−0.005	−2.5	μA
$I_{I(on)}$	Analog channel on-state input current, during sample cycle		Analog input at V_{CC}		0.4	1	μA
			Analog input at 0 V		−0.4	−1	
I_{CC}	Operating supply current		$\overline{CS}$ at 0 V		1.8	2.5	mA
I_{CC} + I_{REF}	Supply and reference current		V_{REF+} = V_{CC}		1.9	3	mA
C_i	Input capacitance	Analog inputs			7	55	pF
		Control inputs			5	15	

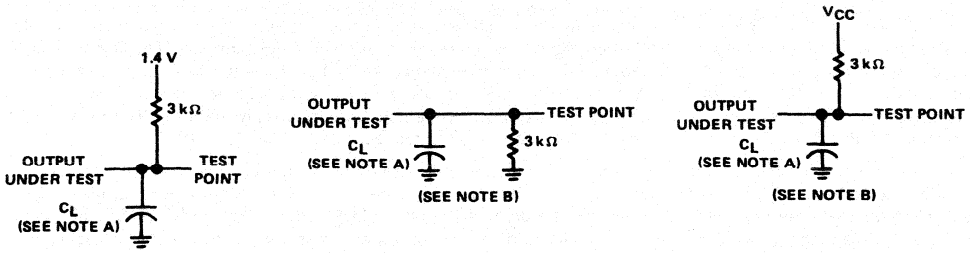
operating characteritics over recommended operating free-air temperature range, V_{CC} = V_{REF+} = 4.75 V to 5.5 V (unless otherwise noted), $f_{CLK(I/O)}$ = 2.048 MHz for TLC548 or 1.1 MHz for TLC549

PARAMETER		TEST CONDITIONS	TLC548			TLC549			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
	Linearity error	See Note 6			±0.5			±0.5	LSB
	Zero error	See Note 7			±0.5			±0.5	LSB
	Full-scale error	See Note 7			±0.5			±0.5	LSB
	Total unadjusted error	See Note 8			±0.5			±0.5	LSB
t_{conv}	Conversion time	See Operating Sequence		8	17		12	17	μs
	Total access and conversion time	See Operating Sequence		12	22		19	25	μs
t_{acq}	Channel acquisition time (sample cycle)	See Operating Sequence			4			4	I/O clock cycles
t_v	Time output data remains valid after I/O clock↓		10			10			ns
t_d	Delay time to data output valid	I/O clock↓			300			400	ns
t_{en}	Output enable time	See Parameter Measurement Information			1.4			1.4	μs
t_{dis}	Output disable time				150			150	ns
$t_{r(bus)}$	Data bus rise time				300			300	ns
$t_{f(bus)}$	Data bus fall time				300			300	ns

†All typicals are at V_{CC} = 5 V, T_A = 25°C.

NOTES: 6. Linearity error is the deviation from the best straight line through the A/D transfer characteristics.
7. Zero error is the difference between 00000000 and the converted output for zero input voltage; full-scale error is the difference between 11111111 and the converted output for full-scale input voltage.
8. Total unadjusted error is the sum of linearity, zero, and full-scale errors.

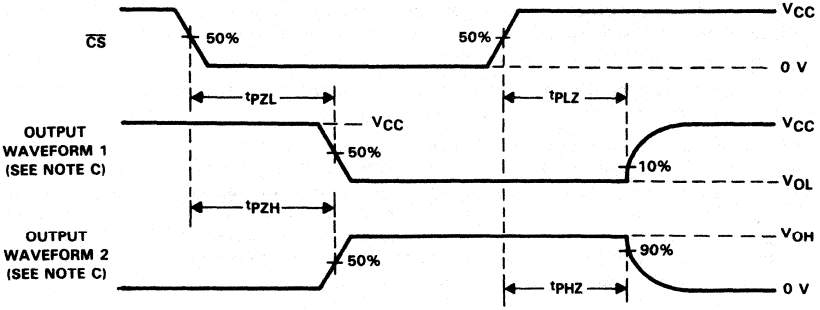
PARAMETER MEASUREMENT INFORMATION



LOAD CIRCUIT FOR t_d, t_r, AND t_f

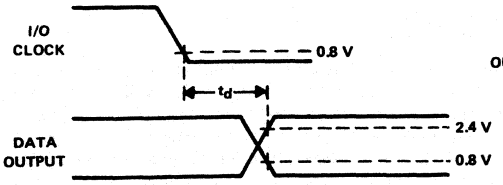
LOAD CIRCUIT FOR t_{PZH} AND t_{PHZ}

LOAD CIRCUIT FOR t_{PZL} AND t_{PLZ}

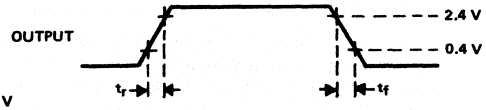


(SEE NOTE B)

VOLTAGE WAVEFORMS FOR ENABLE AND DISABLE TIMES



VOLTAGE WAVEFORM FOR DELAY TIME



VOLTAGE WAVEFORM FOR RISE AND FALL TIMES

NOTES: A. C_L = 50 pF for TLC548 and 100 pF for TLC549; C_L includes jig capacitance.
B. t_{en} = t_{PZH} or t_{PZL}, t_{dis} = t_{PHZ} or t_{PLZ}.
C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.

PRINCIPLES OF OPERATION

The TLC548 and TLC549 are each complete data acquisition systems on a single chip. Each contains an internal system clock, sample-and-hold, 8-bit A/D converter, data register, and control logic circuitry. For flexibility and access speed, there are two control inputs: I/O Clock and Chip Select ($\overline{CS}$). These control inputs and a TTL-compatible three-state output facilitate serial communications with a microprocessor or minicomputer. A conversion can be completed in 17 microseconds or less, while complete input-conversion-output cycles can be repeated in 22 microseconds for the TLC548 and in 25 microseconds for the TLC549.

The internal system clock and I/O clock are used independently and do not require any special speed or phase relationships between them. This independence simplifies the hardware and software control tasks for the device. Due to this independence and the internal generation of the system clock, the control hardware and software need only be concerned with reading the previous conversion result and starting the conversion by using the I/O clock. In this manner, the internal system clock drives the "conversion crunching" circuitry so that the control hardware and software need not be concerned with this task.

When $\overline{CS}$ is high, the data output pin is in a high-impedance condition and the I/O clock pin is disabled. This $\overline{CS}$ control function allows the I/O Clock pin to share the same control logic point with its counterpart pin when additional TLC548 and TLC549 devices are used. This also serves to minimize the required control logic pins when using multiple TLC548 and TLC549 devices.

The control sequence has been designed to minimize the time and effort required to initiate conversion and obtain the conversion result. A normal control sequence is:

1. $\overline{CS}$ is brought low. To minimize errors caused by noise at the $\overline{CS}$ input, the internal circuitry waits for two rising edges and then a falling edge of the internal system clock after a $\overline{CS}\downarrow$ before the transition is recognized. However, upon a $\overline{CS}$ rising edge, DATA OUT will go to a high-impedance state within the t_{dis} specification even though the rest of the IC's circuitry will not recognize the transition until the $t_{su(CS)}$ specification has elapsed. This technique is used to protect the device against noise when used in a noisy environment. The most significant bit (MSB) of the previous conversion result will initially appear on the DATA OUT pin when $\overline{CS}$ goes low.
2. The falling edges of the first four I/O clock cycles shift out the 2nd, 3rd, 4th, and 5th most significant bits of the previous conversion result. The on-chip sample-and-hold begins sampling the analog input after the 4th high-to-low transition of the I/O Clock. The sampling operation basically involves the charging of internal capacitors to the level of the analog input voltage.
3. Three more I/O clock cycles are then applied to the I/O pin and the 6th, 7th, and 8th conversion bits are shifted out on the falling edges of these clock cycles.
4. The final, (the 8th), clock cycle is applied to the I/O clock pin. The on-chip sample-and-hold begins the hold function upon the high-to-low transition of this clock cycle. The hold function will continue for the next four internal system clock cycles, after which the holding function terminates and the conversion is performed during the next 32 system clock cycles, giving a total of 36 cycles. After the 8th I/O clock cycle, $\overline{CS}$ must go high or the I/O clock must remain low for at least 36 internal system clock cycles to allow for the completion of the hold and conversion functions. $\overline{CS}$ can be kept low during periods of multiple conversion. When keeping $\overline{CS}$ low during periods of multiple conversion, special care must be exercised to prevent noise glitches on the I/O Clock line. If glitches occur on the I/O Clock line, the I/O sequence between the microprocessor/controller and the device will lose synchronization. If $\overline{CS}$ is taken high, it must remain high until the end of conversion. Otherwise, a valid high-to-low transition of $\overline{CS}$ will cause a reset condition, which will abort the conversion in progress.

A new conversion may be started and the ongoing conversion simultaneously aborted by performing steps 1 through 4 before the 36 internal system clock cycles occur. Such action will yield the conversion result of the previous conversion and not the ongoing conversion.

PRINCIPLES OF OPERATION

For certain applications, such as strobing applications, it is necessary to start conversion at a specific point in time. This device will accommodate these applications. Although the on-chip sample-and-hold begins sampling upon the high-to-low transition of the 4th I/O clock cycle, the hold function does not begin until the high-to-low transition of the 8th I/O clock cycle, which should occur at the moment when the analog signal must be converted. The TLC548 and TLC549 will continue sampling the analog input until the high-to-low transition of the 8th I/O clock pulse. The control circuitry or software will then immediately lower the I/O clock signal and start the holding function to hold the analog signal at the desired point in time and start conversion.

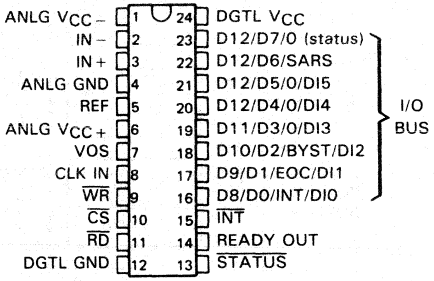
Detailed information on interfacing to the most popular microprocessor is readily available from Texas Instruments.

TLC1205A, TLC1205B, TLC1225A, TLC1225B
SELF-CALIBRATING 12-BIT-PLUS-SIGN UNIPOLAR OR BIPOLAR ANALOG-TO-DIGITAL CONVERTERS

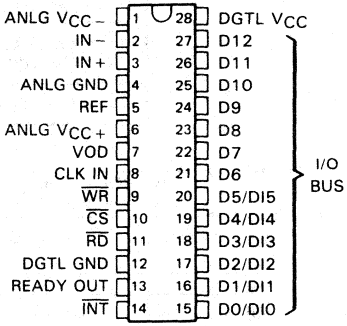
D2982, FEBRUARY 1987

- ADVANCED LinCMOS™ Technology
- Self-Calibration Eliminates Expensive Trimming at Factory and Offset Adjustment in the Field
- 12-Bit Plus Sign Unipolar or Bit Bipolar
- ± ½ and ± 1 LSB Linearity Error in Unipolar Configuration
- 10 μs Conversion Time (Mode 2) (clock = 2.6 MHz)
  20 μs Conversion Time (Mode 1) (clock = 2.6 MHz)
- Compatible with All Microprocessors
- True Differential Analog Voltage Inputs
- 0 to 5 V Analog Voltage Range with Single 5-V Supply (Unipolar Configuration)
- −5 V to 5 V Analog Voltage Range with ±5-V Supplies (Bipolar Configuration)
- Low Power . . . 25 mW Maximum
- Replaces National Semiconductor ADC1205 and ADC1225 in Mode 1 Operation

TLC1205
J OR N DUAL-IN-LINE PACKAGE
(TOP VIEW)



TLC1225
J OR N DUAL-IN-LINE PACKAGE
(TOP VIEW)



description

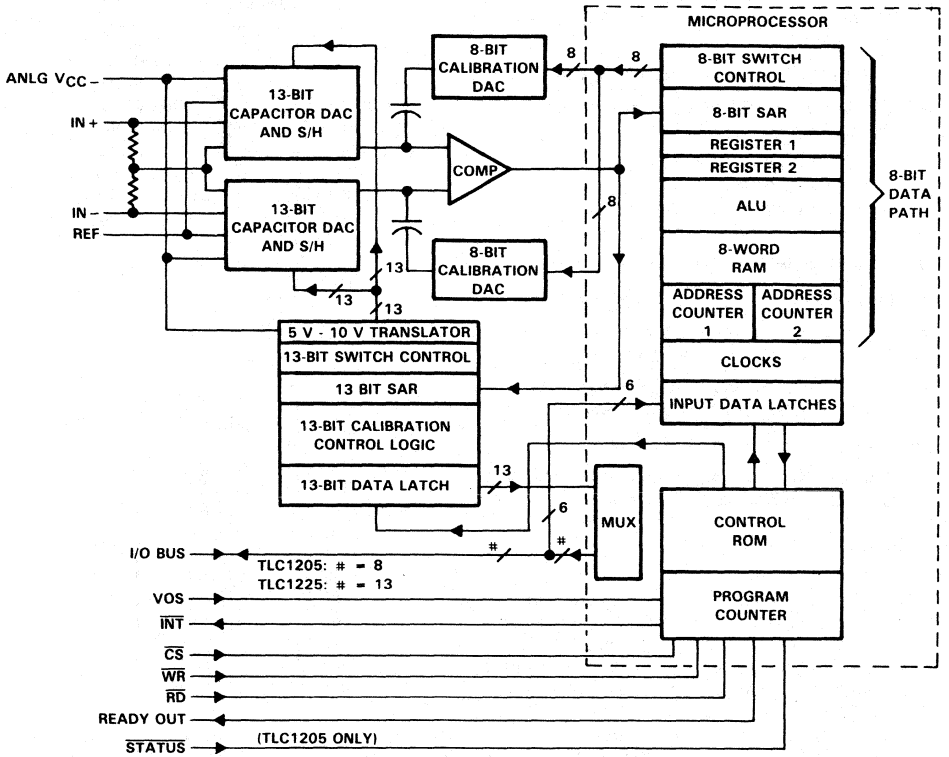
The TLC1205 and TLC1225 converters are manufactured with Texas Instruments highly efficient ADVANCED LinCMOS™ technology. Either of the TLC1205 or TLC1225 CMOS analog-to digital converters can be operated as a unipolar or bipolar converter. A unipolar input (0 to 5 V) can be accommodated with a single 5-volt supply, while a bipolar input (−5 V to 5 V) requires the addition of a 5-volt negative supply. Conversion is performed via the successive-approximation method. The 24-pin TLC1205 outputs the converted data in two 8-bit bytes, while the TLC1225 outputs the converted data in a parallel word and interfaces directly to a 16-bit data bus. Negative numbers are given in the 2's complement data format. All digital signals are fully TTL and CMOS compatible.

These converters utilize a self-calibration technique by which seven of the internal capacitors in the capacitive ladder of the A/D conversion circuitry can be automatically or manually calibrated. If the converters are operated in Mode 1, one of the seven internal capacitors is calibrated during the first part of the conversion sequence. For example, one capacitor is calibrated during the first conversion. The next capacitor is calibrated during the second conversion. If the converters are operated in Mode 2, the internal capacitors are calibrated during a nonconversion, capacitor-calibrate cycle in which all seven of the internal capacitors are calibrated at the same time. A Mode 2 conversion requires only 10 μs (2.6 MHz clock) after the nonconversion, capacitor-calibrating cycle has been completed. The calibration or conversion cycle may be initiated at any time by issuing the proper address to the data bus. The self-calibrating techniques eliminate the need for expensive trimming of thin-film resistors at the factory and provide excellent performance at low cost.

ADVANCED LinCMOS™ is a trademark of Texas Instruments Incorporated

TEXAS INSTRUMENTS

functional block diagram



In Mode 1, these converters are replacements for National Semiconductor ADC1205 and ADC1225 integrated circuits. The Mode 1 conversion time for guaranteed accuracy is 51 clock cycles. In the Mode 2 operation, these devices are no longer true replacements. However, the Mode 2 conversion time for guaranteed accuracy is only 26 clock cycles.

The TLC1205AM, TLC1205BM, TLC1225AM, and TLC1225BM are characterized for operation over the full military temperature range of −55°C to 125°C. The TLC1205AI, TLC1205BI, TLC1225AI, and TLC1225BI are characterized for operation from −40°C to 85°C.

operation description

calibration of comparator offset

The following actions are performed to calibrate the comparator offset:

1. The IN+ and IN− inputs are internally shorted together in order that the comparator input is zero. A course comparator offset calibration is performed by storing the offset voltages of the interconnecting comparator stages on the coupling capacitors, which connect the interconnecting stages. Refer to Figure 1. The storage of offset voltages is accomplished by closing all switches and then opening switches A and A′, then switches B and B′, and then C and C′. This process continues until all interconnecting stages of the comparator are calibrated. After this action, some of the comparator offset still remains uncalibrated.

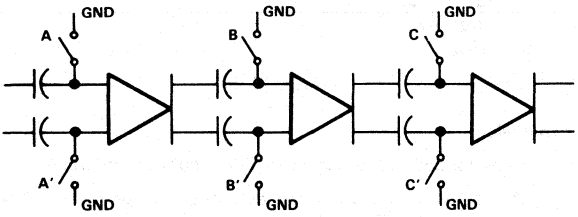


FIGURE 1

2. An A/D conversion is done on the remaining offset with the 8-bit calibration DACs and 8-bit SAR and the result is stored in the RAM.

capacitor calibration of the ADC's Capacitive Ladder

The following actions are performed to calibrate capacitors in the 13-bit DAC's, which comprise the ADC's capacitive ladder:

1. The IN+ and IN− inputs are internally disconnected from the 13-bit capacitive DACs.
2. The most-significant-bit (MSB) capacitor is tied to REF, while the rest of the ladder capacitors are tied to GND. The A/D conversion result for the remaining comparator offset, obtained in step 2 above, is retrieved from the RAM and is input to the 8-bit DACs.
3. Step 1 of the Calibration of Comparator Offset sequence is performed. The 8-bit DAC input is returned to zero and the remaining comparator offset is then subtracted. Thus, the comparator offset is completely corrected.
4. Now the MSB capacitor is tied to GND, while the rest of the ladder capacitors, C_X , are tied to REF. An MSB capacitor voltage error (see Figure 2) on the comparator output will occur if the MSB capacitor does not equal the sum of the other capacitors in the capacitive ladder. This error voltage is converted to an 8-bit word from which a capacitor error is computed and stored in the RAM.
5. The capacitor voltage error for the next most significant capacitor is calibrated by keeping the MSB capacitor grounded and then performing the above Steps 1 - 4 while using the next most significant capacitor in lieu of the MSB capacitor. The seven most significant capacitors can be calibrated in this manner.

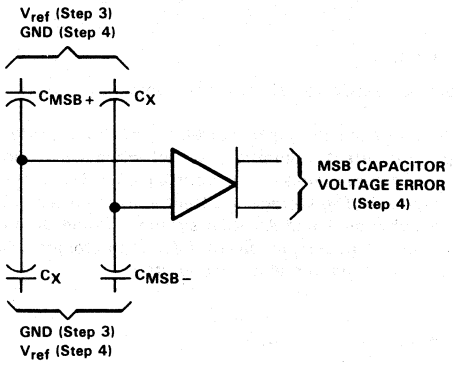


FIGURE 2

analog-to-digital conversion

The following steps are performed in the analog-to-digital conversion process:

1. Step 1 of the Calibration of Comparator Offset Sequence is performed. The A/D conversion result for the remaining comparator offset, which was obtained in Step 2 of the Calibration of Comparator Offset, is retrieved from the RAM and is input to the 8-bit DACs. Thus the comparator offset is completely corrected.
2. IN+ and IN− are sampled onto the 13-bit capacitive ladders.
3. The 13-bit analog-to-digital conversion is performed. As the successive-approximation conversion proceeds successively through the seven most significant capacitors, the error for each of these capacitors is recovered from the RAM and accumulated in a register. This register controls the 8-bit DACs so the total accumulated error for these capacitors is subtracted out during the conversion process.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage (ANLG V_{CC+} and DGTL V_{CC}) (see Note 1) . . . . . 15 V
Supply voltage, ANLG V_{CC-} . . . . . −15 V
Control and Clock input voltage range . . . . . −0.3 V to +15 V
Analog input (IN+, IN−) voltage range,
V_{I+} and V_{I-} . . . . . ANLG V_{CC-} −0.3 V to ANLG V_{CC+} + 0.3 V
Reference voltage range, V_{ref} . . . . . −0.3 V to ANLG V_{CC+} + 0.3 V
Mode select voltage range, VOS . . . . . −0.3 V to ANLG V_{CC+} + 0.3 V
Output voltage range . . . . . −0.3 V to DGTL V_{CC} + 0.3 V
Input current (per pin) . . . . . ±5 mA
Input current (per package) . . . . . ±20 mA
Operating free-air temperature range:
TLC1205AM, TLC1205BM, TLC1225AM, TL1225BM . . . . . −55°C to 125°C
TLC1205AI, TLC1205BI, TLC1225AI, TLC1225BI . . . . . −40°C to 85°C
Storage temperature range . . . . . −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from the case for 60 seconds: J package . . . . . 300°C
Lead temperature 1,6 mm (1/16 inch) from the case for 10 seconds: N package . . . . . 260°C

Note 1: All analog voltages are referred to ANLG GND and all digital voltages are referred to DGTL GND.

recommended operating conditions

		MIN	MAX	UNIT
Supply voltage	ANLG V_{CC+}	4.5	6	V
	ANLG V_{CC-}	−5.5	ANLG GND	
	DGTL V_{CC}	4.5	6	
High-level input voltage, V_{IH}, all digital inputs except CLK IN (V_{CC} = 4.75 V to 5.25 V)		2		V
Low level input voltage, V_{IL}, all digital inputs except CLK IN (V_{CC} = 4.75 V to 5.25 V)			0.8	V
Analog input voltage, V_{I+}, V_{I-}	Bipolar range	ANLG V_{CC-} − 0.05	ANLG V_{CC+} + 0.05	V
	Unipolar range	ANLG GND − 0.05	ANLG V_{CC+} + 0.05	
Clock input frequency, f_{clock}		0.3	2.6	MHz
Clock duty cycle		40%	60%	
Pulse duration, $\overline{CS}$ and $\overline{WR}$ both low, $t_{w(\overline{CS}\cdot\overline{WR})}$		350		ns
Setup time before $\overline{WR}\uparrow$ or $\overline{CS}\uparrow$, t_{su}			100	ns
Hold time after $\overline{WR}\uparrow$ or $\overline{CS}\uparrow$, t_h			20	ns
Operating free-air temperature, T_A	TLC1205AM, TLC1225AM TLC1205BM, TLC1225BM	−55	125	°C
	TLC1205AI, TLC1225AI TLC1205BI, TLC1225BI	−40	85	

electrical characteristics over recommended operating free-air temperature range, ANLG V_{CC+} = DGTL V_{CC} = V_{ref} = 5 V, ANLG V_{CC-} = −5 V (for bipolar input range), ANLG V_{CC-} = ANLG GND (for unipolar input range) (unless otherwise noted) (see Note 1)

PARAMETER		TEST CONDITIONS		MIN	MAX	UNIT
V_{OH}	High-level output voltage	DGTL V_{CC} = 4.75 V	I_O = −1.8 mA	2.4		V
			I_O = −50 μA	4.5		
V_{OL}	Low-level output voltage	DGTL V_{CC} = 4.75 V,	I_O = 8 mA		0.4	V
V_{T+}	Clock positive-going threshold voltage			2.7	3.5	V
V_{T-}	Clock negative-going threshold voltage			1.4	2.1	V
V_{hys}	Clock input hysteresis	V_{T+}min − V_{T-}max		0.6		V
		V_{T+}max − V_{T-}min			2.1	
R_{ref}	Input resistance, REF terminal			1	10	MΩ
I_{IH}	High-level input current	V_I = 5 V			1	μA
I_{IL}	Low-level input current	V_I = 0			−1	μA
I_{OZ}	High-impedance-state output leakage current	V_O = 0			−3	μA
		V_O = 5 V			3	
I_O	Output current	V_O = 0			−6	mA
		V_O = 5 V			8	
DGTL I_{CC}	Supply current from DGTL V_{CC}	f_{clk} = 2.6 MHz,	$\overline{CS}$ high		3	mA
ANLG I_{CC+}	Supply current from ANLG V_{CC+}	f_{clk} = 2.6 MHz,	$\overline{CS}$ high		3	mA
ANLG I_{CC-}	Supply current from ANLG V_{CC-}	f_{clk} = 2.6 MHz,	$\overline{CS}$ high		−3	mA

NOTE 1: Bipolar input range is defined as: V_{I+} = −5.05 V to +5.05 V, V_{I-} = −5.05 V to +5.05 V, and $|V_{I+} - V_{I-}| \leq 5.05$ V. The unipolar input voltage range is defined as: V_{I+} = −0.05 V to 5.05 V, V_{I-} = −0.05 V to 5.05 V, and $|V_{I+} - V_{I-}| \leq 5.05$ V.

operating characteristics over recommended operating free-air temperature range, ANLG V_{CC+} = DGTL V_{CC} = V_{ref} = 5 V, ANLG V_{CC-} = −5 V (for bipolar input range), ANLG V_{CC-} = ANLG GND (for unipolar input range), f_{clock} = 2.6 MHz (unless otherwise noted)(see Note 1)

PARAMETER			TEST CONDITIONS		MIN	MAX	UNIT
Linearity error			Unipolar input range	TLC1205A, TLC1225A		±1	LSB
				TLC1205B, TLC1225B		±0.5	
			Bipolar input range	TLC1205A, TLC1225A		±2	
				TLC1205B, TLC1225B		±1.5	
Zero error						±0.5	LSB
Adjusted positive and negative full-scale error (see Note 2)			Unipolar input range			±1	LSB
Adjusted positive and negative full-scale error (see Note 3)			Bipolar input range			±1	LSB
Temperature coefficient of gain						15	ppm/°C
Temperature coefficient of offset point						1.5	ppm/°C
k_{SVS}	Supply voltage sensitivity	Zero error	ANLG V_{CC+} = 5 V ± 5%, ANLG V_{CC-} = −5 V ± 5%, DGTL V_{CC} = 5 V ± 5%			±0.75	LSB
		Positive and negative full-scale error				±0.75	
		Linearity error				±0.25	
t_c	Conversion time	Mode 1				51	$\frac{1}{f_{clk}}$
		Mode 2				26	
t_a	Access time (delay from falling edge of $\overline{CS}$•$\overline{RD}$ to data output)		C_L = 100 pF			210	ns
t_{dis}	Disable time, output (delay from rising edge of $\overline{RD}$ to high-impedance state		R_L = 10 kΩ,	C_L = 10 pF		260	ns
			R_L = 2 kΩ,	C_L = 100 pF		290	
$t_{d(READY)}$	$\overline{RD}$ or $\overline{WR}$ to READY OUT delay					400	ns
$t_{d(INT)}$	$\overline{RD}$ or $\overline{WR}$ to reset of $\overline{INT}$ delay					400	ns

NOTES: 1. Bipolar input range is defined as: V_{I+} = −5.05 V to +5.05 V, V_{I-} = −5.05 V to +5.05 V, and $|V_{I+} - V_{I-}| \leq 5.05$ V. The unipolar input voltage range is defined as: V_{I+} = −0.05 V to 5.05 V, V_{I-} = −0.05 V to 5.05 V, and $|V_{I+} - V_{I-}| \leq 5.05$ V.
2. See section — Positive and Negative Full-Scale Adjustment, Unipolar Inputs.
3. See section — Positive and Negative Full-Scale Adjustment, Bipolar Inputs.

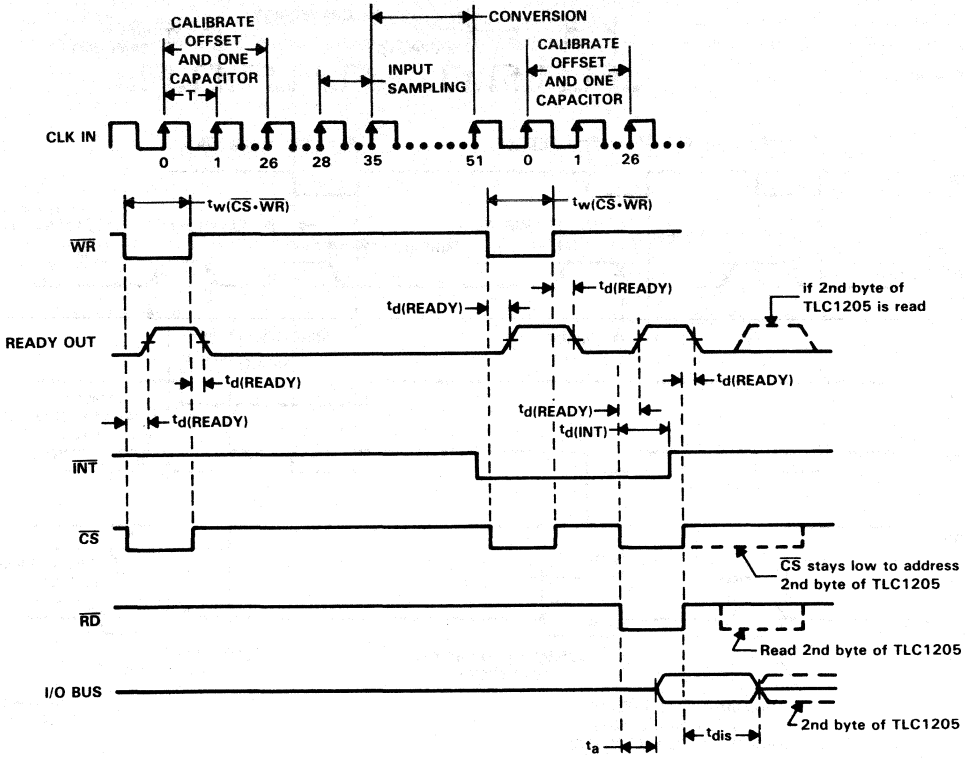


FIGURE 3. MODE 1 TIMING DIAGRAM

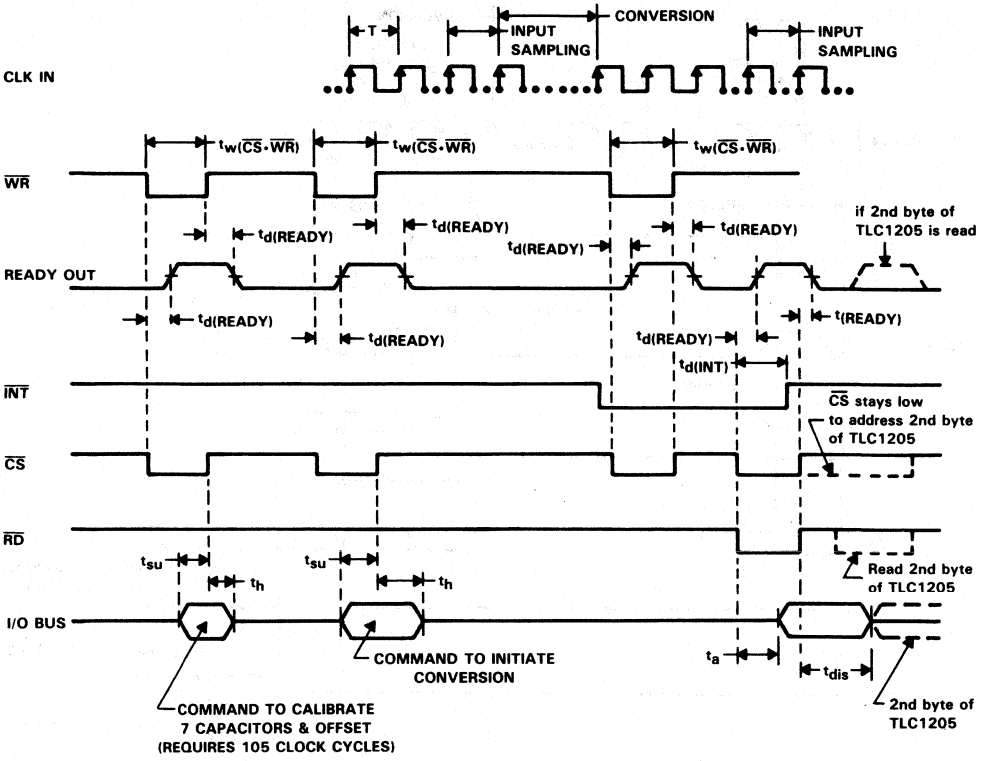


FIGURE 4. MODE 2 TIMING DIAGRAM

PARAMETER MEASUREMENT INFORMATION

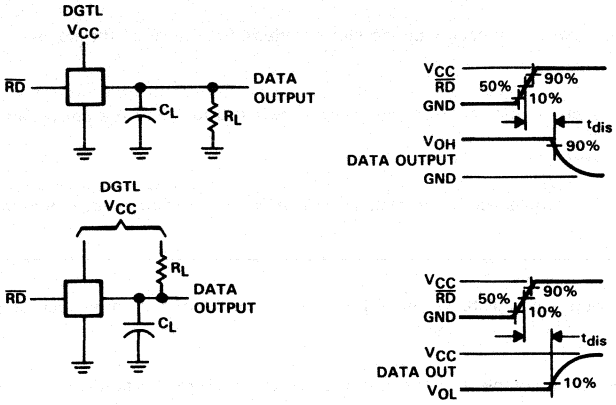


FIGURE 5. LOAD CIRCUITS AND WAVEFORMS

PRINCIPLES OF OPERATION

The following information is categorized into Mode 1 and Mode 2 groupings to allow the designer to concentrate on a particular mode of interest

power-up calibration sequence

Mode 1

When the chip is powered-up, the internal capacitors are automatically calibrated as part of the power-up sequence. This initial calibration sequence requires 105 clock cycles. The chip will not perform an A/D conversion during this calibration sequence.

Mode 2

Power-Up calibration is not automatic and calibration is initiated by writing control words to the six least significant bits of the data bus. If addressed or initiated, conversion can begin after the first clock cycle. However, full A/D conversion accuracy is not guaranteed until after internal capacitor calibration.

conversion start sequence

Mode 1

The conversion sequence is initiated when $\overline{CS}$ and $\overline{WR}$ are both low.

Mode 2

The writing of the conversion command word to the six least significant bits of the data bus, when either $\overline{CS}$ or $\overline{WR}$ goes high, initiates the conversion sequence.

analog sampling sequence

Mode 1

Sampling of the input signal occurs during clock cycles 29 thru 35 of the conversion sequence.

Mode 2

Sampling of the input signal occurs during clock cycles 4 thru 10 of the conversion sequence.

completed A/D conversion

When $\overline{INT}$ goes low, conversion is complete and the A/D result can be read. A new conversion can begin immediately.

Mode 1

The A/D conversion is complete at the end of clock cycle 51 of the conversion sequence.

Mode 2

The A/D conversion is complete at the end of clock cycle 26 of the conversion sequence.

aborting a conversion in process and beginning a new conversion

Mode 1 and Mode 2

If a conversion is initiated while a conversion sequence is in process, the ongoing conversion will be aborted and a new conversion sequence will begin.

Mode 1

If the new conversion is started before the Analog Sampling begins (see Analog Sampling Sequence section and the Mode 1 Timing Diagram), the particular internal capacitor that was being calibrated during the aborted conversion sequence will be calibrated during the new conversion sequence. Otherwise, the next internal capacitor will be calibrated during the new conversion sequence.

reading the conversion result

TLC1205

Upon activating the required control signals to read the conversion result or status information, the appropriate pins are brought out of a high-impedance state and drive the data bus with the proper information. These pins are D12/D7/0 through D8/DO/INT/DIO.

If $\overline{STATUS}$, $\overline{CS}$, and $\overline{RD}$ are all low, status information can be read. The format of the conversion result and status information and the respective pins for output are presented in Table 1.

TABLE 1

BYTES	$\overline{\text{STATUS}}$	$\overline{\text{CS}}$	$\overline{\text{RD}}$	I/O BUS							
				D12/ D7/ 0	D12/ D6/ SARS	D12/ D5/ 0/ DI5	D12/ D4/ 0/ DI4	D11/ D3/ 0/ DI3	D10/ D2/ BYST/ DI2	D9/ D1/ EOC/ DI1	D8/ D0/ INT/ DI0
MSB	H	L	L	D12	D12	D12	D12	D11	D10	D9	D8
LSB	H	L	↑↓	D7	D6	D5	D4	D3	D2	D1	D0
STATUS	L	L	L	L	SARS	L	L	L	BYST	EOC	INT

The status information is described in Table 2.

TABLE 2

STATUS BIT	BIT DESCRIPTION	TO CLEAR BIT
L	The output has no meaning and is low.	
SARS	A high indicates that conversion is in progress.	
BYST	A low indicates that the next conversion result read will be the most significant conversion byte. A high indicates that the next conversion result read will be the least significant conversion byte. The BYST bit is toggled by reading the conversion result bytes. This bit can be cleared with a "status write" instruction.	By a "status write" or toggled by reading a conversion data byte
EOC	A high indicates that conversion is complete and the conversion data has been transferred to the output latch.	
INT	A high indicates that conversion is complete and the conversion data has been transferred to the output latch and is ready to read.	By reading a conversion data byte, reading the status byte, or a "status write"

With $\overline{\text{STATUS}}$ high, when $\overline{\text{CS}}$ and $\overline{\text{RD}}$ both go low, the most significant byte (MSB) of the conversion result can be read. Then by taking $\overline{\text{RD}}$ high and back low, the least significant byte (LSB) of the conversion result can be read. Subsequently taking $\overline{\text{RD}}$ high and low causes the alternate reading of the MSB and LSB of the conversion result.

The format of the output is extended sign with 2's complement, right justified data. For both unipolar and bipolar cases, the sign bit D12 is low if $V_{I+} - V_{I-}$ is positive and high if $V_{I+} - V_{I-}$ is negative. The format of the conversion result and the respective output pins are presented in Table 2. The format of the conversion result and the respective pins for output are presented in Table 1.

TLC1225

When both $\overline{\text{CS}}$ and $\overline{\text{RD}}$ go low, all 13 bits of conversion data are output to the I/O bus. The format of the output is extended sign with 2's complement, right justified data. Unlike the TLC1205, the TLC1225 does not have internal status information or a $\overline{\text{STATUS}}$ pin. For both unipolar and bipolar cases, the sign bit D12 is low if $V_{I+} - V_{I-}$ is positive and high if $V_{I+} - V_{I-}$ is negative.

general

reset INT

When reading the conversion data, the falling edge of the first low-going combination of $\overline{CS}$ and $\overline{RD}$ will reset $\overline{INT}$. The falling edge of the low-going combination of $\overline{CS}$ and $\overline{WR}$ will also reset $\overline{INT}$.

ready out

For high-speed microprocessors, READY OUT allows the TLC1205 and the TLC1225 to insert a wait state in the microprocessor's read cycle.

status write (TLC1205)

A status write resets the internal logic and status bits and aborts any conversion in process. A status write occurs when $\overline{CS}$, $\overline{WR}$, and $\overline{STATUS}$ are taken low.

reference voltage (V_{ref})

This voltage defines the range for $|V_{I+} - V_{I-}|$. When $|V_{I+} - V_{I-}|$ equals V_{ref}, the highest conversion data value results. When $|V_{I+} - V_{I-}|$ equals 0, the conversion data value is zero. Thus, for a given input, the conversion data changes ratiometrically with changes in V_{ref}.

V_{OS}

This pin is a digital input and is used to select Mode 1 or Mode 2 operation. A logic low selects Mode 1; a logic high selects Mode 2.

In Mode 1, the ICs are true replacements for National Semiconductor's ADC1205 and ADC1225. The ADC1205 and ADC1225 use the VOS pin to adjust zero error. Since the zero error adjustment voltage is below the TLC1205's and TLC1225's maximum acceptable level for a logic low signal, the TLC1205 and TLC1225 ICs are true replacements. Even in Mode 1, the TLC1205's and TLC1225's converted data can be read earlier than the ADC1205's and ADC1225's.

calibration and conversion considerations

Mode 1

Calibration of the seven internal capacitors is an integral part of the A/D conversion. One of the seven internal capacitors is calibrated during the first part of the conversion sequence. For example, one of the capacitors is calibrated during the first conversion. The next capacitor is calibrated during the second conversion. After seven conversions, the pattern for calibrating the internal capacitors repeats. A conversion sequence requires 51 clock cycles.

A conversion is initiated by the low-going combination of $\overline{CS}$ and $\overline{WR}$. The conversion sequence is illustrated in the Mode 1 timing diagram.

Mode 2

Calibration of the internal capacitor and A/D conversion are two separate actions. Each action is independently initiated. Mode 2 conversion is much faster than Mode 1, since Mode 2 conversion is not accompanied by the calibration of internal capacitors. In Mode 2, a calibration command that calibrates all seven internal capacitors is normally issued first. A conversion command then initiates the A/D conversion without calibrating the internal capacitors. Subsequent conversions can be performed by issuing additional conversion commands. The calibration and conversion commands are totally independent from one another and can be initiated in any order. Calibration and conversion commands require 105 and 26 clock cycles, respectively.

The calibrate and conversion commands are initiated by writing control words on the six least significant bits of the data bus. These control words are written into the IC when either $\overline{CS}$ or $\overline{WR}$ goes high. The initiation of these commands is illustrated in the Mode 2 Timing Diagram. The bit patterns for the commands are shown in Table 3.

TABLE 3. MODE 2 CONVERSION COMMANDS

COMMAND	$\overline{CS}$ + $\overline{WR}$	I/O BUS						Required number of clock cycles
		DI5	DI4	DI3	DI2	DI1	DI0	
Conversion	↑	H	L	X	X	X	L	26
Calibrate†	↑	L	X	L	L	L	L	105

†Calibration is lost when clock is stopped.

analog inputs

differential inputs provide common mode rejection

The differential inputs reduce common-mode noise. Common-mode noise is noise common to both IN+ and IN− inputs, such as 60-Hz noise. There is no time interval between the sampling of the IN+ and IN− so these inputs are truly differential. Thus, no conversion errors result from a time interval between the sampling of the IN+ and IN− inputs.

input bypass capacitors

Input bypass capacitors may be used for noise filtering. However, the charge on these bypass capacitors will be depleted during the input sampling sequence when the internal sampling capacitors are charged. Note that the charging of the bypass capacitors through the differential source resistances must keep pace with the charge depletion of the bypass capacitors during the input sampling sequence. Note that higher source resistances reduce the amount of charging current for the bypass capacitors. Also, note that fast, successive conversion will have the greatest charge depletion effect on the bypass capacitors. Therefore, the above phenomenon becomes more significant as source resistances and the conversion rate (i.e., higher clock frequency and conversion initiation rate) increase.

In addition, if the above phenomenon prevents the bypass capacitors from fully charging between conversions, voltage drops across the source resistances will result due to the ongoing bypass capacitor charging currents. The voltage drops will cause a conversion error. Also, the voltage drops increase with higher $|V_{I+} - V_{I-}|$ values, higher source resistances, and lower charge on the bypass capacitors (i.e., faster conversion rate).

For low-source-resistance applications ($R_{source} < 100\ \Omega$), a 0.001-μF bypass capacitor at the inputs will prevent pickup due to the series lead inductance of a long wire. A 100-ohm resistor can be placed between the capacitor and the output of an operational amplifier to isolate the capacitor from the operational amplifier.

input leads

The input leads should be kept as short as possible, since the coupling of noise and digital clock signals to the inputs can cause errors.

power supply considerations

Noise spikes on the V_{CC} lines can cause conversion error. Low-inductance tantalum capacitors ($> 1\ \mu F$) with short leads should be used to bypass ANLG V_{CC} and DGTL V_{CC}. A separate regulator for the TLC1205 or TLC1225 and other analog circuitry will greatly reduce digital noise on the supply line.

positive and negative full-scale adjustment

unipolar inputs

Apply a differential input voltage that is 0.5 LSB below the desired analog full-scale voltage (V_{FS}) and adjust the magnitude of the REF input so that the output code is just changing from 0 1111 1111 1110 to 0 1111 1111 1111. If this transition is desired for a different input voltage, the reference voltage can be adjusted accordingly.

bipolar inputs

First, follow the procedure for the Unipolar case.

Second, apply a differential input voltage so that the digital output code is just changing from 1 0000 0000 0001 to 1 0000 0000 0000. Call this actual differential voltage V_X. The ideal differential voltage for this transition is:

$$-V_{FS} + \frac{V_{FS}}{8192} \quad (1)$$

The difference between the actual and ideal differential voltages is:

$$\text{Delta} = V_X - (-V_{FS} + \frac{V_{FS}}{8192}) \quad (2)$$

Then apply a differential input voltage of:

$$V_X - \frac{\text{Delta}}{2} \quad (3)$$

and adjust V_{ref} so the digital output code is just changing from 1 0000 0000 0001 to 1 0000 0000 0000. This procedure produces positive and negative full-scale transitions with symmetrical minimum error.

TYPICAL APPLICATIONS

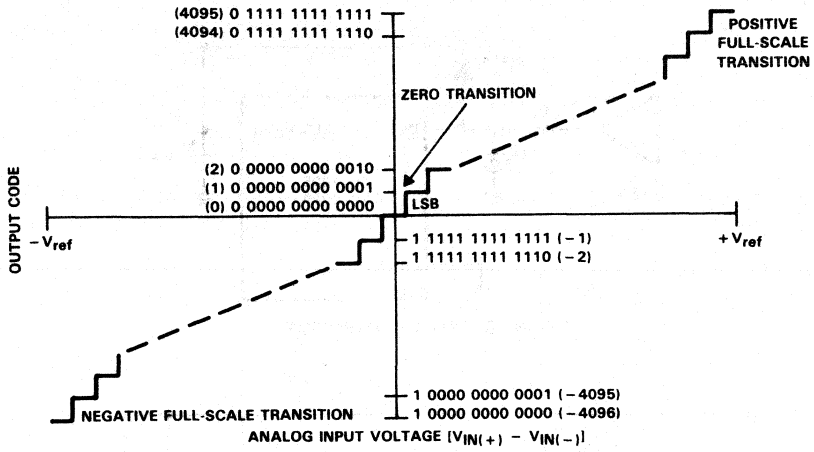
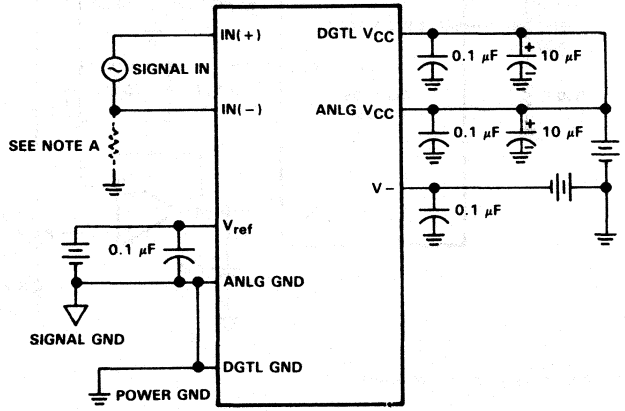


FIGURE 6. TRANSFER CHARACTERISTIC



NOTE: A. The analog input must have some current return path to ANALOG GND.
B. Bypass capacitor leads must be as short as possible.

FIGURE 7. ANALOG CONSIDERATIONS

TYPICAL APPLICATIONS (Continued)

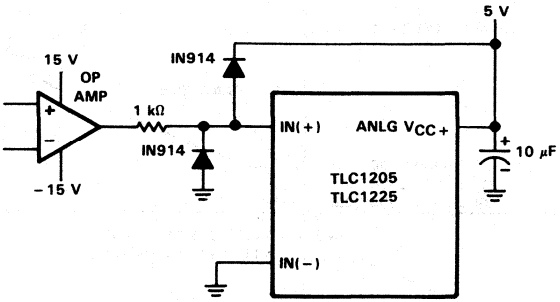
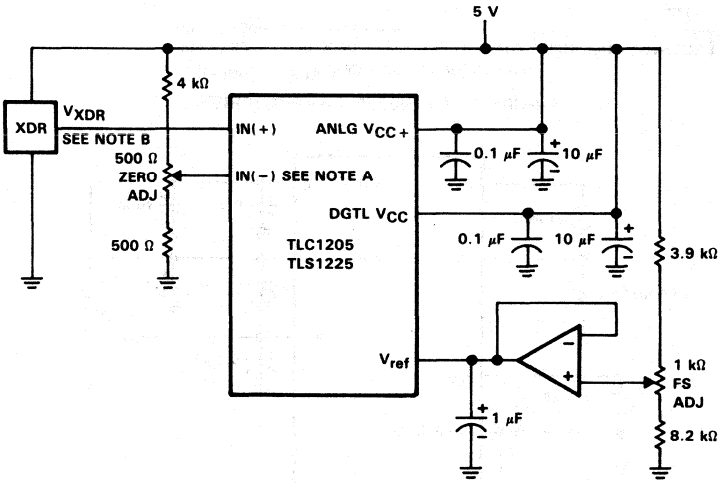


FIGURE 8. INPUT PROTECTION



NOTE: A. $V_{I-} = 0.15 \times \text{ANLG } V_{CC+}$.
B. 15% of ANALOG $V_{CC} \leq V_{XDR} \leq$ 85% of ANALOG V_{CC}.

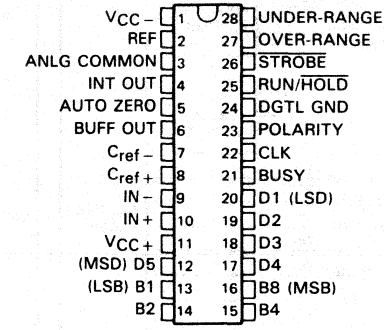
FIGURE 9. OPERATING WITH RATIOMETRIC TRANSDUCERS

TLC7135
Advanced LinCMOS™ 4 1/2-DIGIT PRECISION ANALOG-TO-DIGITAL CONVERTER

D2851, DECEMBER 1986

- ADVANCED LinCMOS™ Technology
- Zero Reading for 0-V Input
- Precision Null Detection with True Polarity at Zero
- 1-pA Typical Input Current
- True Differential Input
- Multiplexed Binary-Coded-Decimal Output
- Low Rollover Error: ±1 Count Maximum
- Control Signals Allow Interfacing with UARTs or Microprocessors
- Autoranging Capability with Over- and Under-Range Signals
- TTL-Compatible Outputs
- Direct Replacement for Teledyne TSC7135, Intersil ICL7135, Maxim ICL7135, and Siliconix Si7135

N
DUAL-IN-LINE PACKAGE
(TOP VIEW)



5

Analog to Digital Converters

Caution. This device has limited built-in gate protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage.

description

The TLC7135 converter is manufactured with Texas Instruments highly efficient ADVANCED LinCMOS™ technology. This 4 1/2-digit dual-slope-integrating analog-to-digital converter is designed to provide interfaces to both a microprocessor and a visual display. The digit-drive outputs D1 through D4 and multiplexed binary-coded-decimal outputs, B1 through B4, provide an interface for LED or LCD decoder/drivers as well as microprocessors.

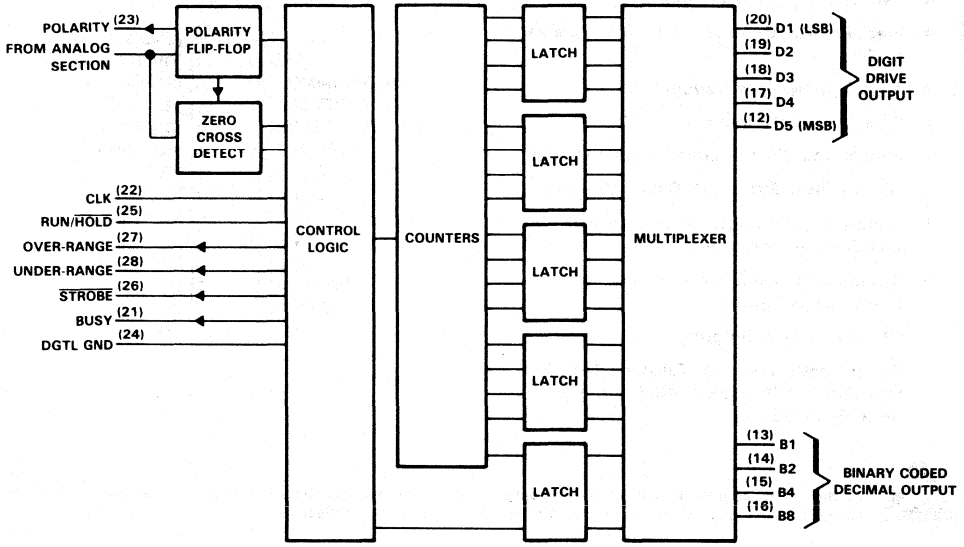
The TLC7135 offers 50-ppm (one part in 20,000) resolution with a maximum linearity error of one count. The zero error is less than 10 μV and zero drift is less than 0.5 μV/°C. Source-impedance errors are minimized by low input current (less than 10 pA). Rollover error is limited to ±1 count.

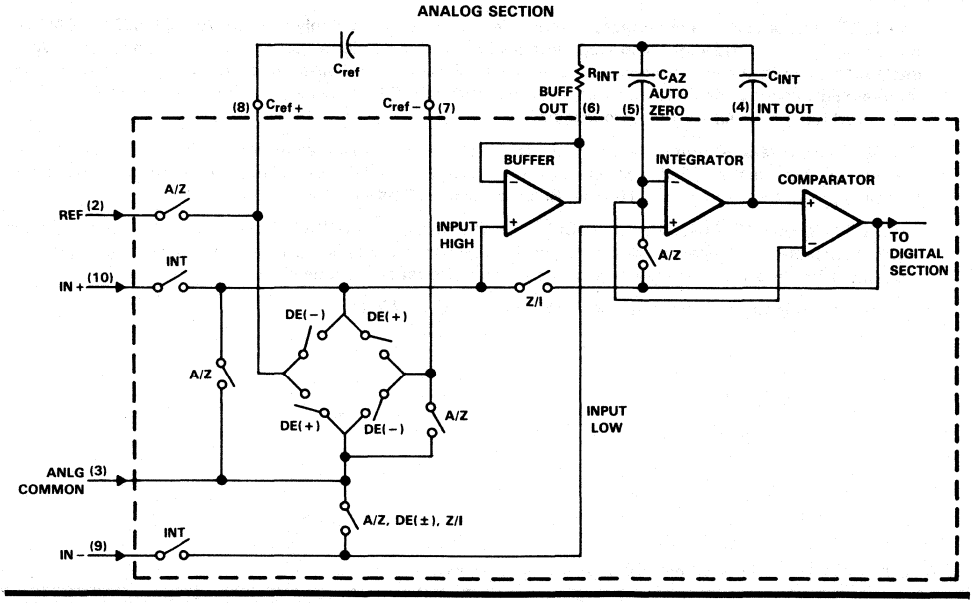
The TLC7135 BUSY, $\overline{\text{STROBE}}$, RUN/$\overline{\text{HOLD}}$, OVER-RANGE, and UNDER-RANGE control signals support microprocessor-based measurement systems. The control signals also can support remote data acquisition systems with data transfer via universal asynchronous receiver transmitters (UARTs).

The TLC7135 is characterized for operation from 0°C to 70°C.

ADVANCED LinCMOS™ is a trademark of Texas Instruments Incorporated.

functional block diagram





absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage (V_{CC+} with respect to V_{CC-}) . . . . . 15 V
Analog input voltage (pin 9 or pin 10) . . . . . V_{CC-} to V_{CC+}
Reference voltage range . . . . . V_{CC-} to V_{CC+}
Clock input voltage range . . . . . 0 V to V_{CC+}
Operating free-air temperature range . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds . . . . . 260°C

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage, V_{CC+}	4	5	6	V
Supply voltage, V_{CC-}	−3	−5	−8	V
Reference voltage, V_{ref}		1		V
High-level input voltage, CLK, RUN/$\overline{HOLD}$, V_{IH}	2.8			V
Low-level input voltage, CLK, RUN/$\overline{HOLD}$, V_{IL}			0.8	V
Differential input voltage, V_{ID}	V_{CC-} +1		V_{CC+} −0.5	V
Maximum operating frequency, f_{clock} (see Note 1)	1.2	2		MHz
Operating free-air temperature range, T_A	0		70	°C

NOTE 1: Clock frequency range extends down to 0 Hz.

electrical characteristics, V_{CC+} = 5 V, V_{CC-} = −5 V, V_{ref} = 1 V, f_{clock} = 120 kHz, T_A = 25°C (unless otherwise noted)

PARAMETER			TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage	D1-D5,B1,B2,B4,B8	I_O = −1 mA		2.4		5	V
		Other outputs	I_O = −10 μA		4.9		5	
V_{OL}	Low-level output voltage		I_O = 1.6 mA				0.4	V
	Peak-to-peak output noise voltage (see Note 2)		V_{ID} = 0,	Full Scale = 2 V		15		μV
α_{VO}	Zero-reading temperature coefficient of output voltage		V_{ID} = 0,	0°C ≤ T_A ≤ 70°C		0.5	2	μV/°C
I_{IH}	High-level input current		V_I = 5 V,	0°C ≤ T_A ≤ 70°C		0.1	10	μA
I_{IL}	Low-level input current		V_I = 0 V,	0°C ≤ T_A ≤ 70°C		−0.02	−0.1	mA
I_I	Input leakage current, pins 9 and 10		V_{ID} = 0	T_A = 25°C		1	10	pA
				0°C ≤ T_A ≤ 70°C			250	
I_{CC+}	Positive supply current		f_{clock} = 0	T_A = 25°C		1	2	mA
				0°C ≤ T_A ≤ 70°C			3	
I_{CC-}	Negative supply current		f_{clock} = 0	T_A = 25°C		−0.8	−2	mA
				0°C ≤ T_A ≤ 70°C			−3	
C_{pd}	Power dissipation capacitance		See Note 3			40		pF

NOTES: 2. This is the peak-to-peak value that is not exceeded 95% of the time.
3. Factor relating clock-frequency to increase in supply current. At V_{CC+} = 5 V

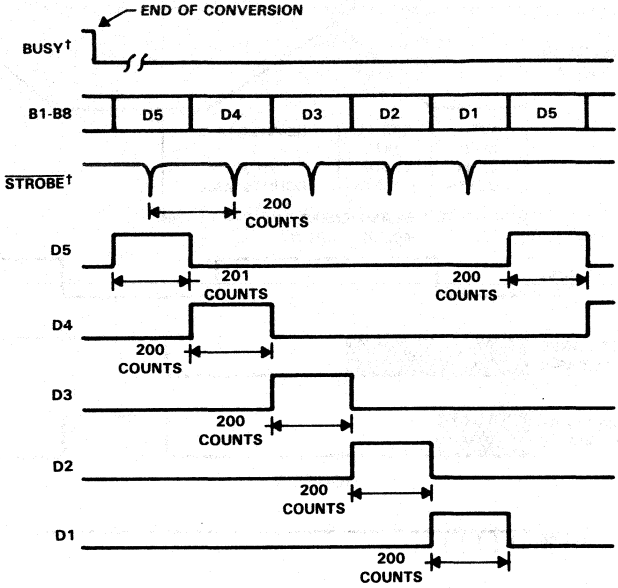
$$I_{CC+} = I_{CC+}(f_{clock} = 0) + C_{pd} \times 5\ V \times f_{clock}$$

operating characteristics, V_{CC+} = 5 V, V_{CC-} = −5 V, V_{ref} = 1 V, f_{clock} = 120 kHz, T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
α_{FS}	Full-scale temperature coefficient (see Note 4)	V_{ID} = 2 V, 0°C ≤ T_A ≤ 70°C			5	ppm/°C
	Linearity error	−2 V ≤ V_{ID} ≤ 2 V		0.5	1	count
	Differential linearity error (see Note 5)	−2 V ≤ V_{ID} ≤ 2 V		0.01		LSB
	± Full-scale symmetry error (see Note 6) (rollover error)	V_{ID} = ±2 V		0.5	1	count
	Display reading with 0-V input	V_{ID} = 0, 0°C ≤ T_A ≤ 70°C	−.0000	±.0000	+.0000	Digital Reading
	Display reading in ratiometric operation	V_{ID} = V_{ref}, T_A = 25°C	+.9998	+.9999	+1.0000	Digital Reading
		0°C ≤ T_A ≤ 70°C	+.9995	+.9999	+1.0005	

NOTES: 4. This parameter is measured with an external reference having a temperature coefficient of less than 0.01 ppm/°C.
5. The magnitude of the difference between the worst case step of adjacent counts and the ideal step.
6. Rollover error is the difference between the absolute values of the conversion for 2 V and −2 V.

timing diagrams



† Delay between BUSY going low and the first STROBE pulse is dependent upon the analog input.

FIGURE 1

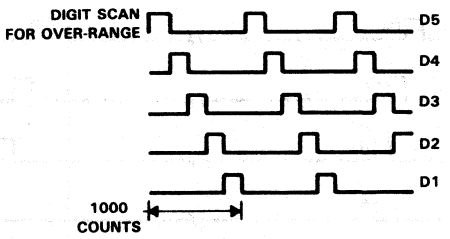


FIGURE 2

timing diagrams (continued)

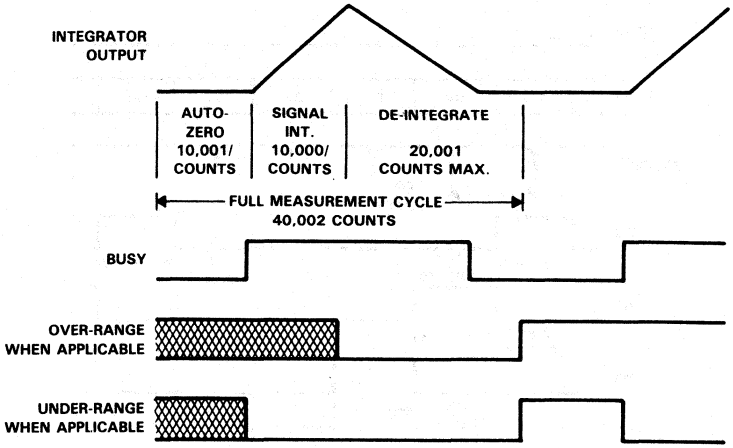
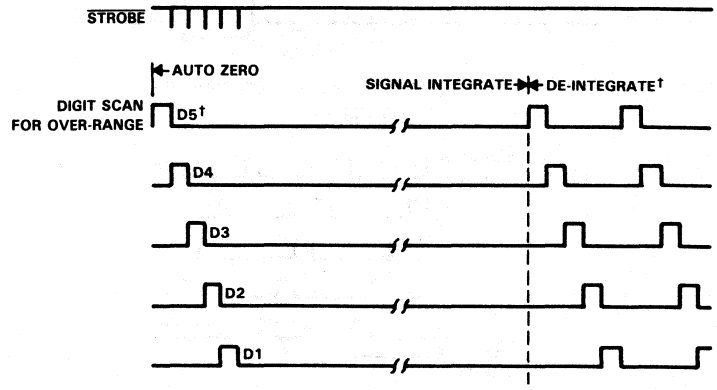


FIGURE 3



†First D5 of AUTO ZERO and DE-INTEGRATE is one count longer.

FIGURE 4

PRINCIPLES OF OPERATION

A measurement cycle for the TLC7135 consists of the following four phases.

1. Auto-Zero Phase. The internal IN+ and IN− inputs are disconnected from the pins and internally connected to ANLG COMMON. The reference capacitor is charged to the reference voltage. The system is configured in a closed loop and the auto-zero capacitor is charged to compensate for offset voltages in the buffer amplifier, integrator, and comparator. The auto-zero accuracy is limited only by the system noise, and the overall offset, as referred to the input, is less than 10 μV.
2. Signal Integrate Phase. The auto-zero loop is opened and the internal IN+ and IN− inputs are connected to the external pins. The differential voltage between these inputs is integrated for a fixed period of time. If the input signal has no return with respect to the converter power supply, IN− can be tied to ANLG COMMON to establish the correct common-mode voltage. Upon completion of this phase, the polarity of the input signal is recorded.
3. De-integrate Phase. The reference is used to perform the de-integrate task. The internal IN− is internally connected to ANLG COMMON and IN+ is connected across the previously charged reference capacitor. The recorded polarity of the input signal is used to ensure that the capacitor will be connected with the correct polarity so that the integrator output polarity will return to zero. The time, which is required for the output to return to zero, is proportional to the amplitude of the input signal. The return time is displayed as a digital reading and is determined by the equation 10,000 x (V_{ID}/V_{ref}). The maximum or full-scale conversion occurs when V_{ID} is two times V_{ref}.
4. Zero Integrator Phase. The internal IN− is connected to ANLG COMMON. The system is configured in a closed loop to cause the integrator output to return to zero. Typically this phase requires 100 to 200 clock pulses. However, after an over-range conversion, 6200 pulses are required.

description of analog circuits

input signal range

The common mode range of the input amplifier extends from 1 V above the negative supply to 1 V below the positive supply. Within this range, the common mode rejection ratio (CMRR) is typically 86 dB. Both differential and common mode voltages cause the integrator output to swing. Therefore, care must be exercised to assure the integrator output does not saturate.

analog common

Analog common (ANLG COMMON) is connected to the internal IN− during the auto-zero, de-integrate, and zero integrator phases. If IN− is connected to a voltage which is different than analog common during the signal integrate phase, the resulting common mode voltage will be rejected by the amplifier. However, in most applications, IN LO will be set at a known fixed voltage (power supply common for instance). In this application, analog common should be tied to the same point, thus removing the common mode voltage from the converter. Removing the common mode voltage in this manner will slightly increase conversion accuracy.

reference

The reference voltage is positive with respect to analog common. The accuracy of the conversion result is dependent upon the quality of the reference. Therefore, to obtain a high accuracy conversion, a high quality reference should be used.

description of digital circuits

RUN/$\overline{\text{HOLD}}$ input

When the RUN/$\overline{\text{HOLD}}$ input is high or open, the device will continuously perform measurement cycles every 40,002 clock pulses. If this input is taken low, the IC will continue to perform the ongoing measurement cycle and then hold the conversion reading for as long as the pin is held low. If the pin is held low after completion of a measurement cycle, a short positive pulse (greater than 300 ns) will initiate a new measurement cycle. If this positive pulse occurs before the completion of a measurement cycle, it will not be recognized. The first STROBE pulse, which occurs 101 counts after the end of a measurement cycle, is an indication of the completion of a measurement cycle. Thus, the positive pulse could be used to trigger the start of a new measurment after the first STROBE pulse.

$\overline{\text{STROBE}}$ input

Negative going pulses from this input are used to transfer the BCD conversion data to external latches, UARTS, or microprocesors. At the end of the measurement cycle, the digit-drive (D5) input goes high and remains high for 201 counts. The most significant digit (MSD) BCD bits are placed on the BCD pins. After the first 101 counts, halfway through the duration of output D1-D5 going high, the $\overline{\text{STROBE}}$ pin goes low for 1/2 clock pulse width. The placement of the $\overline{\text{STROBE}}$ pulse at the midpoint of the D5 high pulse allows the information to be latched into an external device on either a low-level or an edge. Such placement of the $\overline{\text{STROBE}}$ pulse also ensures that the BCD bits for the second MSD will not yet be competing for the BCD lines and latching of the correct bits is assured. The above process is repeated for the second MSD and the D4 output. Similarly, the process is repeated through the least significant digit (LSD). Subsequently, inputs D5 through D1 and the BCD lines will continue scanning without the inclusion of $\overline{\text{STROBE}}$ pulses. This subsequent continuous scanning causes the conversion results to be continuously displayed. Such subsequent scanning does not occur when an over-range condition occurs.

BUSY output

The BUSY output goes high at the beginning of the signal integrate phase and remains high until the first clock pulse after zero-crossing or at the end of the measurement cycle if an over-range condition occurs. It is possible to use the BUSY pin to serially transmit the conversion result. Serial transmission can be accomplished by ANDing the BUSY and CLOCK signals and transmitting the ANDed output. The transmitted output consists of 10,001 clock pulses, which occur during the signal integrate phase, and the number of clock pulses, which occur during the de-integrate phase. The conversion result can be obtained by subtracting 10,001 from the total number of clock pulses.

OVER-RANGE output

When an over-range condition occurs, this pin goes high after the BUSY signal goes low at the end of the measurement cycle. As previously noted, the BUSY signal remains high until the end of the measurement cycle when an over-range condition occurs. The OVER-RANGE output goes high at end of BUSY and goes low at the beginning of the de-integrate phase in the next measurement cycle.

UNDER-RANGE output

At the end of the BUSY signal, this pin goes high if the conversion result is less than or equal to 9% (count of 1800) of the full-scale range. The UNDER-RANGE output is brought low at the beginning of the signal integrate phase of the next measurement cycle.

PRINCIPLES OF OPERATION

POLARITY output

The POLARITY output is high for a positive input signal and is updated at the beginning of each de-integrate phase. The polarity output is valid for all inputs including ±0 and over-range signals.

digit-drive (D5, D4, D2 and D1) outputs

Each digit-drive output (D1 through D5) sequentially goes high for 200 clock pulses. This sequential process is continuous unless an over-range occurs. When an over-range occurs, all of the digit drive outputs are blanked from the end of the strobe sequence until the beginning of the de-integrate phase (when the sequential digit drive activation begins again). The blanking activity, during an over-range condition, may be used to cause the display to flash and indicate the over-range condition.

BCD outputs

The BCD bits (B8, B4, B2 and B1) for a given digit are sequentially activated on these outputs. Simultaneously, the appropriate Digit-drive line for the given digit is activated.

system aspects

integrating resistor

The value of the integrating resistor (R_{INT}) is determined by the full scale input voltage and the output current of the integrating amplifier. The integrating amplifier can supply 20 μA of current with negligible non-linearity. The equation for determining the value of this resistor is as follows:

$$R_{INT} = \frac{\text{FULL-SCALE VOLTAGE}}{I_{INT}}$$

Integrating amplifier current, I_{INT}, from 5 to 40 μA will yield good results. However, the nominal and recommended current is 20 μA.

integrating capacitor

The product of the integrating resistor and capacitor should be selected to give the maximum voltage swing without causing the integrating amplifier output to saturate and get too close to the power supply voltages. If the amplifier output is within 0.3 V of either supply, saturation will occur. With ±5-V supplies and ANLG COMMON connected to ground, the designer should design for a ±3.5-V to ±4-V integrating amplifier swing. A nominal capacitor value is 0.47 μF. The equation for determining the value of the integrating capacitor (C_{INT}) is as follows:

$$C_{INT} = \frac{10{,}000 \times \text{CLOCK PERIOD} \times I_{INT}}{\text{INTEGRATOR OUTPUT VOLTAGE SWING}}$$

where: I_{INT} is nominally 20 μA.

Capacitors with large tolerances and high dielectric absorption can induce conversion inaccuracies. A capacitor, which is too small could cause the integrating amplifier to saturate. High dielectric absorption causes the effective capacitor value to be different during the signal integrate and de-integrate phases. Polypropylene capacitors have very low dielectric absorption. Polystyrene and Polycarbonate capacitors have higher dielectric absorption, but also work well.

PRINCIPLES OF OPERATION

auto-zero and reference capacitor

Large capacitors will tend to reduce noise in the system. Dielectric absorption is unimportant except during power-up or overload recovery. Typical values are 1 μF.

reference voltage

For high-accuracy absolute measurements, a high quality reference should be used.

rollover resistor and diode

The TLC7135 has a small rollover error, however it can be corrected. The correction is to connect the cathode of any silicon diode to the INT OUT pin and the anode to a resistor. The other end of the resistor is connected to ANLG COMMON or ground. For the recommended operating conditions the resistor value is 100 kΩ. This value may be changed to correct any rollover error which has not been corrected. In many non-critical applications, the resistor and diode are not needed.

maximum clock frequency

For most dual-slope A/D converters, the maximum conversion rate is limited by the frequency response of the comparator. In this circuit, the comparator follows the integrator ramp with a 3 μs delay. Therefore, with a 160 kHz clock frequency (6 μs period), half of the first reference integrate clock period is lost in delay. Hence, the meter reading will change from 0 to 1 with a 50 μV input, 1 to 2 with a 150 μV input, 2 to 3 with a 250 μV input, etc. This transition at midpoint is desirable; however, if the clock frequency is increased appreciably above 160 kHz, the instrument will flash "1" on noise peaks even when the input is shorted. The above transition points assume a 2-V input range is equivalent to 20,000 clock cycles.

If the input signal is always of one polarity, comparator delay need not be a limitation. Clock rates of 1 MHz are possible since non-linearity and noise do not increase substantially with frequency. For a fixed clock frequency, the extra count or counts caused by comparator delay will be a constant and can be subtracted out digitally.

For signals with both polarities, the clock frequency can be extended above 160 kHz without error by using a low value resistor in series with the integrating capacitor. This resistor causes the integrator to jump slightly towards the zero-crossing level at the beginning of the de-integrate phase and thus, compensates for the comparator delay. This series resistor should be 10 to 50 ohms. This approach allows clock frequencies up to 480 kHz.

minimum clock frequency

The minimum clock frequency limitations result from capacitor leakage from the auto-zero and reference capacitors. Measurement cycles as high as 10 seconds are not influenced by leakage error.

rejection of 50 Hz or 60 Hz pickup

To maximize the rejection of 50 Hz or 60 Hz pickup, the clock frequency should be chosen so that an integral multiple of 50 Hz or 60 Hz periods occur during the signal integrate phase. To achieve rejection of these signals, some clock frequencies which could be used are as follows:

50 Hz: 250, 166.66, 125, 100 kHz, etc.
60 Hz: 300, 200, 150, 120, 100, 40, 33.33 kHz, etc.

PRINCIPLES OF OPERATION

zero-crossing flip-flop

This flip-flop interrogates the comparator's zero-crossing status. The interrogation is performed after the previous clock cycle and the positive half of the ongoing clock cycle have occurred so that any comparator transients which result from the clock pulses do not affect the detection of a zero-crossing. This procedure delays the zero-crossing detection by one clock cycle. To eliminate the inaccuracy, which is caused by this delay, the counter is disabled for one clock cycle at the beginning of the de-integrate phase. Therefore, when the zero-crossing is detected one clock cycle later than the zero-crossing actually occurs, the correct number of counts is displayed.

noise

The peak-to-peak noise around zero is approximately 15 μV (peak-to-peak value not exceeded 95% of the time). Near full scale, this value increases to approximately 30 μV. Much of the noise originates in the auto-zero loop, and is proportional to the ratio of the input signal to the reference.

analog and digital grounds

For high-accuracy applications, ground loops must be avoided. Return currents from digital circuits must not be sent to the analog ground line.

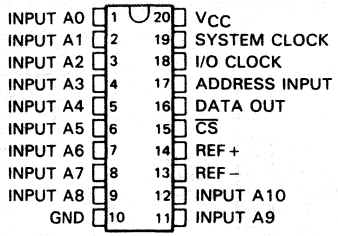
power supplies

The TLC7135 is designed to work with ±5-V power supplies. However, 5-V operation is possible if the input signal does not vary more than ±1.5 V from mid-supply.

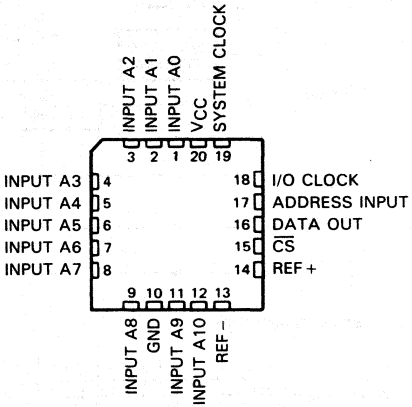
- **LinCMOS™ Technology**
- **10-Bit Resolution A/D Converter**
- **Microprocessor Peripheral or Stand-Alone Operation**
- **On-Chip 12-Channel Analog Multiplexer**
- **Built-In Self-Test Mode**
- **Software-Controllable Sample and Hold**
- **Total Unadjusted Error . . .**
  TLC1540: ±0.5 LSB Max
  TLC1541: ±1.0 LSB Max
- **Pinout and Control Signals Compatible with TLC540 and TLC549 Families of 8-Bit A/D Converters**

TYPICAL PERFORMANCE	
Channel Acquisition Sample Time	5.5 μs
Conversion Time	21 μs
Samples per Second	32×10^3
Power Dissipation	6 mW

J OR N DUAL-IN-LINE PACKAGE
(TOP VIEW)



FK OR FN CHIP CARRIER PACKAGE
(TOP VIEW)



description

The TLC1540 and TLC1541 are LinCMOS™ A/D peripherals built around a 10-bit, switched-capacitor, successive-approximation, A/D converter. They are designed for serial interface to a microprocessor or peripheral via a three-state output with up to four control inputs [including independent System Clock, I/O Clock, Chip Select ($\overline{CS}$), and Address Input]. A 2.1-megahertz system clock for the TLC1540 and TLC1541, with a design that includes simultaneous read/write operation, allows high-speed data transfers and sample rates of up to 32,258 samples per second. In addition to the high-speed converter and versatile control logic, there is an on-chip 12-channel analog multiplexer that can be used to sample any one of 11 inputs or an internal "self-test" voltage, and a sample-and-hold that can operate automatically or under microprocessor control. Detailed information on interfacing to most popular microprocessors is readily available from the factory.

The converters incorporated in the TLC1540 and TLC1541 feature differential high-impedance reference inputs that facilitate ratiometric conversion, scaling, and analog circuitry isolation from logic and supply noises. A totally switched-capacitor design allows guaranteed low-error conversion (±0.5 LSB for the TLC1540, ±1 LSB for the TLC1541) in 21 microseconds over the full operating temperature range.

The TLC1540 and the TLC1541 are available in FK, FN, J, and N packages. The M-suffix versions are characterized for operation from −55°C to 125°C. The I-suffix versions are characterized for operation from −40°C to 85°C.

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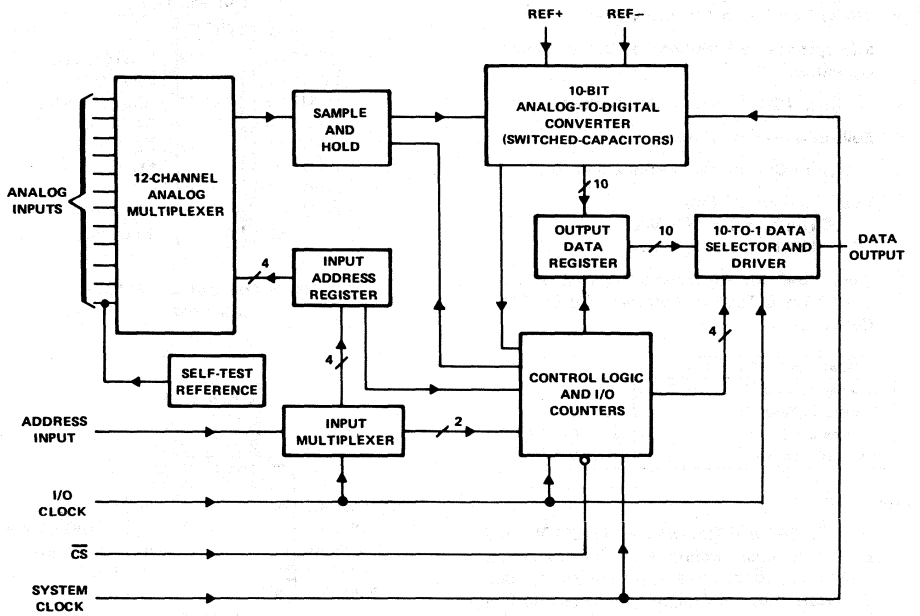
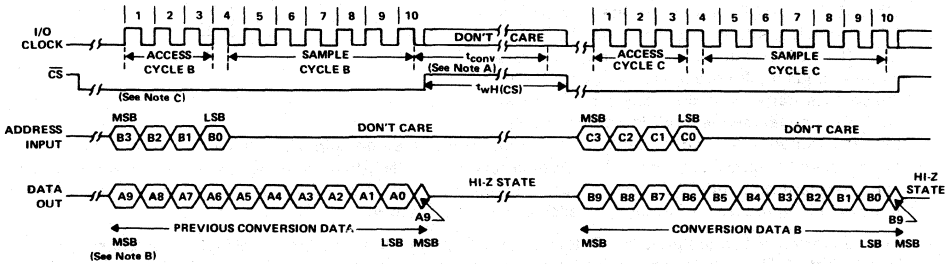
functional block diagram



operating sequence



NOTES: A. The conversion cycle, which requires 44 System Clock periods, is initiated on the 10th falling edge of the I/O Clock↓ after CS↓ goes low for the channel whose address exists in memory at that time. If $\overline{CS}$ is kept low during conversion, the I/O Clock must remain low for at least 44 System Clock cycles to allow conversion to be completed.

B. The most significant bit (MSB) will automatically be placed on the DATA OUT bus after $\overline{CS}$ is brought low. The remaining nine bits (A8-A0) will be clocked out on the first nine I/O Clock falling edges.

C. To minimize errors caused by noise at the CS input, the internal circuitry waits for three System Clock cycles (or less) after a chip-select falling edge is detected before responding to control input signals. Therefore, no attempt should be made to clock-in address data until the minimum chip-select setup time has elapsed.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1)	6.5 V
Input voltage range (any input)	−0.3 V to V_{CC} + 0.3 V
Output voltage range	−0.3 V to V_{CC} + 0.3 V
Peak input current range (any input)	±10 mA
Peak total input current (all inputs)	±30 mA
Operating free-air temperature range: TLC1540I, TLC1541I	−40°C to 85°C
TLC1540M, TLC1541M	−55°C to 125°C
Storage temperature range	−65°C to 150°C
Case temperature for 60 seconds: FK package	260°C
Case temperature for 10 seconds: FN package	260°C
Lead temperature 1,6 mm (1/16 inch) from the case for 60 seconds: J package	300°C
Lead temperature 1,6 mm (1/16 inch) from the case for 10 seconds: N package	260°C

NOTE 1: All voltage values are with respect to digital ground with REF− and GND wired together (unless otherwise noted).

recommended operating conditions

			TLC1540, TLC1541			UNIT
			MIN	NOM	MAX	
Supply voltage, V_{CC}			4.75	5	5.5	V
Positive reference voltage, V_{REF+} (see Note 2)			2.5	V_{CC}	$V_{CC}+0.1$	V
Negative reference voltage, V_{REF-} (see Note 2)			−0.1	0	2.5	V
Differential reference voltage, $V_{REF+} - V_{REF-}$ (see Note 2)			1	V_{CC}	$V_{CC}+0.2$	V
Analog input voltage (see Note 2)			0		V_{CC}	V
High-level control input voltage, V_{IH}			2			V
Low-level control input voltage, V_{IL}					0.8	V
Setup time, address bits before I/O CLK↑, $t_{su(A)}$			400			ns
Hold time, address bits after I/O CLK↑, $t_{h(A)}$			0			ns
Setup time, $\overline{CS}$ low before clocking in first address bit, $t_{su(CS)}$ (see Note 3)			3			System clock cycles
$\overline{CS}$ high during conversion, $t_{wH(CS)}$			44			System clock cycles
Input/Output clock frequency, $f_{CLK(I/O)}$			0		1.1	MHz
System clock frequency, $f_{CLK(SYS)}$			$f_{CLK(I/O)}$		2.1	MHz
System clock high, $t_{wH(SYS)}$			210			ns
System clock low, $t_{wL(SYS)}$			190			ns
Input/Output clock high, $t_{wH(I/O)}$			404			ns
Input/Output clock low, $t_{wL(I/O)}$			404			ns
Clock transition time (see Note 4)	System	$f_{CLK(SYS)} \le 1048$ kHz			30	ns
		$f_{CLK(SYS)} > 1048$ kHz			20	
	I/O	$f_{CLK(I/O)} \le 525$ kHz			100	ns
		$f_{CLK(I/O)} > 525$ kHz			40	
Operating free-air temperature, T_A		TLC1540M, TLC1541M	−55		125	°C
		TLC1540I, TLC1541I	−40		85	

NOTES: 2. Analog input voltages greater than that applied to REF+ convert as all "1"s (11111111), while input voltages less than that applied to REF− convert as all "0"s (00000000). For proper operation, REF+ voltage must be at least 1 volt higher than REF− voltage. Also, the total unadjusted error may increase as this differential reference voltage falls below 4.75 volts.

3. To minimize errors caused by noise at the chip select input, the internal circuitry waits for three System Clock cycles (or less) after a chip select falling edge is detected before responding to control input signals. Therefore, no attempt should be made to clock-in an address until the minimum chip select setup time has elapsed.

4. This is the time required for the clock input signal to fall from V_{IH} min to V_{IL} max or to rise from V_{IL} max to V_{IH} min. In the vicinity of normal room temperature, the devices function with input clock transition time as slow as 2 microseconds for remote data acquisition applications where the sensor and the A/D converter are placed several feet away from the controlling microprocessor.

electrical characteristics over recommended operating temperature range, V_{CC} = V_{REF+} = 4.75 V to 5.5 V (unless otherwise noted), $f_{CLK(I/O)}$ = 1.1 MHz, $f_{CLK(SYS)}$ = 2.1 MHz

PARAMETER			TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{OH}	High-level output voltage (pin 16)		V_{CC} = 4.75 V,	I_{OH} = 360 μA	2.4			V
V_{OL}	Low-level output voltage		V_{CC} = 4.75 V,	I_{OL} = 3.2 mA			0.4	V
I_{OZ}	Off-state (high-impedance state) output current		V_O = V_{CC},	$\overline{CS}$ at V_{CC}			10	μA
			V_O = 0,	$\overline{CS}$ at V_{CC}			−10	
I_{IH}	High-level input current		V_I = V_{CC}			0.005	2.5	μA
I_{IL}	Low-level input current		V_I = 0			−0.005	−2.5	μA
I_{CC}	Operating supply current		$\overline{CS}$ at 0 V			1.2	2.5	mA
	Selected channel leakage current		Selected channel at V_{CC}, Unselected channel at 0 V			0.4	1	μA
			Selected channel at 0 V, Unselected channel at V_{CC}			−0.4	−1	
I_{CC} + I_{REF}	Supply and reference current		V_{REF+} = V_{CC},	$\overline{CS}$ at 0 V		1.3	3	mA
C_i	Input capacitance	Analog inputs				7	55	pF
		Control inputs				5	15	

operating characteristics over recommended operating free-air temperature range, V_{CC} = V_{REF+} = 4.75 V to 5.5 V, $f_{CLK(I/O)}$ = 1.1 MHz, $f_{CLK(SYS)}$ = 2.1 MHz

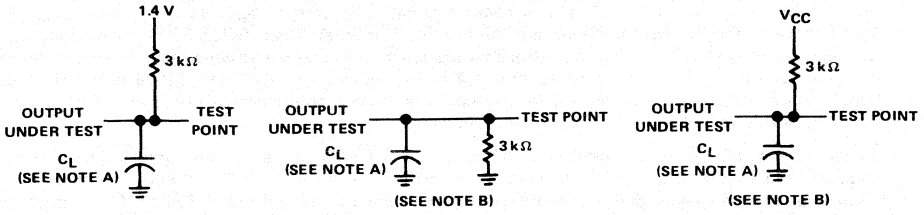
PARAMETER			TEST CONDITIONS	MIN	MAX	UNIT
	Linearity error	TLC1540	See Note 5		±0.5	LSB
		TLC1541			±1	
	Zero error	TLC1540	See Notes 2 and 6		±0.5	LSB
		TLC1541			±1	
	Full-scale error	TLC1540	See Notes 2 and 6		±0.5	LSB
		TLC1541			±1	
	Total unadjusted error	TLC1540	See Note 7		±0.5	LSB
		TLC1541			±1	
	Self-test output code		Input A11 address = 1011 (See Note 8)	0111110100 (500)	1000001100 (524)	
t_{conv}	Conversion time		See Operating Sequence		21	µs
	Total access and conversion time		See Operating Sequence		31	µs
t_{acq}	Channel acquisition time (sample cycle)		See Operating Sequence		6	I/O clock cycles
t_v	Time output data remains valid after I/O clock↓			10		ns
t_d	Delay time, I/O clock↓ to data output valid		See Parameter Measurement Information		400	ns
t_{en}	Output enable time				150	ns
t_{dis}	Output disable time				150	ns
$t_{r(bus)}$	Data bus rise time				300	ns
$t_{f(bus)}$	Data bus fall time				300	ns

† All typical values are at V_{CC} = 5 V, T_A = 25°C.

NOTES: 2. Analog input voltages greater than that applied to REF+ convert to all "1"s (11111111), while input voltages less than that applied to REF− convert to all"0"s (00000000). For proper operation, REF+ voltage must be at least 1 volt higher than REF− voltage. Also, the total unadjusted error may increase as this differential reference voltage falls below 4.75 volts.

5. Linearity error is the maximum deviation from the best straight line through the A/D transfer characteristics.
6. Zero error is the difference between 00000000 and the converted output for zero input voltage; full-scale error is the difference between 11111111 and the converted output for full-scale input voltage.
7. Total unadjusted error comprises linearity, zero, and full-scale errors.
8. Both the input address and the output codes are expressed in positive logic. The A11 analog input signal is internally generated and is used for test purposes.

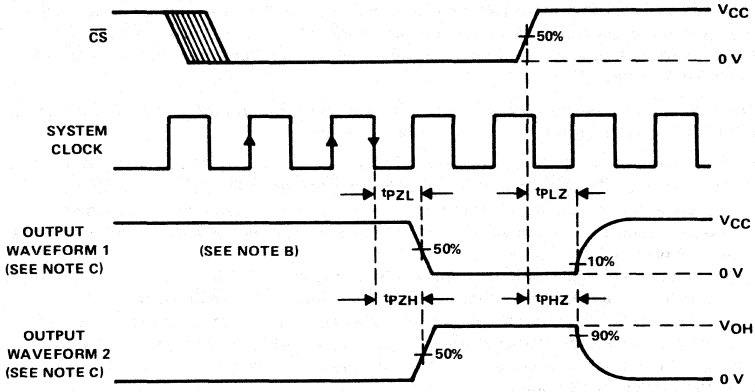
PARAMETER MEASUREMENT INFORMATION



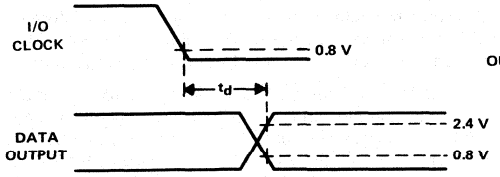
LOAD CIRCUIT FOR t_d, t_r, AND t_f

LOAD CIRCUIT FOR t_{PZH} AND t_{PHZ}

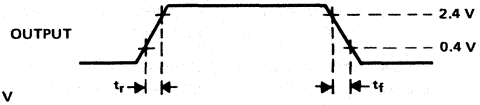
LOAD CIRCUIT FOR t_{PZL} AND t_{PLZ}



VOLTAGE WAVEFORMS FOR ENABLE AND DISABLE TIMES



VOLTAGE WAVEFORM FOR DELAY TIME



VOLTAGE WAVEFORM FOR RISE AND FALL TIMES

NOTES: A. C_L = 50 pF
B. t_{en} = t_{PZH} or t_{PZL}, t_{dis} = t_{PHZ} or t_{PLZ}.
C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.

principles of operation

The TLC1540 and TLC1541 are complete data acquisition systems on single chips. Each includes such functions as sample-and-hold, 10-bit A/D converter, data and control registers, and control logic. For flexibility and access speed, there are four control inputs; Chip Select ($\overline{CS}$), Address Input, I/O Clock, and System Clock. These control inputs and a TTL-compatible three-state output are intended for serial communications with a microprocessor or microcomputer. The TLC1540 and TLC1541 can complete conversions in a maximum of 21 microseconds, while complete input-conversion-output cycles can be repeated at a maximum of 31 microseconds.

The System and I/O Clocks are normally used independently and do not require any special speed or phase relationships between them. This independence simplifies the hardware and software control tasks for the device. Once a clock signal within the specification range is applied to the System Clock input, the control hardware and software need only be concerned with addressing the desired analog channel, reading the previous conversion result, and starting the conversion by using the I/O Clock. The System Clock will drive the "conversion crunching" circuitry so that the control hardware and software need not be concerned with this task.

When $\overline{CS}$ is high, the Data Output pin is in a three-state condition and the Address Input and I/O Clock pins are disabled. This feature allows each of these pins, with the exception of the $\overline{CS}$ pin, to share a control logic point with their counterpart pins on additional A/D devices when additional TLC1540/1541 devices are used. In this way, the above feature serves to minimize the required control logic pins when using multiple A/D devices.

The control sequence has been designed to minimize the time and effort required to initiate conversion and obtain the conversion result. A normal control sequence is:

1. $\overline{CS}$ is brought low. To minimize errors caused by noise at the $\overline{CS}$ input, the internal circuitry waits for two rising edges and then a falling edge of the System Clock after a low $\overline{CS}$ transition, before the low transition is recognized. This technique is used to protect the device against noise when the device is used in a noisy environment. The MSB of the previous conversion result will automatically appear on the Data Out pin.
2. A new positive-logic multiplexer address is shifted in on the first four rising edges of the I/O Clock. The MSB of the address is shifted in first. The negative edges of these four I/O Clock pulses shift out the second, third, fourth, and fifth most significant bits of the previous conversion result. The on-chip sample-and-hold begins sampling the newly addressed analog input after the fourth falling edge. The sampling operation basically involves the charging of internal capacitors to the level of the analog input voltage.
3. Five clock cycles are then applied to the I/O pin and the sixth, seventh, eighth, ninth, and tenth conversion bits are shifted out on the negative edges of these clock cycles.
4. The final tenth clock cycle is applied to the I/O Clock pin. The falling edge of this clock cycle completes the analog sampling process and initiates the hold function. Conversion is then performed during the next 44 System Clock cycles. After this final I/O Clock cycle, $\overline{CS}$ must go high or the I/O Clock must remain low for at least 44 System Clock cycles to allow for the conversion function.

$\overline{CS}$ can be kept low during periods of multiple conversion. When keeping $\overline{CS}$ low during periods of multiple conversion, special care must be exercised to prevent noise glitches on the I/O Clock line. If glitches occur on the I/O Clock line, the I/O sequence between the microprocessor/controller and the device will lose synchronization. Also, if $\overline{CS}$ is taken high, it must remain high until the end of the conversion. Otherwise, a valid falling edge of $\overline{CS}$ will cause a reset condition, which will abort the conversion in progress.

A new conversion may be started and the ongoing conversion simultaneously aborted by performing steps 1 through 4 before the 44 System Clock cycles occur. Such action will yield the conversion result of the previous conversion and not the ongoing conversion.

principles of operation (continued)

It is possible to connect the System and I/O Clock pins together in special situations in which controlling circuitry points must be minimized. In this case, the following special points must be considered in addition to the requirements of the normal control sequence previously described.

1. When $\overline{CS}$ is recognized by the device to be at a low level, the common clock signal is used as an I/O Clock. When $\overline{CS}$ is recognized by the device to be at a high level, the common clock signal is used to drive the "conversion crunching" circuitry.
2. The device will recognize a $\overline{CS}$ low transition only when the $\overline{CS}$ input changes and subsequently the System Clock pin receives two positive edges and then a negative edge. For this reason, after a $\overline{CS}$ negative edge, the first two clock cycles will not shift in the address because a low $\overline{CS}$ must be recognized before the I/O Clock can shift in an analog channel address. Also, upon shifting in the address, $\overline{CS}$ must be raised after the eighth I/O Clock that has been recognized by the device, so that a $\overline{CS}$ low level will be recognized upon the lowering of the tenth I/O Clock signal that is recognized by the device. Otherwise, additional common clock cycles will be recognized as I/O Clock pulses and will shift in an erroneous address.

For certain applications, such as strobing applications, it is necessary to start conversion at a specific point in time. This device will accommodate these applications. Although the on-chip sample-and-hold begins sampling upon the negative edge of the fourth I/O Clock cycle, the hold function is not initiated until the negative edge of the tenth I/O Clock cycle. Thus, the control circuitry can leave the I/O Clock signal in its high state during the tenth I/O Clock cycle until the moment at which the analog signal must be converted. The TLC1540/TLC1541 will continue sampling the analog input until the tenth falling edge of the I/O Clock. The control circuitry or software will then immediately lower the I/O Clock signal and hold the analog signal at the desired point in time and start conversion.

Detailed information on interfacing to most popular microprocessors is readily available from the factory.

General Information 1

Operational Amplifiers 2

Voltage Comparators 3

Timers 4

Analog to Digital Converters 5

Digital to Analog Converters 6

Analog Switches 7

Switched Capacitor Filters 8

Packaging Information 9

DIGITAL TO ANALOG CONVERTERS

	LINEARITY ERROR	SELLING TIME TO ½ LSB (nS)	PROPAGATION DELAY 90% OF FINAL OUTPUT (nS)	CS SETUP TIME (nS)	DATA BUS INPUT SETUP TIME (nS)	MAX POWER DISSIPATION @ 5V (mW)	RESOLUTION (Bits)	PAGE No.
Single								
TLC7524	± 0.5 LSB	100	80	40	25	5	8	6-5
TLC7533	± 0.5 LSB	150			30	10	10	6-25
Dual								
TLC7528	± 0.5 LSB	100	80	50	25	5	8	6-13

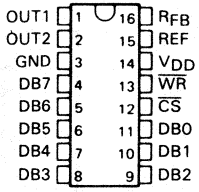
ADVANCE INFORMATION

TLC7524
Advanced LinCMOS™ 8-BIT MULTIPLYING DIGITAL-TO-ANALOG CONVERTER

D3008, SEPTEMBER 1986

- **Advanced LinCMOS™ Silicon-Gate Technology**
- **Easily Interfaced to Microprocessors**
- **On-Chip Data Latches**
- **Guaranteed Monotonicity**
- **Segmented High-Order Bits Ensure Low-Glitch Output**
- **Designed to be Interchangeable with Analog Devices AD7524, PMI PM-7524, and Micro Power Systems MP7524**
- **Fast Control Signaling for Digital Signal Processor Applications Including Interface with TMS320**

D OR N PACKAGE
(TOP VIEW)



KEY PERFORMANCE SPECIFICATIONS	
Resolution	8 Bits
Linearity error	½ LSB Max
Power dissipation at V_{DD} = 5 V	5 mW Max
Settling time	100 ns Max
Propagation delay	80 ns Max

description

The TLC7524 is an Advanced LinCMOS™ 8-bit digital-to-analog converter (DAC) designed for easy interface to most popular microprocessors.

The TLC7524 is an 8-bit multiplying DAC with input latches and with a load cycle similar to the "write" cycle of a random access memory. Segmenting the high-order bits minimizes glitches during changes in the most-significant bits, which produce the highest glitch impulse. The TLC7524 provides accuracy to ½ LSB without the need for thin-film resistors or laser trimming, while dissipating less than 5 milliwatts typically.

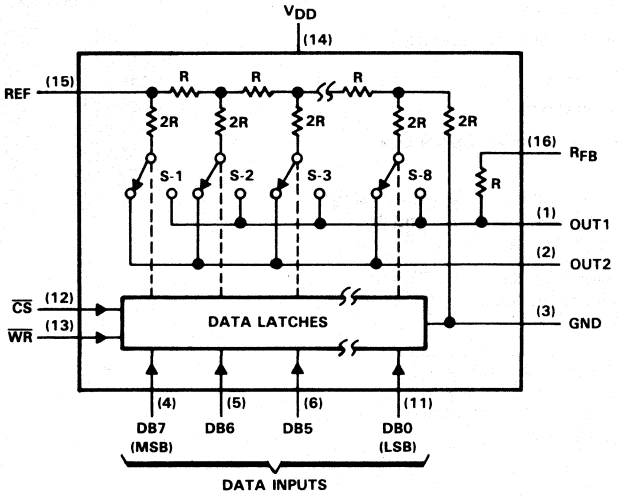
Featuring operation from a 5-V to 15-V single supply, the TLC7524 interfaces easily to most microprocessor buses or output ports. Excellent multiplying (2 or 4 quadrant) makes the TLC7524 an ideal choice for many microprocessor-controlled gain-setting and signal-control applications.

The TLC7524I is characterized for operation from −25°C to 85°C, and the TLC7524C is characterized for operation from 0°C to 70°C.

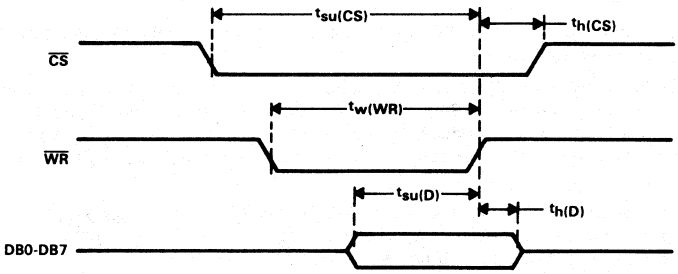
Advanced LinCMOS is a trademark of Texas Instruments Incorporated.

TEXAS INSTRUMENTS

functional block diagram



operating sequence



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{DD} . . . . . −0.3 V to 16.5 V
Digital input voltage, V_I . . . . . −0.3 V to V_{DD} + 0.3 V
Reference voltage, V_{ref} . . . . . ±25 V
Peak digital input current, I_I . . . . . 10 μA
Operating free-air temperature range: TLC7524I . . . . . −25°C to 85°C
TLC7524C . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds . . . . . 260°C

recommended operating conditions

		V_{DD} = 5 V			V_{DD} = 15 V			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{DD}		4.75	5	5.25	14.5	15	15.5	V
Reference voltage, V_{ref}			±10			±10		V
High-level input voltage, V_{IH}		2.4			13.5			V
Low-level input voltage, V_{IL}				0.8			1.5	V
CS setup time, $t_{su(CS)}$		40			40			ns
CS hold time, $t_{h(CS)}$		0			0			ns
Data bus input setup time, $t_{su(D)}$		25			25			ns
Data bus input hold time, $t_{h(D)}$		10			10			ns
Pulse duration, $\overline{WR}$ low, $t_{w(WR)}$		40			40			ns
Operating free-air temperature, T_A	TLC7524I	−25		85	−25		85	°C
	TLC7524C	0		70	0		70	

electrical characteristics over recommended operating free-air temperature range, V_{ref} = ±10 V, OUT1 and OUT2 at GND (unless otherwise noted)

PARAMETER			TEST CONDITIONS	V_{DD} = 5 V			V_{DD} = 15 V			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
I_{IH}	High-level input current		$V_I = V_{DD}$			10			10	μA
I_{IL}	Low-level input current		V_I = 0			−10			−10	μA
	Output leakage current, OUT1 (Pin 1)		DB0-DB7 at 0 V, $\overline{WR}$, $\overline{CS}$ at 0 V, V_{ref} = ±10 V			±400			±200	nA
	Output leakage current, OUT2 (Pin 2)		DB0-DB7 at V_{DD}, $\overline{WR}$, $\overline{CS}$ at 0 V, V_{ref} = ±10 V			±400			±200	nA
I_{DD}	Supply current (quiescent)		DB0-DB7 at $V_{IH(min)}$ or $V_{IL(max)}$			1			2	mA
I_{DD}	Supply current (standby)		DB0-DB7 at 0 V or V_{DD}			500			500	μA
k_{SVS}	Supply voltage sensitivity, $\Delta gain/\Delta V_{DD}$		ΔV_{DD} = ±10%		0.01	0.16		0.005	0.04	%FSR
C_i	Input capacitance, DB0-DB7, $\overline{WR}$, $\overline{CS}$		V_I = 0			5			5	pF
C_o	Output capacitance.	OUT1	DB0-DB7 at 0 V, $\overline{WR}$ and $\overline{CS}$ at 0 V			30			30	pF
		OUT2				120			120	
C_o	Output capacitance	OUT1	DB0-DB7 at V_{DD}, $\overline{WR}$ and $\overline{CS}$ at 0 V			120			120	pF
		OUT2				30			30	
	Reference input impedance (Pin 15 to GND)			5		20	5		20	kΩ

operating characteristics over recommended operating free-air temperature range, V_{ref} = ±10 V, OUT1 and OUT2 at GND (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{DD} = 5 V			V_{DD} = 15 V			UNIT
		MIN	TYP†	MAX	MIN	TYP†	MAX	
Linearity error				±0.5			±0.5	LSB
Gain error	See Note 1			±2.5			±2.5	LSB
Settling time (to ½ LSB)	See Note 2			100			100	ns
Propagation delay (from digital input to 90% of final analog output current)	See Note 2			80			80	ns
Feedthrough at OUT1 or OUT2	V_{ref} = ±10 V (100-kHz sinewave) $\overline{WR}$ and $\overline{CS}$ at 0 V, DB0-DB7 at 0 V			0.5			0.5	%FSR
Temperature coefficient of gain	T_A = 25°C to MAX		±0.004			±0.001		%FSR/°C

†Typical values at T_A = 25°C.

NOTES: 1. Gain error is measured using the internal feedback resistor. Nominal Full Scale Range (FSR) = V_{ref} − 1 LSB.
2. OUT1 load = 100 Ω, C_{ext} = 13 pF, $\overline{WR}$ at 0 V, $\overline{CS}$ at 0 V, DB0-DB7 at 0 V to V_{DD} or V_{DD} to 0 V.

principles of operation

The TLC7524 is an 8-bit multiplying D/A converter consisting of an inverted R-2R ladder, analog switches, and data input latches. Binary weighted currents are switched between the OUT1 and OUT2 bus lines, thus maintaining a constant current in each ladder leg independent of the switch state. The high-order bits are decoded and these decoded bits, through a modification in the R-2R ladder, control three equally weighted current sources. Most applications only require the addition of an external operational amplifier and a voltage reference.

The equivalent circuit for all digital inputs low is seen in Figure 1. With all digital inputs low, the entire reference current, I_{ref}, is switched to OUT2. The current source I/256 represents the constant current flowing through the termination resistor of the R-2R ladder, while the current source I_{lkg} represents leakage currents to the substrate. The capacitances appearing at OUT1 and OUT2 are dependent upon the digital input code. With all digital inputs high, the off-state switch capacitance (30 pF maximum) appears at OUT2 and the on-state switch capacitance (120 pF maximum) appears at OUT1. With all digital inputs low, the situation is reversed as shown in Figure 1. Analysis of the circuit for all digital inputs high is similar to Figure 1; however, in this case, I_{ref} would be switched to OUT1.

Interfacing the TLC7524 D/A converter to a microprocessor is accomplished via the data bus and the $\overline{CS}$ and $\overline{WR}$ control signals. When $\overline{CS}$ and $\overline{WR}$ are both low, the TLC7524 analog output responds to the data activity on the DB0-DB7 data bus inputs. In this mode, the input latches are transparent and input data directly affects the analog output. When either the $\overline{CS}$ signal or $\overline{WR}$ signal goes high, the data on the DB0-DB7 inputs are latched until the $\overline{CS}$ and $\overline{WR}$ signals go low again. When $\overline{CS}$ is high, the data inputs are disabled regardless of the state of the $\overline{WR}$ signal.

The TLC7524 is capable of performing 2-quadrant or full 4-quadrant multiplication. Circuit configurations for 2-quadrant or 4-quadrant multiplication are shown in Figures 2 and 3. Input coding for unipolar and bipolar operation are summarized in Tables 1 and 2, respectively.

principles of operation (continued)

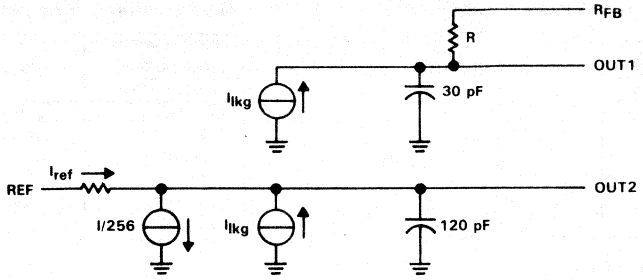


FIGURE 1. TLC7524 EQUIVALENT CIRCUIT WITH ALL DIGITAL INPUTS LOW

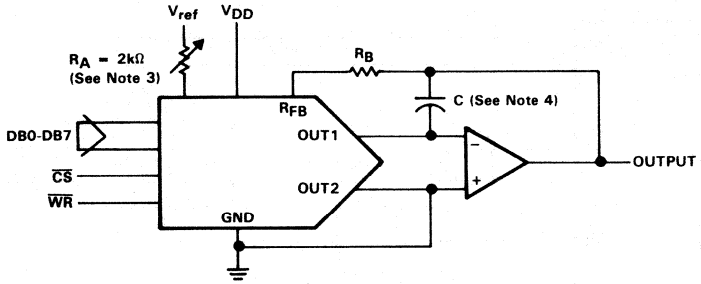


FIGURE 2. UNIPOLAR OPERATION (2-QUADRANT MULTIPLICATION)

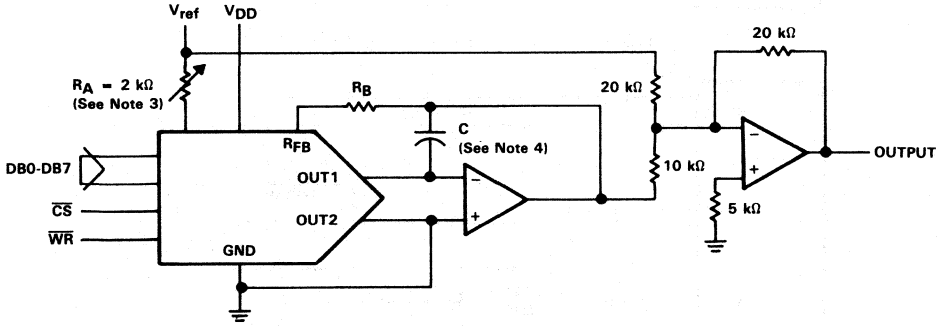


FIGURE 3. BIPOLAR OPERATION (4-QUADRANT OPERATION)

NOTES: 3. R_A and R_B used only if gain adjustment is required.
4. C phase compensation (10-15 pF) is required when using high-speed amplifiers to prevent ringing or oscillation.

principles of operation (continued)

TABLE 1. UNIPOLAR BINARY CODE

DIGITAL INPUT (SEE NOTE 5) MSB LSB	ANALOG OUTPUT
11111111	$-V_{ref}$ (255/256)
10000001	$-V_{ref}$ (129/256)
10000000	$-V_{ref}$ (128/256) = $-V_{ref}/2$
01111111	$-V_{ref}$ (127/256)
00000001	$-V_{ref}$ (1/256)
00000000	0

TABLE 2. BIPOLAR (OFFSET BINARY) CODE

DIGITAL INPUT (SEE NOTE 6) MSB LSB	ANALOG OUTPUT
11111111	V_{ref} (127/128)
10000001	V_{ref} (1/128)
10000000	0
01111111	$-V_{ref}$ (1/128)
00000001	$-V_{ref}$ (127/128)
00000000	$-V_{ref}$

NOTES: 5. LSB = 1/256 (V_{ref}).
6. LSB = 1/128 (V_{ref}).

microprocessor interfaces

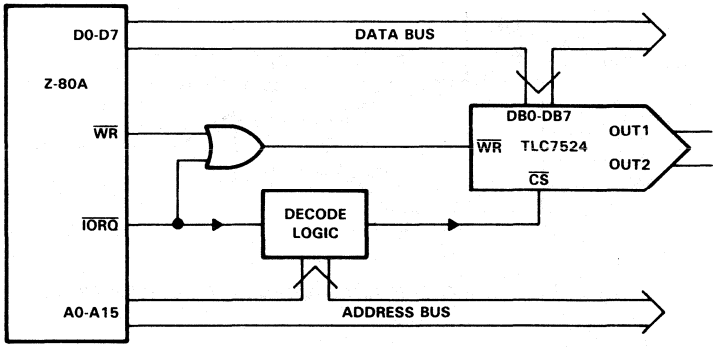


FIGURE 4. TLC7524—Z-80A INTERFACE

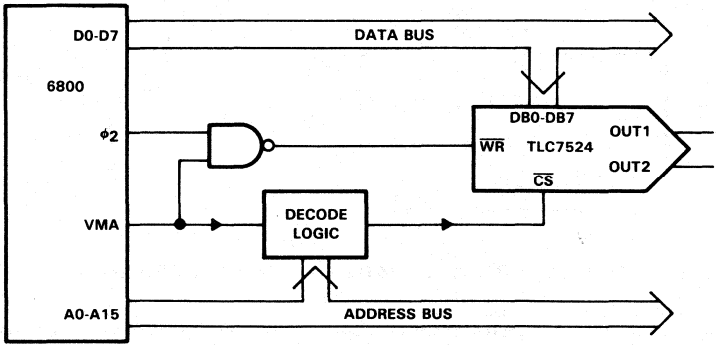


FIGURE 5. TLC7524—6800 INTERFACE

microprocessor interfaces (continued)

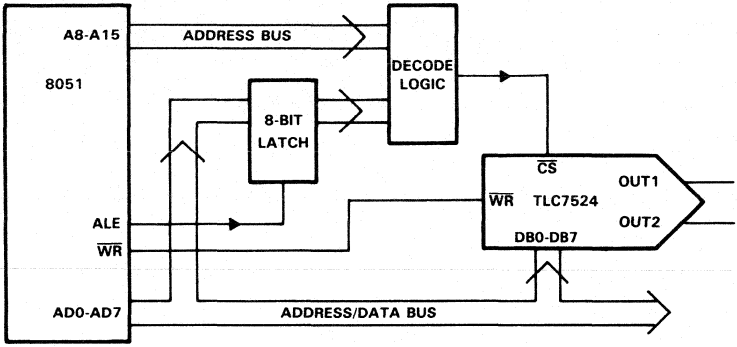
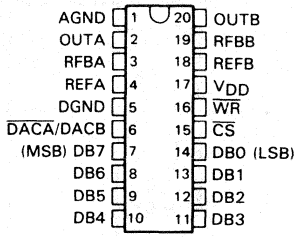


FIGURE 6. TLC7524–8051 INTERFACE

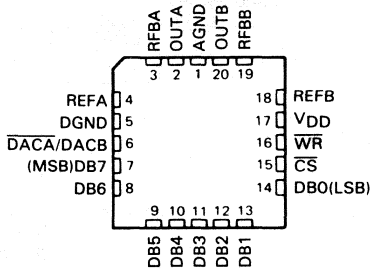
- **ADVANCED LinCMOS™ Silicon-Gate Technology**
- **Easily Interfaced to Microprocessors**
- **On-Chip Data Latches**
- **Guaranteed Monotonicity**
- **Designed to be Interchangeable with Analog Devices AD7528 and PMI PM-7528**
- **Fast Control Signaling for Digital Signal Processor Applications Including Interface with TMS320**

DW OR N PACKAGE
(TOP VIEW)



KEY PERFORMANCE SPECIFICATIONS	
Resolution	8 bits
Linearity Error	1/2 LSB
Power Dissipation at V_{DD} = 5 V	5 mW
Settling Time at V_{DD} = 5 V	100 ns
Propagation Delay at V_{DD} = 5 V	80 ns

FN PACKAGE
(TOP VIEW)



description

The TLC7528 is a dual 8-bit digital-to-analog converter designed with separate on-chip data latches and featuring excellent DAC-to-DAC matching. Data is transferred to either of the two DAC data latches via a common 8-bit input port. Control input DACA/DACB determines which DAC is to be loaded. The "load" cycle of the TLC7528 is similar to the "write" cycle of a random-access memory, allowing easy interface to most popular microprocessor busses and output ports. Segmenting the high-order bits minimizes glitches during changes in the most significant bits, where glitch impulse is typically the strongest.

The TLC7528 operates from a 5-volt to 15-volt power supply and dissipates less than 15 mW (typical). Excellent 2- or 4-quadrant multiplying makes the TLC7528 a sound choice for many microprocessor-controlled gain-setting and signal-control applications.

The TLC7528I is characterized for operation from −25 to 85°C. The TLC7528C is characterized for operation from 0°C to 70°C.

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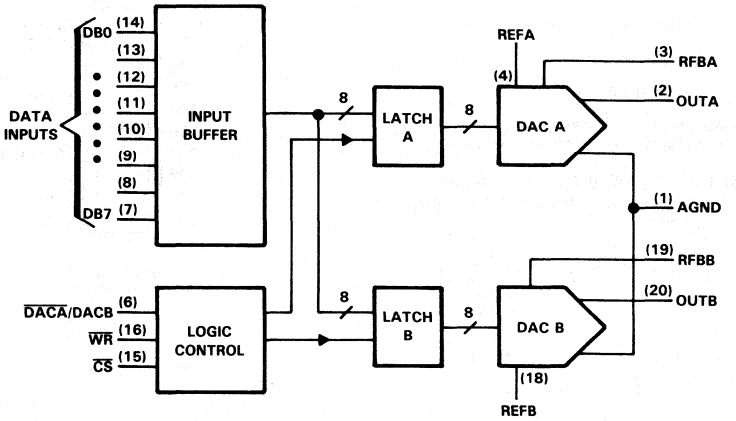
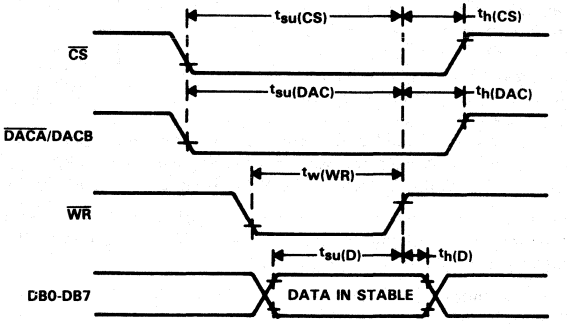
functional block diagram



operating sequence



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{DD} (to AGND or DGND) . . . . . −0.3 V to 16.5 V
Voltage between AGND and DGND . . . . . ±V_{DD}
Input voltage, V_I (to DGND) . . . . . −0.3 V to V_{DD}+0.3
Reference voltage, V_{refA} or V_{refB} (to AGND) . . . . . ±25 V
Output voltage, V_{OA} or V_{OB} (to AGND) . . . . . ±25 V
Peak input current . . . . . 10 μA
Operating free-air temperature range: TLC7528I . . . . . −25°C to 85°C
TLC7528C . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C
Case temperature for 10 seconds: FN package . . . . . 260°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: DW or N package . . . . . 260°C

recommended operating conditions

		V_{DD} = 4.75 V to 5.25 V			V_{DD} = 14.5 V to 15.5 V			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
Reference voltage, V_{refA} or V_{refB}			±10			±10		V
High-level input voltage, V_{IH}		2.4			13.5			V
Low-level input voltage, V_{IL}				0.8			1.5	V
$\overline{CS}$ setup time, $t_{su(CS)}$		50			50			ns
$\overline{CS}$ hold time, $t_{h(CS)}$		0			0			ns
DAC select setup time, $t_{su(DAC)}$		50			50			ns
DAC select hold time, $t_{h(DAC)}$		10			10			ns
Data bus input setup time $t_{su(D)}$		25			25			ns
Data bus input hold time $t_{h(D)}$		0			0			ns
Pulse duration, $\overline{WR}$ low, $t_{w(WR)}$		50			50			ns
Operating free-air temperature, T_A	TLC7528I	−25		85	−25		85	°C
	TLC7528C	0		70	0		70	

electrical characteristics over recommended operating free-air temperature range, V_{refA} = V_{refB} = 10 V, V_{OA} and V_{OB} at 0 V (unless otherwise noted)

PARAMETER			TEST CONDITIONS	V_{DD} = 5 V			V_{DD} = 15 V			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
I_{IH}	High-level input current		V_I = V_{DD}			10			10	μA
I_{IL}	Low-level input current		V_I = 0 V			−10			−10	μA
	Reference input impedance (Pin 15 to GND)			5	12	20	5	12	20	kΩ
I_{lkg}	Output leakage current	OUTA	DACA data latch loaded with 00000000, V_{refA} = ±10 V			±400			±200	nA
		OUTB	DACB data latch loaded with 00000000, V_{refB} = ±10 V			±400			±200	
	Input resistance match (REFA to REFB)					±1%			±1%	
	DC supply sensitivity, Δ gain/Δ V_{DD}		ΔV_{DD} = ±10%			0.04			0.02	%/%
I_{DD}	Supply current (quiescent)		DB0-DB7 at V_{IH}min or V_{IL}max			1			1	mA
I_{DD}	Supply current (standby)		DB0-DB7 at 0 V or V_{DD}			0.5			0.5	mA
C_i	Input capacitance	DB0-DB7				10			10	pF
		$\overline{WR}$, $\overline{CS}$ $\overline{DACA}$/DACB				15			15	
C_o	Output capacitance, (OUTA, OUTB)		DAC data latches loaded with 00000000			50			50	pF
			DAC data latches loaded with 11111111			120			120	

†All typical values are at T_A = 25°C.

operating characteristics over recommended operating free-air temperature range, V_{refA} = V_{refB} = 10 V, V_{OA} and V_{OB} at 0 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{DD} = 5 V			V_{DD} = 15 V			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
Linearity error					±1/2			±1/2	LSB
Settling time (to 1/2 LSB)		See Note 1			100			100	ns
Gain error		See Note 2			2.5			2.5	LSB
AC feedthrough	REFA to OUTA	See Note 3			−65			−65	dB
	REFB to OUTB				−65			−65	
Temperature coefficient of gain		See Note 4			0.007			0.0035	%FSR/°C
Propagation delay (from digital input to 90% of final analog output current)		See Note 5			80			80	ns
Channel-to-channel isolation	REFA to OUTB	See Note 6		77			77		dB
	REFB to OUTA	See Note 7		77			77		
Digital-to-analog glitch impulse area		Measured for code transition from 00000000 to 11111111, T_A = 25°C		160			440		nVs
Digital crosstalk glitch impulse area		Measured for code transition from 00000000 to 11111111, T_A = 25°C		30			60		nVs
Harmonic distortion		V_i = 6 V rms, f = 1 kHz, T_A = 25°C		−85			−85		dB

NOTES: 1. OUTA, OUTB load = 100 Ω, C_{ext} = 13 pF; $\overline{WR}$ and $\overline{CS}$ at 0 V; DB0-DB7 at 0 V to V_{DD} or V_{DD} to 0 V.
2. Gain error is measured using an internal feedback resistor. Nominal Full Scale Range (FSR) = V_{ref} − 1 LSB.
3. V_{ref} = 20 V peak-to-peak, 100-kHz sine wave; DAC data latches loaded with 00000000.
4. Temperature coefficient of gain measured from 0°C to 25°C or from 25°C to 70°C.
5. V_{refA} = V_{refB} = 10 V; OUTA/OUTB load = 100 Ω, C_{ext} = 13 pF; $\overline{WR}$ and $\overline{CS}$ at 0 V; DB0-DB7 at 0 V to V_{DD} or V_{DD} to 0 V.
6. Both DAC latches loaded with 11111111; V_{refA} = 20 V peak-to-peak, 100-kHz sine wave; V_{refB} = 0; T_A = 25°C.
7. Both DAC latches loaded with 11111111; V_{refB} = 20 V peak-to-peak, 100-kHz sine wave; V_{refA} = 0; T_A = 25°C.

principles of operation

The TLC7528 contains two identical 8-bit multiplying D/A converters, DACA and DACB. Each DAC consists of an inverted R-2R ladder, analog switches, and input data latches. Binary-weighted currents are switched between DAC output and AGND, thus maintaining a constant current in each ladder leg independent of the switch state. Most applications require only the addition of an external operational amplifier and voltage reference. A simplified D/A circuit for DACA with all digital inputs low is shown in Figure 1.

Figure 2 shows the DACA equivalent circuit. A similar equivalent circuit can be drawn for DACB. Both DACs share the analog ground pin 1 (AGND). With all digital inputs high, the entire reference current flows to OUTA. A small leakage current (I_{lkg}) flows across internal junctions, and as with most semiconductor devices, doubles every 10°C. C_O is due to the parallel combination of the NMOS switches and has a value that depends on the number of switches connected to the output. The range of C_O is 50 pF to 120 pF maximum. The equivalent output resistance r_O varies with the input code from 0.8R to 3R where R is the nominal value of the ladder resistor in the R-2R network.

Interfacing the TLC7528 to a microprocessor is accomplished via the data bus, $\overline{CS}$, $\overline{WR}$, and $\overline{DACA}$/DACB control signals. When $\overline{CS}$ and $\overline{WR}$ are both low, the TLC7528 analog output, specified by the $\overline{DACA}$/DACB control line, responds to the activity on the DB0-DB7 data bus inputs. In this mode, the input latches are transparent and input data directly affects the analog output. When either the $\overline{CS}$ signal or $\overline{WR}$ signal goes high, the data on the DB0-DB7 inputs is latched until the $\overline{CS}$ and $\overline{WR}$ signals go low again. When $\overline{CS}$ is high, the data inputs are disabled regardless of the state of the $\overline{WR}$ signal.

The digital inputs of the TLC7528 provide TTL compatibility when operated from a supply voltage of 5 V. The TLC7528 may be operated with any supply voltage in the range from 5 V to 15 V, however, input logic levels are not TTL compatible above 5 V.

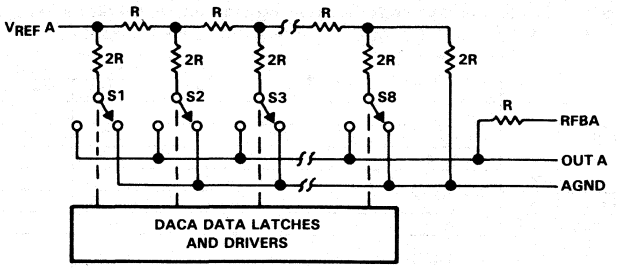


FIGURE 1. SIMPLIFIED FUNCTIONAL CIRCUIT FOR DACA

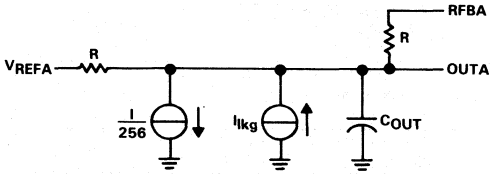


FIGURE 2. TLC7528 EQUIVALENT CIRCUIT, DACA LATCH LOADED WITH 11111111.

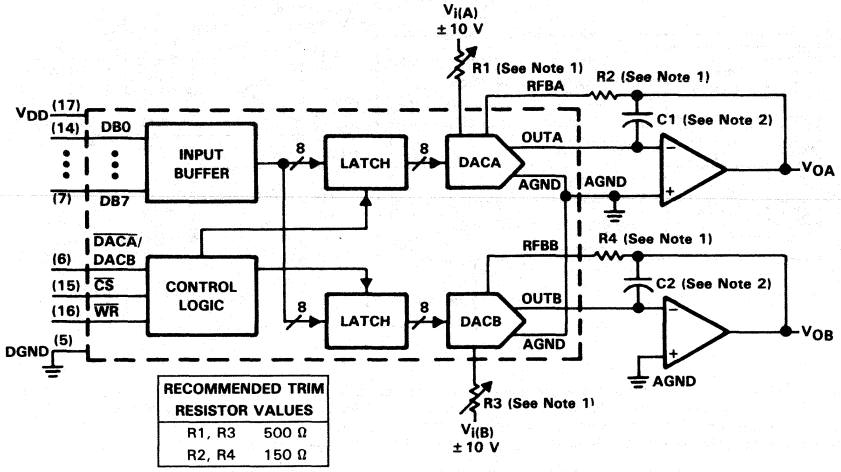
MODE SELECTION TABLE

$\overline{DACA}$/DACB	$\overline{CS}$	$\overline{WR}$	DACA	DACB
L	L	L	WRITE	HOLD
H	L	L	HOLD	WRITE
X	H	X	HOLD	HOLD
X	X	H	HOLD	HOLD

L = low level, H = high level, X = don't care

TYPICAL APPLICATION DATA

The TLC7528 is capable of performing 2-quadrant or full 4-quadrant multiplication. Circuit configurations for 2-quadrant and 4-quadrant multiplication are shown in Figures 3 and 4. Input coding for unipolar and bipolar operation are summarized in Tables 1 and 2, respectively.

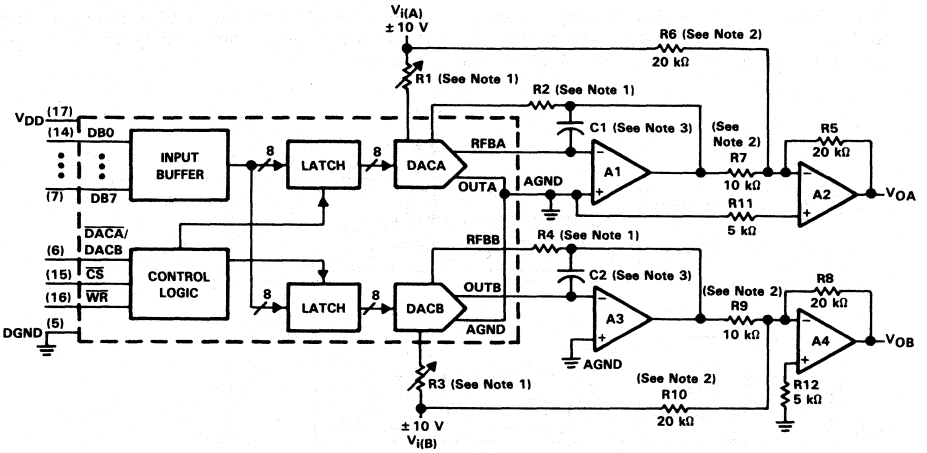


RECOMMENDED TRIM RESISTOR VALUES	
R1, R3	500 Ω
R2, R4	150 Ω

NOTES: 1. R1, R2, R3, and R4 are used only if gain adjustment is required. See table for recommended values. Make gain adjustment with digital input of 255.
2. C1 and C2 phase compensation capacitors (10 pF to 15 pF) are required when using high-speed amplifiers to prevent ringing or oscillation.

FIGURE 3. UNIPOLAR OPERATION (2-QUADRANT MULTIPLICATION)

TYPICAL APPLICATION DATA



NOTES: 1. R1, R2, R3, and R4 are used only if gain adjustment is required. See table in Figure 5 for recommended values. Adjust R1 for V_{OA} = 0 V with code 10000000 in DACA latch. Adjust R3 for V_{OB} = 0 V with 10000000 in DACB latch.
2. Matching and tracking are essential for resistor pairs R6, R7, R9, and R10.
3. C1 and C2 phase compensation capacitors (10 pF to 15 pF) may be required if A1 and A3 are high-speed amplifiers.

FIGURE 4. BIPOLAR OPERATION (4-QUADRANT OPERATION)

TABLE 1. UNIPOLAR BINARY CODE

DAC LATCH CONTENTS MSB LSB†	ANALOG OUTPUT
11111111	$-V_i$ (255/256)
10000001	$-V_i$ (129/256)
10000000	$-V_i$ (128/256) = $-V_i/2$
01111111	$-V_i$ (127/256)
00000001	$-V_i$ (1/256)
00000000	$-V_i$ (0/256) = 0

† 1 LSB = $(2^{-8})V_i$

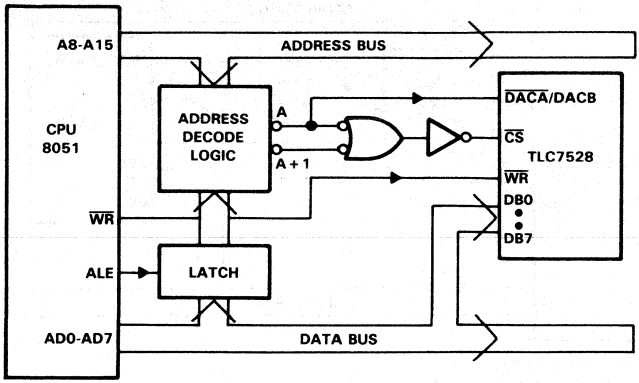
TABLE 2. BIPOLAR (OFFSET BINARY) CODE

DAC LATCH CONTENTS MSB LSB‡	ANALOG OUTPUT
11111111	V_i (127/128)
10000001	V_i (1/128)
10000000	0 V
01111111	$-V_i$ (1/128)
00000001	$-V_i$ (127/128)
00000000	$-V_i$ (128/128)

‡ 1 LSB = $(2^{-7})V_i$

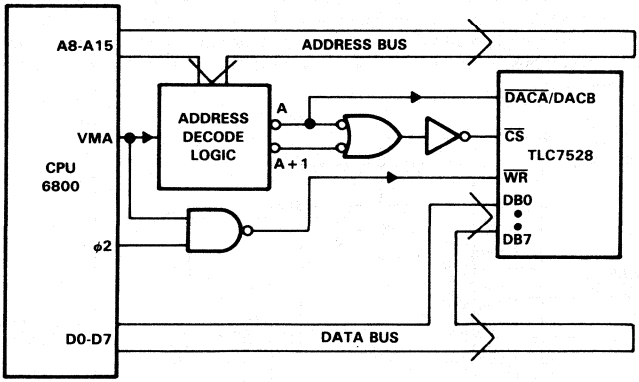
TYPICAL APPLICATION DATA

microprocessor interface information



NOTE: A = decoded address for TLC7528 DACA.
A+1 = decoded address for TLC7528 DACB.

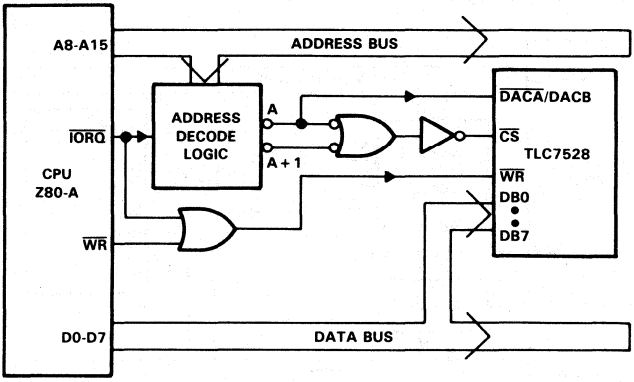
FIGURE 5. TLC7528 — INTEL 8051 INTERFACE



NOTE: A = decoded address for TLC7528 DACA.
A+1 = decoded address for TLC7528 DACB.

FIGURE 6. TLC7528 — 6800 INTERFACE

TYPICAL APPLICATION DATA



NOTE: A = decoded address for TLC7528 DACA.
A + 1 = decoded address for TLC7528 DACB.

FIGURE 7. TLC7528 TO Z80-A INTERFACE

programmable window detector

The programmable window comparator shown in Figure 8 will determine if voltage applied to the DAC feedback resistors are within the limits programmed into the TLC7528 data latches. Input signal range depends on the reference and polarity, that is, the test input range is 0 to $-V_{ref}$. The DACA and DACB data latches are programmed with the upper and lower test limits. A signal within the programmed limits will drive the output high.

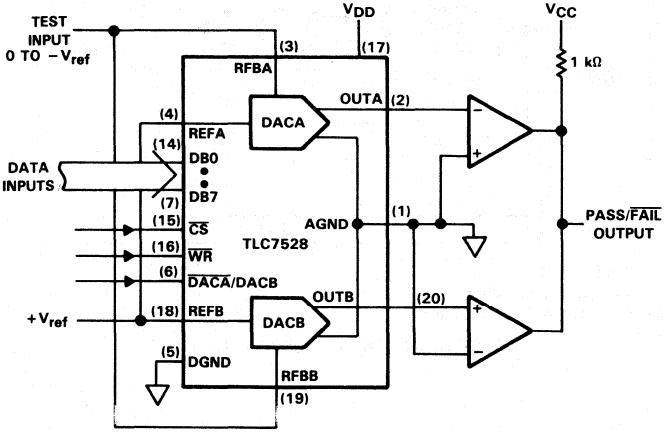


FIGURE 8. DIGITALLY PROGRAMMABLE WINDOW COMPARATOR (UPPER- AND LOWER-LIMIT TESTER)

TYPICAL APPLICATION DATA

digitally controlled signal attenuator

Figure 9 shows the TLC7528 configured as a two-channel programmable attenuator. Applications include stereo audio and telephone signal level control. Table 3 shows input codes vs attenuation for a 0 to 15.5 dB range.

Attentuation db = $-20 \log_{10} D/256$, D = digital input code

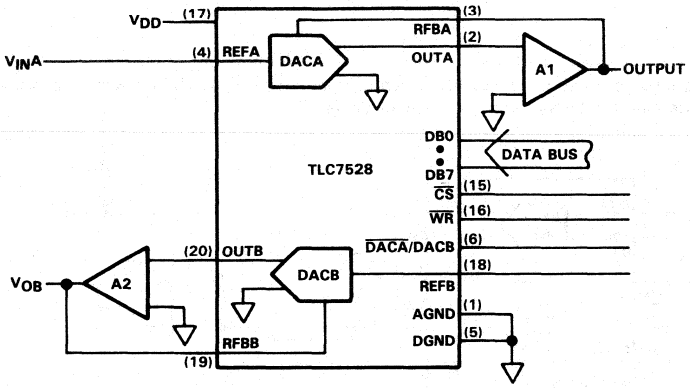


FIGURE 9. DIGITALLY CONTROLLED DUAL TELEPHONE ATTENUATOR

TABLE 3. ATTENUATION vs DACA, DACB CODE

ATTN(dB)	DAC INPUT CODE	CODE IN DECIMAL	ATTN(dB)	DAC INPUT CODE	CODE IN DECIMAL
0	11111111	255	8.0	01100110	102
0.5	11110010	242	8.5	01100000	96
1.0	11100100	228	9.0	01011011	91
1.5	11010111	215	9.5	01010110	86
2.0	11001011	203	10.0	01010001	81
2.5	11000000	192	10.5	01001100	76
3.0	10110101	181	11.0	01001000	72
3.5	10101011	171	11.5	01000100	68
4.0	10100010	162	12.0	01000000	64
4.5	10011000	152	12.5	00111101	61
5.0	10010000	144	13.0	00111001	57
5.5	10001000	136	13.5	00110110	54
6.0	10000000	128	14.0	00110011	51
6.5	01111001	121	14.5	00110000	48
7.0	01110010	114	15.0	00101110	46
7.5	01101100	108	15.5	00101011	43

TYPICAL APPLICATION DATA

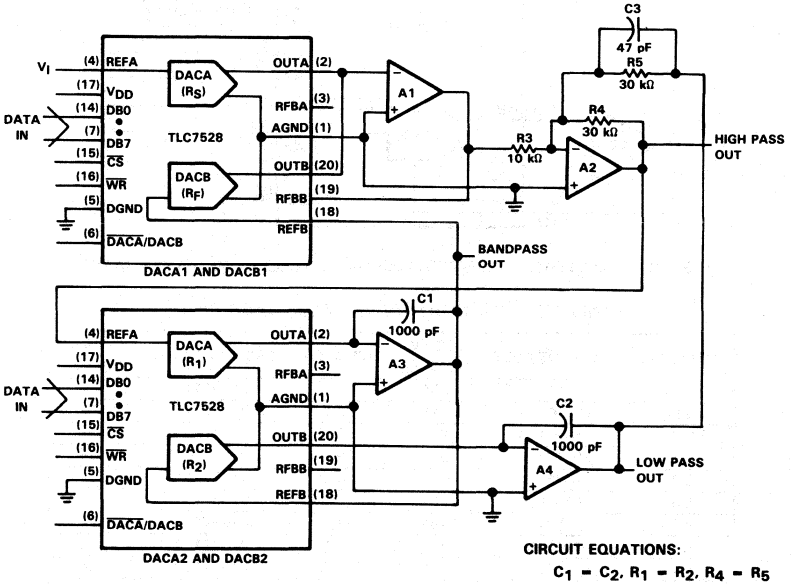
programmable state-variable filter

This programmable state-variable or universal filter configuration provides low-pass, high-pass, and band-pass outputs, and is suitable for applications in which microprocessor control of filter parameters is required.

As shown in Figure 10, DACA1 and DACB1 control the gain and Q of the filter while DACA2 and DACB2 control the cutoff frequency. Both halves of the DACA2 and DACB2 must track accurately in order for the cutoff-frequency equation to be true. With the TLC7528, this is easily achieved.

$$f_C = \frac{1}{2\pi\ R1\ C1}$$

The programmable range for the cutoff or center frequency is 0 to 15 kHz with a Q ranging from 0.3 to 4.5. This defines the limits of the component values.



CIRCUIT EQUATIONS:

$C_1 = C_2,\ R_1 = R_2,\ R_4 = R_5$

$$Q = \frac{R_3}{R_4} \cdot \frac{R_F}{R_{fb(DACB1)}}$$

$$A_o = -\frac{R_F}{R_S}$$

NOTES: A. Op-amps A1, A2, A3, and A4 are TL287.

B. C3 compensates for the op-amp gain-bandwidth limitations.

C. DAC equivalent resistance equals $\frac{256 \times \text{(DAC ladder resistance)}}{\text{DAC digital code}}$

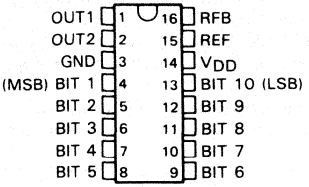
FIGURE 10. DIGITALLY CONTROLLED STATE-VARIABLE FILTER

TLC7533I, TLC7533C
Advanced LinCMOS™ 10-BIT MULTIPLYING DIGITAL-TO-ANALOG CONVERTERS

D2166, OCTOBER 1986

- **ADVANCED LinCMOS™ Silicon-Gate Technology**
- **Guaranteed Monotonicity**
- **Fast Settling Time**
- **CMOS/TTL Compatible**
- **Four-Quadrant Multiplication**
- **Designed to be Interchangeable with Analog Devices AD7533, AD7520, and PMI PM-7533**

N DUAL-IN-LINE PACKAGE
(TOP VIEW)



KEY PERFORMANCE SPECIFICATIONS	
Resolution	10 Bits
Linearity Error	1/2 LSB
Power Dissipation	30 mW
Settling Time	150 ns

description

The TLC7533 is an ADVANCED LinCMOS™ 10-bit digital-to-analog converter featuring two- and four-quadrant multiplication.

The TLC7533 is pin and functionally equivalent to the AD7520 and AD7533. Texas Instruments advanced thin-film-on-monolithic-CMOS fabrication process provides 10-bit linearity without laser trimming.

The TLC7533 features TTL or CMOS compatibility with low input leakage currents from 5-V to 15-V power supplies. Output scaling is provided by an internal feedback resistor and an external operational amplifier. Both positive and negative reference voltages can be utilized.

The TLC7533I is characterized for operation from −25°C to 85°C. The TLC7533C is characterized for operation from 0°C to 70°C.

ADVANCED LinCMOS is a trademark of Texas Instruments Incorporated

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{DD} (see Note 1) . . . . . −0.3 V to 16.5 V
Digital input voltage, V_I . . . . . −0.3 to V_{DD} +0.3 V
Reference voltage, V_{ref} . . . . . ±25 V
Operating free-air temperature range: TLC7533I . . . . . −25°C to 85°C
TLC7533C . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds . . . . . 260°C

NOTE 1: All voltage values are with respect to the network ground terminal.

recommended operating conditions

		MIN	NOM	MAX	UNIT
Supply voltage, V_{DD}		5		16.5	V
Reference voltage, V_{ref}			±10		V
High-level input voltage, V_{IH}		2.4			V
Low-level input voltage, V_{IL}				0.8	V
Operating free-air temperature, T_A	TLC7533I	−25		85	°C
	TLC7533C	0		70	

electrical characteristics over recommended operating temperature range, V_{DD} = 15 V, V_{ref} = ±10 V, OUT1 and OUT2 at 0 V (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	MAX	UNIT
I_I	Input leakage current, digital input		V_I = 0 or V_{DD}		±1	μA
r_I	Input resistance (pin 15) (see Note 2)			5	20	kΩ
I_{lkg}	Output leakage current	OUT1	Digital inputs at V_{IL}		±200	nA
		OUT2	Digital inputs at V_{IH}		±200	
k_{svs}	Supply voltage sensitivity ($\Delta A_V/\Delta V_{DD}$) (see Note 3)		V_{DD} = 14 V to 16.5 V, Digital inputs at V_{IH}		0.008	%/%
I_{DD}	Supply current				2	mA
C_i	Input capacitance, digital input		V_I = V_{IL}		10	pF
C_o	Output capacitance	OUT1	Digital inputs at V_{IH}		100	pF
		OUT2			35	
		OUT1	Digital inputs at V_{IL}		35	
		OUT2			100	

NOTES: 2. Temperature coefficient is approximately −300 ppm/°C.
3. A_V is the ratio of the DAC's external operational amplifier output voltage to the REF input voltage when using the internal feedback resistor.

operating characteristics over recommended operating free-air temperature range, V_{DD} = 15 V, V_{ref} = 10 V, OUT1 and OUT2 at 0 V (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	MAX	UNIT
Relative accuracy	See Note 4		±0.05	%FSR
Gain error	Digital inputs at V_{IH}, See Notes 4 and 5		±1.5	%FS
Output current settling time	To ±0.05% FSR, R_L = 100 Ω, Digital inputs changing from V_{IH} to V_{IL}, or V_{IL} to V_{IH}		150	ns
Feedthrough error	Digital inputs at V_{IL}, V_{ref} = ±10 V sine wave at 100 kHz		±0.1	%FSR

NOTES: 4. Practical Full Scale Range (FSR) = V_{ref} − 1 LSB.
5. Gain error is measured using the internal feedback resistor. Full-Scale (FS) = $-V_{ref}$ (1023/1024). Maximum gain change from T_A = 25°C to minimum or maximum temperature is 0.1% FSR.

PRINCIPLES OF OPERATION

The TLC7533 is a 10-bit multiplying D/A converter consisting of an inverted R-2R ladder and analog switches. Binary-weighted currents are switched between the OUT1 and OUT2 bus lines by NMOS current switches. The on-state resistances of these switches are binarily scaled so that the voltage drop across every switch is the same. The OUT1 and OUT2 bus lines should be maintained at the same potential so that the current in each ladder leg remains constant and is independent of the switch state. Most applications require only the addition of an external operational amplifier and a voltage reference.

The equivalent circuit for all digital inputs low is shown in Figure 1. With all of the digital inputs low, the entire reference current, I_{ref}, is switched to OUT2 as shown in Figure 2. The current source $I_{ref}/1024$ represents the constant current flowing through the termination resistor of the R-2R ladder; while the current source I_{lkg} represents leakage currents to the substrate. The output capacitances, $C_{o(1)}$ and $C_{o(2)}$, are due to the capacitance of the NMOS current switches and vary with the switch state. With all digital inputs low, all of the current switches and the entire resistor ladder are switched to the OUT2 bus line. The capacitance appearing at OUT2 is a maximum of 100 pF; at OUT1 there is a maximum of 35 pF. With all digital inputs high, all of the current switches are switched to OUT1, and 100 pF maximum appears at OUT1. A maximum of 35 pF appears at OUT2 as shown in Figure 3.

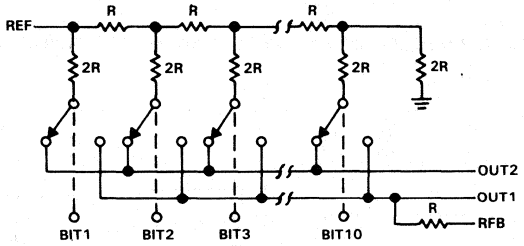


FIGURE 1. SIMPLIFIED DAC CIRCUIT – ALL DIGITAL INPUTS LOW

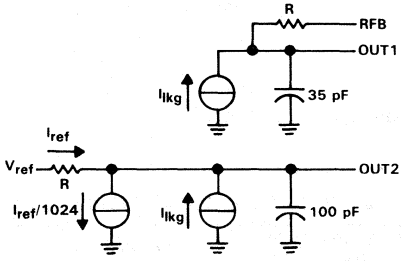


FIGURE 2. DAC EQUIVALENT CIRCUIT – ALL DIGITAL INPUTS LOW

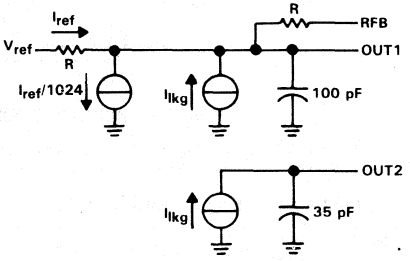


FIGURE 3. DAC EQUIVALENT CIRCUIT – ALL DIGITAL INPUTS HIGH

TYPICAL APPLICATION DATA

The TLC7533 is capable of performing 2-quadrant or full 4-quadrant multiplication. Circuit configurations for 2-quadrant or 4-quadrant multiplication are shown in Figures 4 and 5. Input coding for unipolar and bipolar operation are summarized in Tables 1 and 2, respectively.

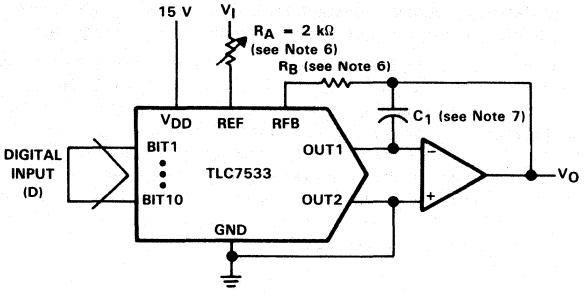


FIGURE 4. UNIPOLAR OPERATION (2-QUADRANT MULTIPLICATION)

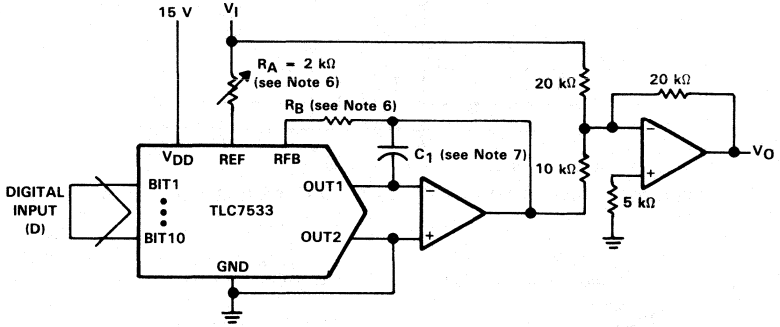


FIGURE 5. BIPOLAR OPERATION (4-QUADRANT OPERATION)

NOTES: 6. R_A and R_B are used only if gain adjustment is required.
7. C_1 (10-33 pF) may be required for phase compensation when using high-speed op-amps.

TABLE 1. UNIPOLAR BINARY CODE

DAC DIGITAL INPUT MSB LSB†	ANALOG OUTPUT
1111111111	$-V_I$ (1023/1024)
1000000001	$-V_I$ (513/1024)
1000000000	$-V_I$ (512/1024) = $-V_{ref}/2$
0111111111	$-V_I$ (511/1024)
0000000001	$-V_I$ (1/1024)
0000000000	$-V_I$ (0/1024) = 0

† 1 LSB = $(2^{-10})\ V_I$

TABLE 2. BIPOLAR (OFFSET BINARY) CODE

DAC DIGITAL INPUT MSB LSB‡	ANALOG OUTPUT
1111111111	$+V_I$ (511/512)
1000000001	$+V_I$ (1/512)
1000000000	0
0111111111	$-V_I$ (1/512)
0000000001	$-V_I$ (511/512)
0000000000	$-V_I$ (512/512) = $-V_I$

‡ 1 LSB = $(2^{-9})\ V_I$

TYPICAL APPLICATION DATA

The TLC7533 may be used in voltage output operation as shown in Figure 6. In this configuration, the input voltage is applied to the OUT1 terminal and the output voltage is taken from the REF terminal. The output voltage varies with the digital input code according to the equation shown. The output should be buffered to prevent loading errors due to the high output resistance of this circuit (typically 10 kilohms). The input voltage should not exceed 1.5 volts to ensure nonlinearity errors less than 1 LSB.

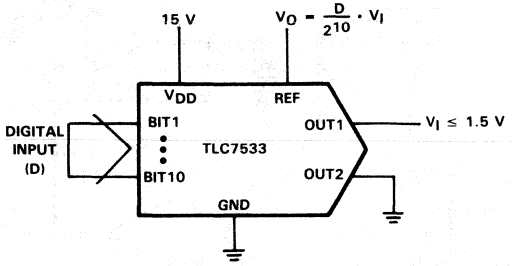
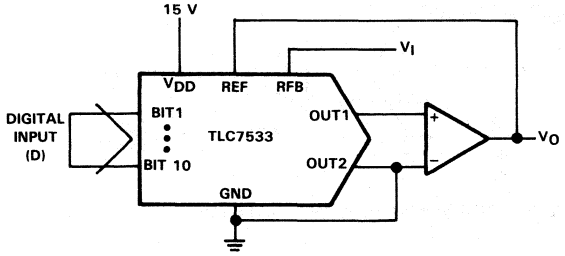


FIGURE 6. VOLTAGE OUTPUT OPERATION

By connecting the DAC in the feedback of an op-amp as shown in Figure 7, the circuit behaves as a programmable gain amplifier with the transfer function:

$$V_O = -V_I \left(\frac{1024}{D}\right)$$

where D = Digital Input Code (expressed as a decimal number)



GAIN TABLE	
D	V_O/V_I
1023	−1.00097
512	−2
256	−4
128	−8
2	−512
1	−1024
0	open loop

FIGURE 7. PROGRAMMABLE GAIN AMPLIFIER

TYPICAL APPLICATION DATA

The programmable function generator shown in Figure 8 produces both square and triangular wave output at a frequency determined by the digital input code. The digital input of the digitally programmable limit detector shown in Figure 9 determines the trip point of the PASS/FAIL output. For a digital input of 00000 00000, the threshold is 0 V, for 11111 11111, the threshold is $-V_{ref}$.

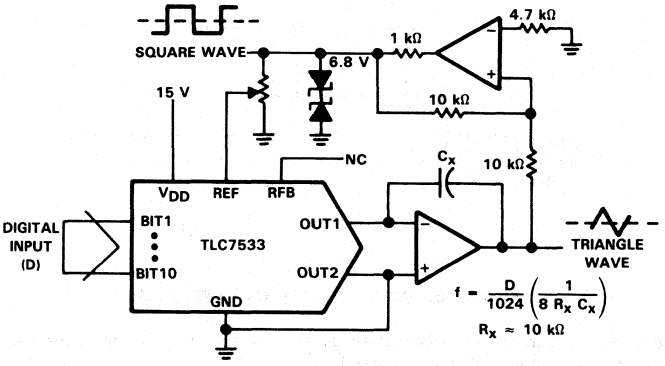


FIGURE 8. PROGRAMMABLE FUNCTION GENERATOR

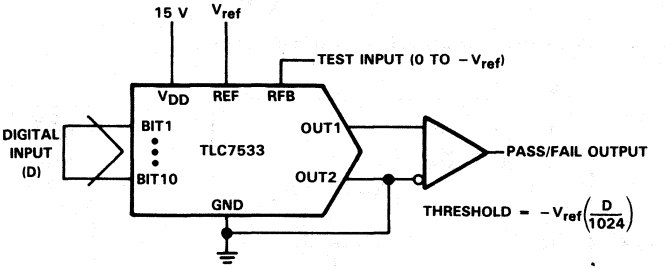


FIGURE 9. PROGRAMMABLE LIMIT DETECTOR

TYPICAL APPLICATION DATA

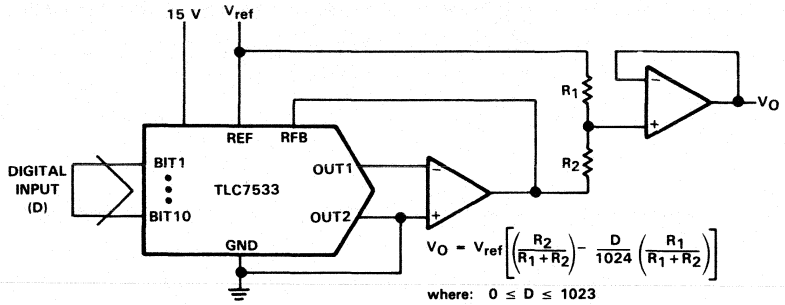


FIGURE 10. MODIFIED SCALE-FACTOR AND OFFSET

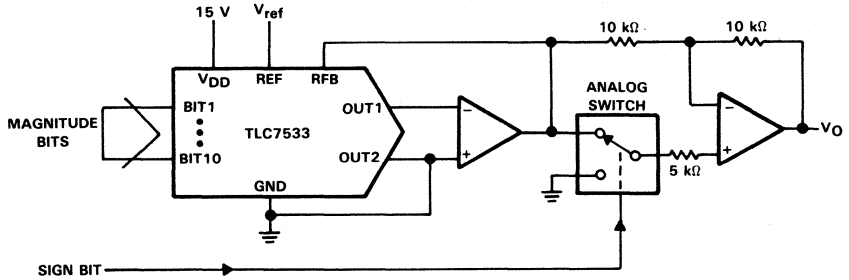


FIGURE 11. 10-BIT AND SIGN MULTIPLYING DAC

General Information 1

Operational Amplifiers 2

Voltage Comparators 3

Timers 4

Analog to Digital Converters 5

Digital to Analog Converters 6

Analog Switches 7

Switched Capacitor Filters 8

Packaging Information 9

ANALOG SWITCHES

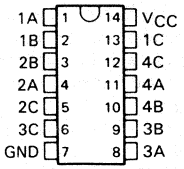
	ON-STATE RESISTANCE @ 4.5V (OHMS)	SWITCH LEAKAGE CURRENTS @ 5.5V OFF STATE (nA)	ON STATE (nA)	PROPAGATION DELAY @ 2.0V (nS)	SUPPLY VOLTAGE RANGE (V) Min	Max	SUPPLY CURRENT @ 5.5V (μA)	PAGE No.
Quad								
TLC4016	200	+/–600	+/–150	62	2	12	20	7-5
TLC4066	200	+/–600	+/–150	30	2	12	20	7-13

TLC4016M, TLC4016I
SILICON-GATE CMOS QUADRUPLE BILATERAL ANALOG SWITCH

D2922, JANUARY 1986

- **High Degree of Linearity**
- **High On-Off Output Voltage Ratio**
- **Low Crosstalk Between Switches**
- **Low On-State Impedance of 50 Ohms Typ at V_{CC} = 9 V**
- **Individual Switch Controls**
- **Extremely Low Input Current**

TLC4016M . . . J OR N PACKAGE
TLC4016I . . . D OR N PACKAGE
(TOP VIEW)



description

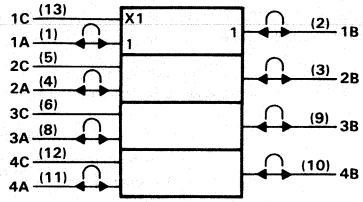
The TLC4016 is a silicon-gate CMOS quadruple analog switch integrated circuit designed to handle both analog and digital signals. Each switch permits signals with amplitudes up to 12 volts peak to be transmitted in either direction.

Each switch section has its own enable input control. A high-level voltage applied to this control terminal turns on the associated switch section.

Applications include signal gating, chopping, modulation or demodulation (modem), and signal multiplexing for analog-to-digital and digital-to-analog conversion systems.

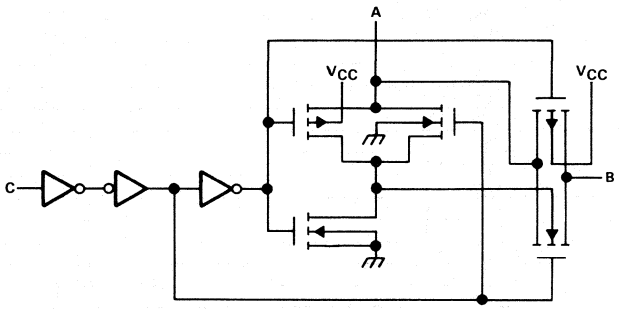
The TLC4016M is characterized for operation from −55°C to 125°C, and the TLC4016I is characterized from −40°C to 85°C.

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage range (see Note 1) . . . . . −0.5 V to 15 V
Control-input diode current ($V_I < 0$ or $V_I > V_{CC}$) . . . . . ±20 mA
I/O port diode current ($V_I < 0$ or $V_{I/O} > V_{CC}$) . . . . . ±20 mA
On-state switch current ($V_{I/O} = 0$ to V_{CC}) . . . . . ±25 mA
Continuous current through V_{CC} or GND pins . . . . . ±50 mA
Continuous total dissipation at (or below) 25°C free-air temperature (see Note 2):
D package . . . . . 950 mW
J package . . . . . 1025 mW
N package . . . . . 875 mW
Operating free-air temperature, T_A: TLC4016M . . . . . −55°C to 125°C
TLC4016I . . . . . −40°C to 85°C
Storage temperature range . . . . . −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: D and N packages . . . . . 260°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds: J package . . . . . 300°C

NOTES: 1. All voltages are with respect to ground unless otherwise specified.
2. For operation above 25°C free-air temperature, see Dissipation Derating Table.

DISSIPATION DERATING TABLE

Package	Maximum Power Dissipation			Derating Factor
	25°C	85°C	125°C	
D	950 mW	494 mW		7.6 mW/°C
J	1025 mW	533 mW	205 mW	8.2 mW/°C
N	875 mW	455 mW	175 mW	7.0 mW/°C

recommended operating conditions

		MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}		2†	5	12	V
I/O port voltage, $V_{I/O}$		0		V_{CC}	V
High-level input voltage, V_{IH}	V_{CC} = 2 V	1.5		V_{CC}	V
	V_{CC} = 4.5 V	3.15		V_{CC}	
	V_{CC} = 9 V	6.3		V_{CC}	
	V_{CC} = 12 V	8.4		V_{CC}	
Low-level input voltage, V_{IL}	V_{CC} = 2 V	0		0.3	V
	V_{CC} = 4.5 V	0		0.9	
	V_{CC} = 9 V	0		1.8	
	V_{CC} = 12 V	0		2.4	
Input rise time, t_r	V_{CC} = 2 V			1000	ns
	V_{CC} = 4.5 V			500	
	V_{CC} = 9 V			400	
Input fall time, t_f	V_{CC} = 2 V			1000	ns
	V_{CC} = 4.5 V			500	
	V_{CC} = 9 V			400	
Operating free-air temperature, T_A	TLC4066M	−55		125	°C
	TLC4066I	−40		85	

†With supply voltages at or near 2 volts, the analog switch on-state resistance becomes very nonlinear. It is recommended that only digital signals be transmitted at these low supply voltages.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted).

PARAMETER			TEST CONDITIONS	V_{CC}	TLC4016M			TLC4016I			UNIT
					MIN	TYP†	MAX	MIN	TYP†	MAX	
r_{Son}	On-state switch resistance		I_S = 1 mA, V_A = 0 to V_{CC}, See Figure 1	4.5 V		100	220		100	200	Ω
				9 V		50	120		50	105	
				12 V		30	100		30	85	
			I_S = 1 mA, V_A = 0 or V_{CC}, See Figure 1	2 V		120	240		120	215	
				4.5 V		50	120		50	100	
				9 V		35	80		35	75	
				12 V		20	70		20	60	
	On-state switch resistance matching		V_A = 0 to V_{CC}, See Figure 1	4.5 V		10	20		10	20	Ω
				9 V		5	15		5	15	
				12 V		5	15		5	15	
I_I	Control input current		V_I = 0 or V_{CC}	2 V to 6 V			±1			±1	μA
			V_I = 0 or V_{CC}, T_A = 25°C				±0.1			±0.1	
I_{Soff}	Off-state switch leakage current		V_S = ±V_{CC}, See Figure 2	5.5 V		±10	±600		±10	±600	nA
				9 V		±15	±800		±15	±800	
				12 V		±20	±1000		±20	±1000	
I_{Son}	On-state switch leakage current		V_A = 0 or V_{CC}, See Figure 3	5.5 V		±10	±150		±10	±150	nA
				9 V		±15	±200		±15	±200	
				12 V		±20	±300		±20	±300	
I_{CC}	Supply current		V_I = 0 or V_{CC}, I_O = 0	5.5 V		2	40		2	20	μA
				9 V		8	160		8	80	
				12 V		16	320		16	160	
C_i	Input capacitance	A or B		2 V to 12 V		15			15		pF
		C				5	10		5	10	
C_f	Feedthrough capacitance	A to B	V_I = 0	2 V to 12 V		5			5		pF

†All typical values are at T_A = 25°C.

switching characteristics over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	TLC4016M			TLC4016I			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{pd}	Propagation delay time, A to B or B to A	See Figure 4	2 V		25	75		25	62	ns
			4.5 V		5	15		5	13	
			9 V		4	14		4	12	
			12 V		3	13		3	11	
t_{on}	Switch turn-on time	R_L = 1 kΩ, See Figures 5 and 6	2 V		32	150		32	125	ns
			4.5 V		8	30		8	25	
			9 V		6	18		6	15	
			12 V		5	15		5	13	
t_{off}	Switch turn-off time	R_L = 1 kΩ, See Figures 5 and 6	2 V		45	252		45	210	ns
			4.5 V		15	54		15	45	
			9 V		10	48		10	40	
			12 V		8	45		8	38	
f_{co}	Switch cutoff frequency (channel loss = 3 dB)		4.5 V		100			100		MHz
			9 V		120			120		
$V_{OCF(PP)}$	Control feedthrough voltage to any switch, peak to peak	See Figure 7	4.5 V			180			180	mV
	Frequency at which crosstalk attenuation between any two switches equals 50 dB	See Figure 8	4.5 V		1			1		MHz

†All typical values are at T_A = 25°C.

PARAMETER MEASUREMENT INFORMATION

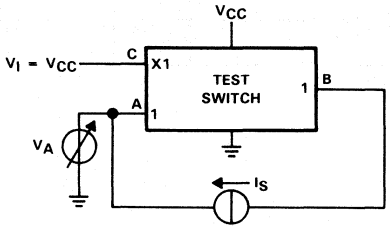
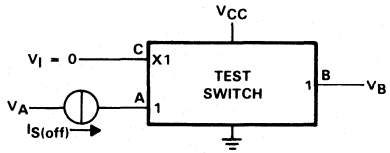


FIGURE 1. ON-STATE RESISTANCE TEST CIRCUIT



$V_S = V_A - V_B$
CONDITION 1: V_A = 0, $V_B = V_{CC}$
CONDITION 2: $V_A = V_{CC}$, V_B = 0

FIGURE 2. OFF-STATE SWITCH LEAKAGE CURRENT TEST CIRCUIT

PARAMETER MEASUREMENT INFORMATION

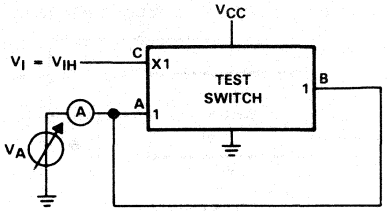
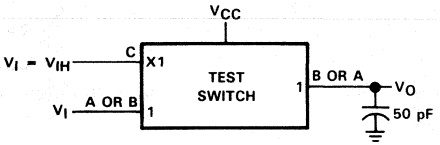
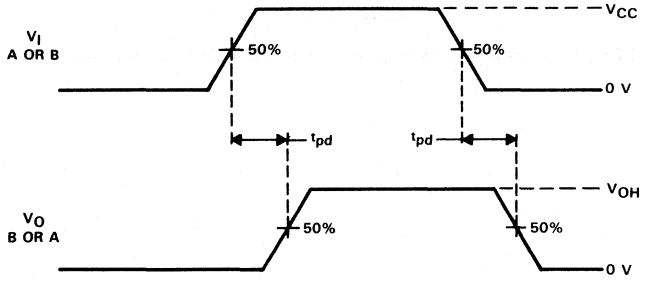


FIGURE 3. ON-STATE SWITCH LEAKAGE CURRENT TEST CIRCUIT



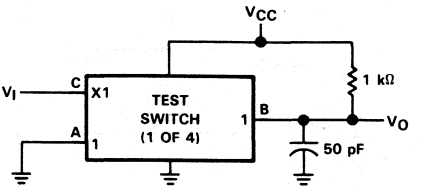
TEST CIRCUIT



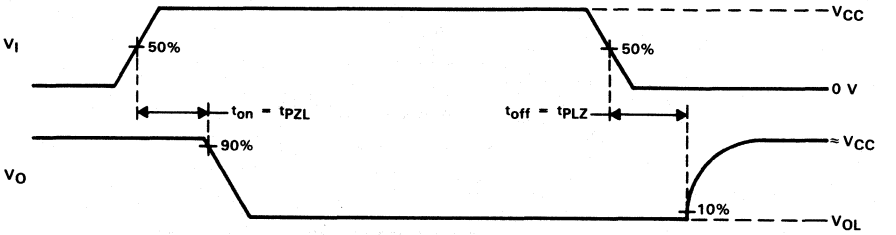
VOLTAGE WAVEFORMS

FIGURE 4. PROPAGATION DELAY TIME, SIGNAL INPUT TO SIGNAL OUTPUT

PARAMETER MEASUREMENT INFORMATION



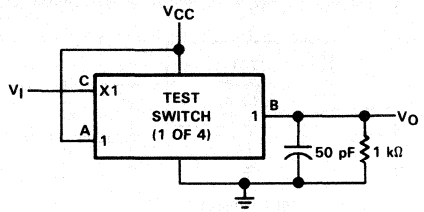
TEST CIRCUIT



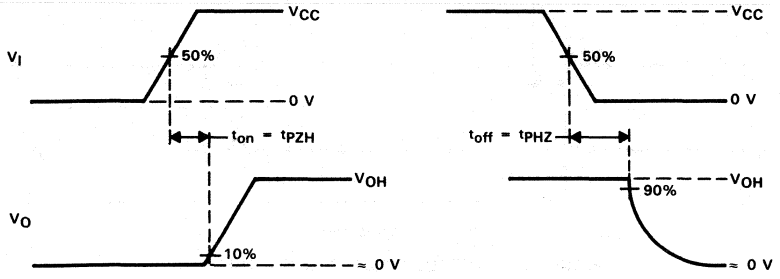
VOLTAGE WAVEFORMS

FIGURE 5. SWITCHING TIME (t_{PZL}, t_{PLZ}), CONTROL TO SIGNAL OUTPUT

PARAMETER MEASUREMENT INFORMATION



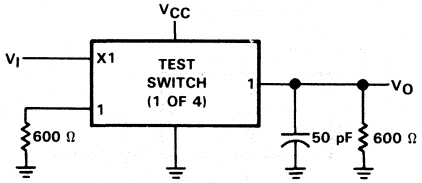
TEST CIRCUIT



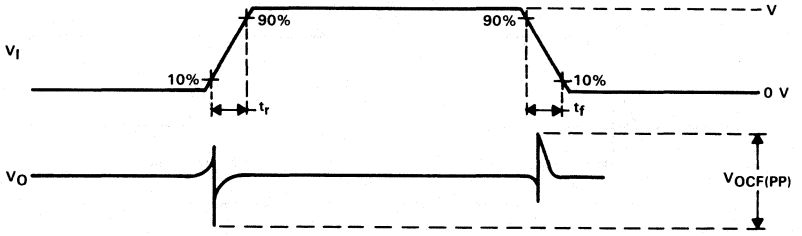
VOLTAGE WAVEFORMS

FIGURE 6. SWITCHING TIME (t_{PZH}, t_{PHZ}), CONTROL TO SIGNAL OUTPUT

PARAMETER MEASUREMENT INFORMATION

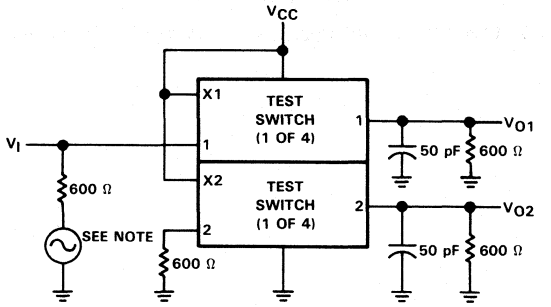


TEST CIRCUIT



VOLTAGE WAVEFORMS

FIGURE 7. CONTROL FEEDTHROUGH VOLTAGE



NOTE: ADJUST f for $a_X = \frac{V_{O2}}{V_{O1}} = 50$ dB.

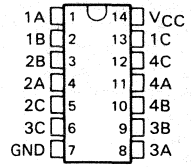
FIGURE 8. CROSSTALK BETWEEN ANY TWO SWITCHES, TEST CIRCUIT

TLC4066M, TLC4066I
SILICON-GATE CMOS QUADRUPLE BILATERAL ANALOG SWITCH

D2922, JANUARY 1986

- **High Degree of Linearity**
- **High On-Off Output Voltage Ratio**
- **Low Crosstalk Between Switches**
- **Low On-State Impedance . . .Typically 30 Ohms at V_{CC} = 12 V**
- **Individual Switch Controls**
- **Extremely Low Input Current**
- **Functionally Interchangeable with National Semiconductor MM54/74HC4066, Motorola MC54/74HC4066, and RCA CD4066A**

TLC4066M . . . J OR N PACKAGE
TLC4066I . . . D OR N PACKAGE
(TOP VIEW)



description

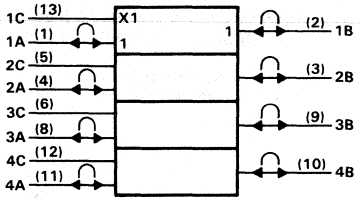
The TLC4066 is a silicon-gate CMOS quadruple analog switch integrated circuit designed to handle both analog and digital signals. Each switch permits signals with amplitudes up to 12 volts peak to be transmitted in either direction.

Each switch section has its own enable input control. A high-level voltage applied to this control terminal turns on the associated switch section.

Applications include signal gating, chopping, modulation or demodulation (modem), and signal multiplexing for analog-to-digital and digital-to-analog conversion systems.

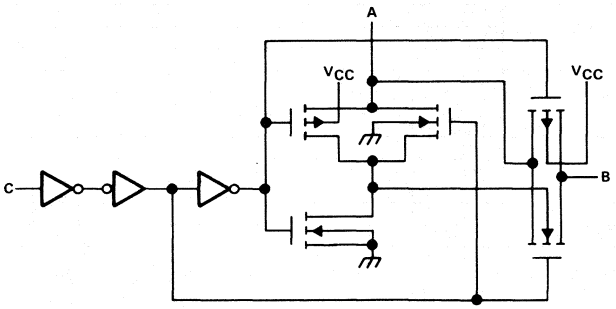
The TLC4066M is characterized for operation from −55°C to 125°C. The TLC4066I is characterized from −40°C to 85°C.

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage range (see Note 1) . . . . . −0.5 V to 15 V
Control-input diode current ($V_I < 0$ or $V_I > V_{CC}$) . . . . . ±20 mA
I/O port diode current ($V_I < 0$ or $V_{I/O} > V_{CC}$) . . . . . ±20 mA
On-state switch current ($V_{I/O}$ = 0 to V_{CC}) . . . . . ±25 mA
Continuous current through V_{CC} or GND pins . . . . . ±50 mA
Continuous total dissipation at (or below) 25°C free-air temperature (see Note 2):
D package . . . . . 950 mW
J package . . . . . 1025 mW
N package . . . . . 875 mW
Operating free-air temperature, T_A: TLC4066M . . . . . −55°C to 125°C
TLC4066I . . . . . −40°C to 85°C
Storage temperature range . . . . . −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: D and N packages . . . . . 260°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds: J package . . . . . 300°C

NOTES: 1. All voltages are with respect to ground unless otherwise specified.
2. For operation above 25°C free-air temperature, see Dissipation Derating Table.

DISSIPATION DERATING TABLE

Package	Maximum Power Dissipation			Derating Factor
	25°C	85°C	125°C	
D	950 mW	494 mW		7.6 mW/°C
J	1025 mW	533 mW	205 mW	8.2 mW/°C
N	875 mW	455 mW	175 mW	7.0 mW/°C

recommended operating conditions

		MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}		2†	5	12	V
I/O port voltage, $V_{I/O}$		0		V_{CC}	V
High-level input voltage, V_{IH}	V_{CC} = 2 V	1.5		V_{CC}	V
	V_{CC} = 4.5 V	3.15		V_{CC}	
	V_{CC} = 9 V	6.3		V_{CC}	
	V_{CC} = 12 V	8.4		V_{CC}	
Low-level input voltage, V_{IL}	V_{CC} = 2 V	0		0.3	V
	V_{CC} = 4.5 V	0		0.9	
	V_{CC} = 9 V	0		1.8	
	V_{CC} = 12 V	0		2.4	
Input rise time, t_r	V_{CC} = 2 V			1000	ns
	V_{CC} = 4.5 V			500	
	V_{CC} = 9 V			400	
Input fall time, t_f	V_{CC} = 2 V			1000	ns
	V_{CC} = 4.5 V			500	
	V_{CC} = 9 V			400	
Operating free-air temperature, T_A	TLC4066M	−55		125	°C
	TLC4066I	−40		85	

†With supply voltages at or near 2 volts, the analog switch on-state resistance becomes very nonlinear. It is recommended that only digital signals be transmitted at these low supply voltages.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS	V_{CC}	TLC4066M			TLC4066I			UNIT
					MIN	TYP†	MAX	MIN	TYP†	MAX	
r_{Son}	On-state switch resistance		I_S = 1 mA, V_A = 0 to V_{CC}, See Figure 1	4.5 V		100	220		100	200	Ω
				9 V		50	110		50	105	
				12 V		30	90		30	85	
			I_S = 1 mA, V_A = 0 or V_{CC}, See Figure 1	2 V		120	240		120	215	
				4.5 V		50	120		50	100	
				9 V		35	80		35	75	
				12 V		20	70		20	60	
	On-state switch resistance matching		V_A = 0 to V_{CC}, See Figure 1	4.5 V		10	20		10	20	Ω
				9 V		5	15		5	15	
				12 V		5	15		5	15	
I_I	Control input current		V_I = 0 or V_{CC}	2 V or 6 V			±1			±1	μA
I_{Soff}	Off-state switch leakage current		V_S = ±V_{CC}, See Figure 2	5.5 V		±10	±600		±10	±600	nA
				9 V		±15	±800		±15	±800	
				12 V		±20	±1000		±20	±1000	
I_{Son}	On-state switch leakage current		V_A = 0 or V_{CC}, See Figure 3	5.5 V		±10	±150		±10	±150	nA
				9 V		±15	±200		±15	±200	
				12 V		±20	±300		±20	±300	
I_{CC}	Supply current		V_I = 0 or V_{CC}, I_O = 0	5.5 V		2	40		2	20	μA
				9 V		8	160		8	80	
				12 V		16	320		16	160	
C_i	Input capacitance	A or B		2 V to 12 V		15			15		pF
		C				5	10		5	10	
C_f	Feedthrough capacitance	A to B	V_I = 0	2 V to 12 V		5			5		pF

†All typical values are at T_A = 25°C.

switching characteristics over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	TLC4066M			TLC4066I			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{pd}	Propagation delay time, A to B or B to A	See Figure 4	2 V		25	75		15	30	ns
			4.5 V		5	15		5	13	
			9 V		4	12		4	10	
			12 V		3	13		3	11	
t_{on}	Switch turn-on time	R_L = 1 kΩ, See Figures 5 and 6	2 V		32	150		32	125	ns
			4.5 V		8	30		8	25	
			9 V		6	18		6	15	
			12 V		5	15		5	13	
t_{off}	Switch turn-off time	R_L = 1 kΩ, See Figures 5 and 6	2 V		45	252		45	210	ns
			4.5 V		15	54		15	45	
			9 V		10	48		10	40	
			12 V		8	45		8	38	
f_{co}	Switch cutoff frequency (channel loss = 3 dB)		4.5 V		100			100		MHz
			9 V		120			120		
$V_{OCF(PP)}$	Control feedthrough voltage to any switch, peak to peak	See Figure 7	4.5 V			180			180	mV
	Frequency at which crosstalk attenuation between any two switches equals 50 dB	See Figure 8	4.5 V		1			1		MHz

†All typical values are at T_A = 25°C.

PARAMETER MEASUREMENT INFORMATION

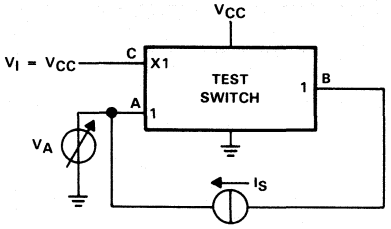
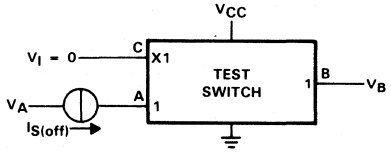


FIGURE 1. ON-STATE RESISTANCE TEST CIRCUIT



$V_S = V_A - V_B$
CONDITION 1: V_A = 0, $V_B = V_{CC}$
CONDITION 2: $V_A = V_{CC}$, V_B = 0

FIGURE 2. OFF-STATE SWITCH LEAKAGE CURRENT TEST CIRCUIT

PARAMETER MEASUREMENT INFORMATION

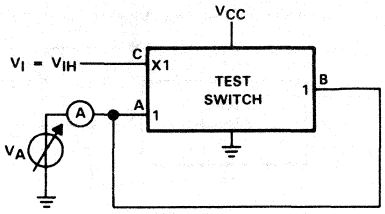
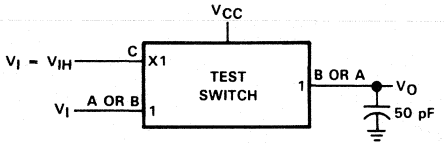
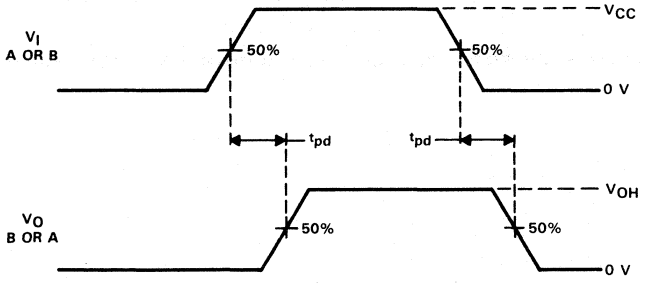


FIGURE 3. ON-STATE SWITCH LEAKAGE CURRENT TEST CIRCUIT



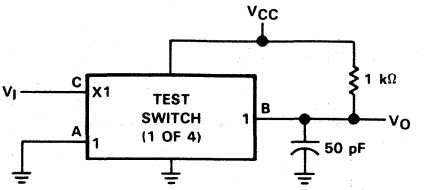
TEST CIRCUIT



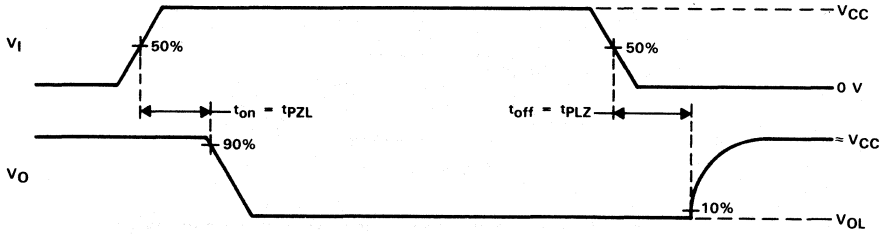
VOLTAGE WAVEFORMS

FIGURE 4. PROPAGATION DELAY TIME, SIGNAL INPUT TO SIGNAL OUTPUT

PARAMETER MEASUREMENT INFORMATION



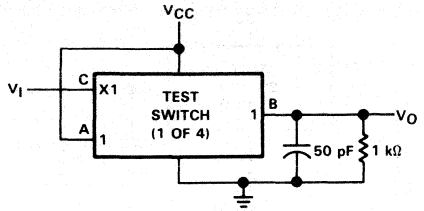
TEST CIRCUIT



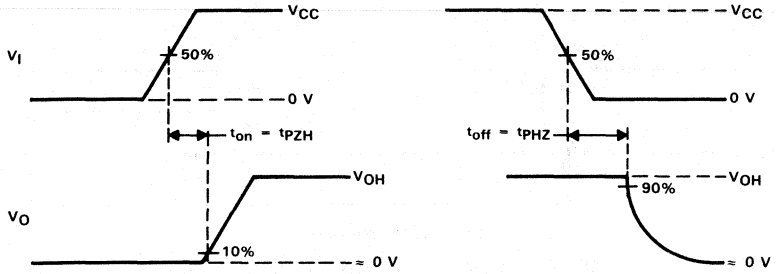
VOLTAGE WAVEFORMS

FIGURE 5. SWITCHING TIME (t_{PZL}, t_{PLZ}), CONTROL TO SIGNAL OUTPUT

PARAMETER MEASUREMENT INFORMATION



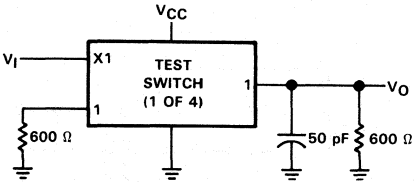
TEST CIRCUIT



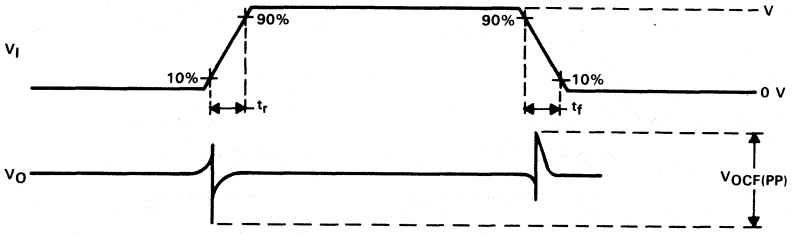
VOLTAGE WAVEFORMS

FIGURE 6. SWITCHING TIME (t_{PZH}, t_{PHZ}), CONTROL TO SIGNAL OUTPUT

PARAMETER MEASUREMENT INFORMATION

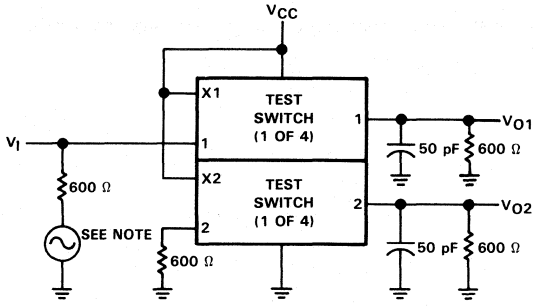


TEST CIRCUIT



VOLTAGE WAVEFORMS

FIGURE 7. CONTROL FEEDTHROUGH VOLTAGE



NOTE: ADJUST f for $a_X = \frac{V_{O2}}{V_{O1}} = 50$ dB.

FIGURE 8. CROSSTALK BETWEEN ANY TWO SWITCHES, TEST CIRCUIT

General Information 1

Operational Amplifiers 2

Voltage Comparators 3

Timers 4

Analog to Digital Converters 5

Digital to Analog Converters 6

Analog Switches 7

Switched Capacitor Filters 8

Packaging Information 9

SWITCHED CAPACITOR FILTERS

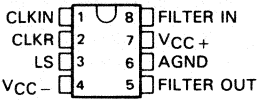
	FILTER FREQUENCY RANGE (KHZ)	MAX CLOCK FREQUENCY (MHZ)	CROSSTALK ATTENU-ATION (dB)	CLOCK TO CENTRE FREQUENCY ERROR	MAX FILTER Q DEVIATION FROM 20	POWER SUPPLY (V) (mA)		MAX SUPPLY CURRENT (mA)	PAGE No.
						Min	Max		
TLC10	30	1.5	60	0.6%	4%	± 4	± 6	10	8-15
TLC20	30	1.5	60	1.5%	6%	± 4	± 6	10	8-15
TLC04	20	1.0	—	± 0.8%	—	± 2.5	± 6	2.25	8-15
TLC14	10	1.0	—	± 1.0%	—	± 2.5	± 6	2.25	8-15

TLC04, TLC14
BUTTERWORTH FOURTH-ORDER LOW-PASS SWITCHED-CAPACITOR FILTERS

D2970, NOVEMBER, 1986

- **Low Clock-to-Cutoff-Frequency Ratio Error**
  TLC04 . . . ±0.8%
  TLC14 . . . ±1%
- **Filter Cutoff Frequency Dependent Only on External-Clock Frequency Stability**
- **Minimum Filter Response Deviation Due to External Component Variations Over Time and Temperature**
- **Cutoff Frequency Range from 0.1 Hz to 20 kHz**
- **5-V to 12-V Operation**
- **Self Clocking or TTL-Compatible and CMOS-Compatible Clock Inputs**
- **Designed to be Interchangeable with National MF4-50 and MF4-100**

D OR N PACKAGE
(TOP VIEW)



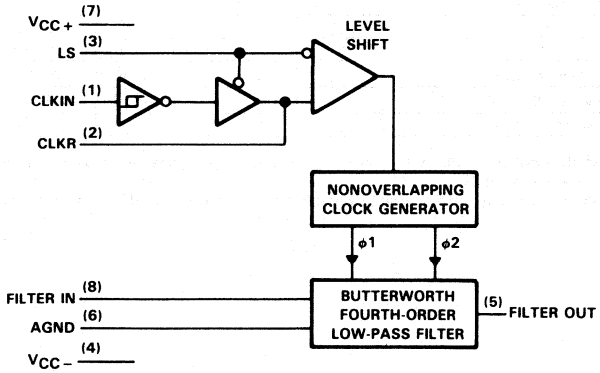
description

The TLC04 and TLC14 are monolithic Butterworth low-pass switched-capacitor filters. Each is designed as a low-cost, easy-to-use device and to provide accurate fourth-order low-pass filter functions in circuit design configurations.

Each filter features cutoff frequency stability that is dependent only on the external-clock frequency stability. The cutoff frequency is clock tunable and has a clock-to-cutoff frequency ratio of 50:1 with less than ±0.8% error for the TLC04 and a clock-to-cutoff frequency ratio of 100:1 with less than ±1% error for the TLC14. The input clock features self-clocking or TTL- or CMOS-compatible options in conjunction with the level shift (LS) pin.

The TLC04 and TLC14 are characterized for operation from 0°C to 70°C.

functional block diagram



pin description

PIN NAME	PIN NO.	I/O	DESCRIPTION
AGND	6	I	Analog Ground — The noninverting input to the operational amplifiers of the Butterworth fourth-order low-pass filter.
CLKIN	1	I	Clock In — The clock input terminal for CMOS-compatible clock or self-clocking options. For either option, the Level Shift (LS) terminal is at V_{CC-}. For self-clocking, a resistor is connected between the CLKIN and CLKR terminal pins and a capacitor is connected from the CLKIN terminal pin to ground.
CLKR	2	I	Clock R — The clock input for a TTL-compatible clock. For a TTL clock, the level shift pin is connected to mid-supply and the CLKIN pin may be left open, but it is recommended that it be connected to either V_{CC+} or V_{CC-}.
FILTER IN	8	I	Filter Input
FILTER OUT	5	O	Butterworth fourth-order low-pass Filter Output
LS	3	I	Level Shift — This terminal accommodates the various input clocking options. For CMOS-compatible clocks or self-clocking, the level-shift terminal is at V_{CC-} and for TTL-compatible clocks, the level-shift terminal is at mid-supply.
V_{CC+}	7	I	Positive supply voltage terminal
V_{CC-}	4	I	Negative supply voltage terminal

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, $V_{CC\pm}$ (see Note 1) . . . . . ±7 V
Operating free-air temperature range . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds . . . . . 260°C

NOTE 1: All voltage values are with respect to the AGND terminal.

recommended operating conditions

		TLC04		TLC14		UNIT
		MIN	MAX	MIN	MAX	
V_{CC+}	Positive supply voltage	2.5	6	2.5	6	V
V_{CC-}	Negative supply voltage	−2.5	−6	−2.5	−6	V
V_{IH}	High-level input voltage	2		2		V
V_{IL}	Low-level input voltage		0.8		0.8	V
f_{clock}	Clock frequency (see Note 2)	5	$1x10^6$	10	$1x10^6$	Hz
f_{co}	Cutoff frequency (see Note 3)	0.1	$20x10^3$	0.1	$10x10^3$	Hz
T_A	Operating free-air temperature	0	70	0	70	°C

NOTES: 2. Above 250 kHz, the input clock duty cycle should be at 50% to allow the operational amplifiers the maximum time to settle while processing analog samples.
3. The cutoff frequency is defined as the frequency where the response is 3.01 dB less than the dc gain of the filter.

electrical characteristics over recommended operating free-air temperature range, V_{CC+} = 2.5 V, V_{CC-} = −2.5 V, f_{clock} ≤ 250 kHz (unless otherwise noted)

filter section

PARAMETER			TEST CONDITIONS	TLC04			TLC14			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{OO}	Output voltage offset				−150			−300		mV
V_{OM}	Peak output voltages	V_{OM+}	R_L = 5 kΩ	2	2.3		2	2.3		V
		V_{OM-}		−1	−1.5		−1	−1.5		
I_{OS}	Short-circuit output current	Source	T_A = 25°C, See Note 4		−0.5			−0.5		mA
		Sink			28			28		
I_{CC}	Supply current		f_{clock} = 250 kHz		1.5	2.25		1.5	2.25	mA

NOTE 4: I_{OS} (source current) is measured by forcing the output to its maximum positive voltage and then shorting the output to the negative supply (V_{CC-}) terminal. I_{OS} (sink current) is measured by forcing the output to its maximum negative voltage and then shorting the output to the positive supply (V_{CC+}) terminal.

operating characteristics over recommended operating free-air temperature range, V_{CC+} = 2.5 V, V_{CC-} = −2.5 V (unless otherwise noted)

PARAMETER	TEST CONDITIONS		TLC04			TLC14			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
Clock-to-cutoff-frequency ratio (f_{clock}/f_{co})	f_{clock} ≤ 250 kHz, T_A = 25°C		49.27	50.07	50.87	99	100	101	
Temperature coefficient of clock-to-cutoff frequency ratio	f_{clock} ≤ 250 kHz		−25	0	25	−25	0	25	ppm/°C
Frequency response above and below cutoff frequency (see Note 5)	f_{co} = 5 kHz, f_{clk} = 250 kHz, T_A = 25°C	f = 6 kHz	−8.11	−7.57	−7.03				dB
		f = 4.5 kHz	−1.7	−1.46	−1.22				
	f_{co} = 2.5 kHz, f_{clk} = 250 kHz, T_A = 25°C	f = 3 kHz				−7.92	−7.42	−6.92	dB
		f = 2.25 kHz				−1.77	−1.51	−1.25	
Dynamic range (see Note 6)	T_A = 25°C			80			78		dB
Stop-band frequency attentuation at 2 f_{co}	f_{clock} ≤ 250 kHz		24	25		24	25		dB
DC voltage amplification	f_{clock} ≤ 250 kHz, RS ≤ 2 kΩ		−0.15	0	0.15	−0.15	0	0.15	dB
Peak-to-peak clock feedthrough voltage	T_A = 25°C			15			15		mV

† All typical values are at T_A = 25°C.

NOTES: 5. The frequency responses at f are referenced to a dc gain of 0 dB.

6. The dynamic range is referenced to 2.82 V rms (4 V peak) where the wideband noise over a 20-kHz bandwidth is typically 282 μV rms for the TLC04 and 355 μV rms for the TLC14.

electrical characteristics over recommended operating free-air temperature range, V_{CC+} = 5 V, V_{CC-} = −5 V, f_{clock} ≤ 250 kHz, (unless otherwise noted)

filter section

PARAMETER			TEST CONDITIONS	TLC04			TLC14			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{OO}	Output voltage offset				−200			−400		mV
V_{OM}	Peak output voltages	V_{OM+}	R_L = 5 kΩ	4	4.5		4	4.5		V
		V_{OM-}		−4	−4.1		−4	−4.1		
I_{OS}	Short-circuit output current	Source	T_A = 25°C,		−1.5			−1.5		mA
		Sink	See Note 4		50			50		
I_{CC}	Supply current		f_{clock} = 250 kHz		2.5	3.5		2.5	3.5	mA

NOTE 4: I_{OS} (source current) is measured by forcing the output to its maximum positive voltage and then shorting the output to the negative supply (V_{CC-}) terminal. I_{OS} (sink current) is measured by forcing the output to its maximum negative voltage and then shorting the output to the positive supply (V_{CC+}) terminal.

clocking section

PARAMETER		TEST CONDITIONS‡		MIN	TYP†	MAX	UNIT
V_{T+} Positive-going input threshold voltage	CLKIN	V_{CC} = 10 V		6.1	7	8.9	V
		V_{CC} = 5 V		3.1	3.5	4.4	
V_{T-} Negative-going input threshold voltage		V_{CC} = 10 V		1.3	3	3.8	V
		V_{CC} = 5 V		0.6	1.5	1.9	
V_{hys} Hysteresis ($V_{T+} - V_{T-}$)		V_{CC} = 10 V		2.3	4	7.6	V
		V_{CC} = 5 V		1.2	2	3.8	
V_{OH} High-level output voltage	CLKR	V_{CC} = 10 V	I_O = −10 μA	9			V
		V_{CC} = 5 V		4.5			
V_{OL} Low-level output voltage		V_{CC} = 10 V	I_O = 10 μA			1	V
		V_{CC} = 5 V				0.5	
Input leakage current		V_{CC} = 10 V	Level Shift pin at mid-supply,			2	μA
		V_{CC} = 5 V	T_A = 25°C			2	
Output current		V_{CC} = 10 V	CLKR shorted to V_{CC-}	−3	−6		mA
		V_{CC} = 5 V		−0.75	−1.5		
Output current		V_{CC} = 10 V	CLKR shorted to V_{CC+}	2.5	5		mA
		V_{CC} = 5 V		0.65	1.3		

† All typical values are at T_A = 25°C.
‡ $V_{CC} = V_{CC+} - V_{CC-}$.

operating characteristics over recommended operating free-air temperature range, V_{CC+} = 5 V, V_{CC-} = −5 V (unless otherwise noted)

PARAMETER	TEST CONDITIONS		TLC04			TLC14			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
Clock-to-cutoff-frequency ratio (f_{clock}/f_{co})	f_{clock} ≤ 250 kHz, T_A = 25°C		49.58	49.98	50.38	99	100	101	
Temperature coefficient of clock-to-cutoff frequency ratio	f_{clock} ≤ 250 kHz		−15	0	15	−15	0	15	ppm/°C
Frequency response above and below cutoff frequency (see Note 5)	f_{co} = 5 kHz, f_{clk} = 250 kHz, T_A = 25°C	f = 6 kHz	−7.84	−7.57	−7.3				dB
		f = 4.5 kHz	−1.56	−1.44	−1.32				
	f_{co} = 2.5 kHz, f_{clk} = 250 kHz, T_A = 25°C	f = 3 kHz				−7.67	−7.42	−7.17	dB
		f = 2.25 kHz				−1.64	−1.51	−1.38	
Dynamic range (see Note 7)	T_A = 25°C			80			78		dB
Stop-band frequency attentuation at 2 f_{co}	f_{clock} ≤ 250 kHz		24	25		24	25		dB
DC voltage amplification	f_{clock} ≤ 250 kHz, RS ≤ 2 kΩ		−0.15	0	0.15	−0.15	0	0.15	dB
Peak-to-peak clock feedthrough voltage	T_A = 25°C			25			25		mV

† All typical values are at T_A = 25°C.

NOTES: 5. The frequency responses at f are referenced to a dc gain of 0 dB.

7. The dynamic range is referenced to 2.82 V rms (4 V peak) where the wideband noise over a 20-kHz bandwidth is typically 282 μV rms for the TLC04 and 355 μV rms for the TLC14.

TYPICAL APPLICATION DATA

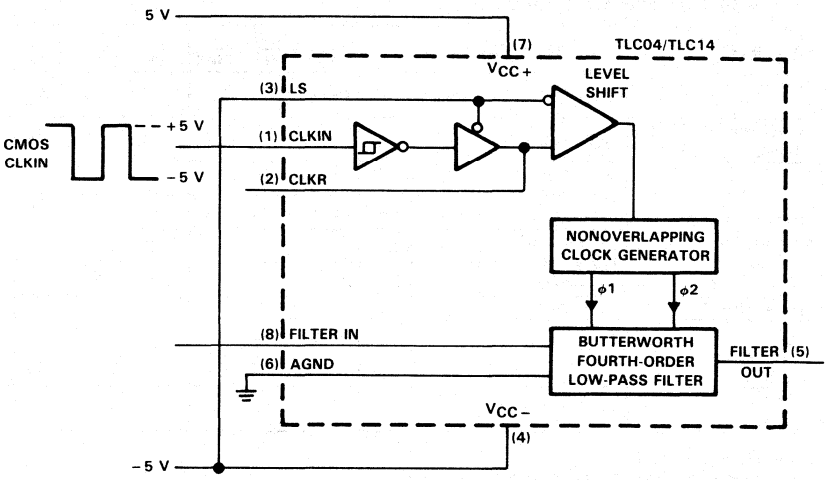


FIGURE 1. CMOS-CLOCK-DRIVEN, DUAL-SUPPLY OPERATION

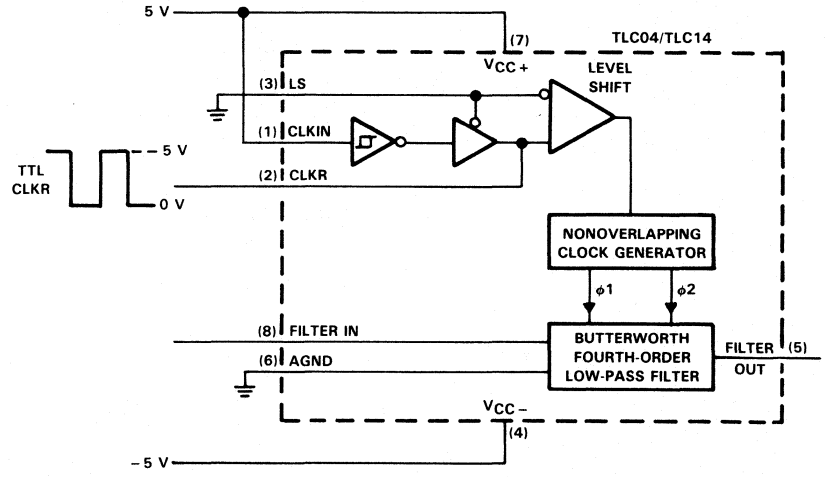
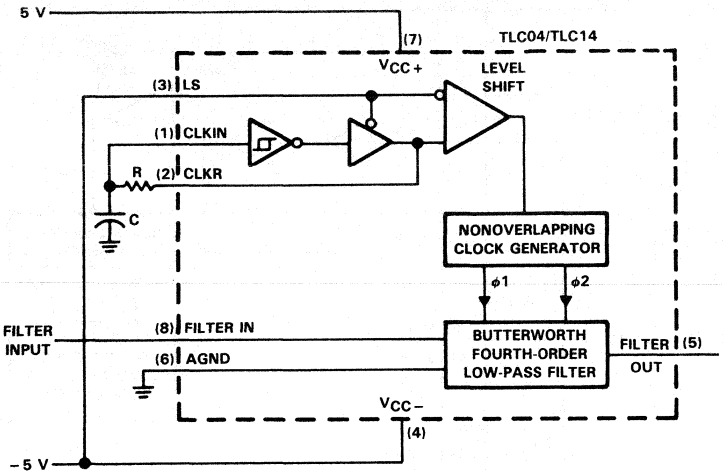


FIGURE 2. TTL-CLOCK-DRIVEN, DUAL-SUPPLY OPERATION

TYPICAL APPLICATION DATA



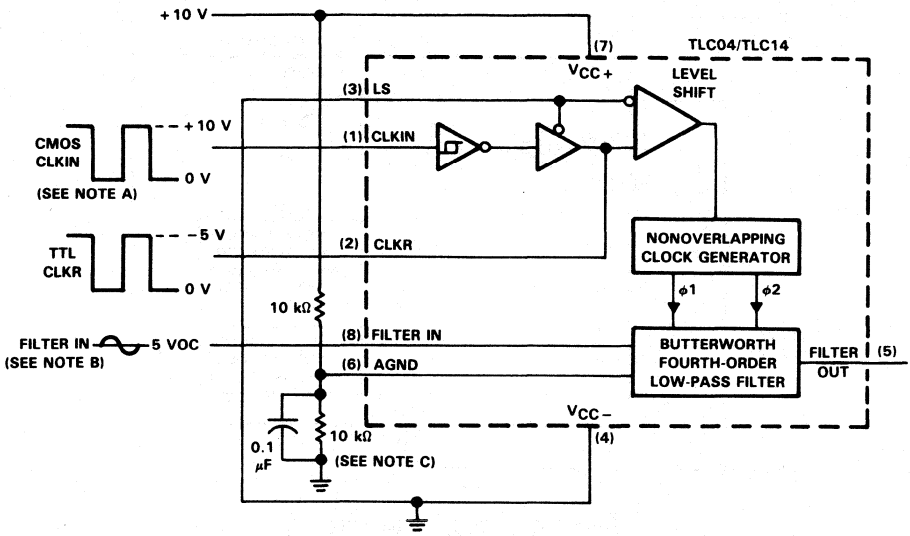
$$f_{clock} = \frac{1}{RC \times \ln\left[\left(\frac{V_{CC} - V_{T-}}{V_{CC} - V_{T+}}\right)\left(\frac{V_{T+}}{V_{T-}}\right)\right]}$$

For V_{CC} = 10 V,

$$f_{clock} = \frac{1}{1.69\ RC}$$

FIGURE 3. SELF-CLOCKING THROUGH SCHMITT TRIGGER OSCILLATOR, DUAL-SUPPLY OPERATION

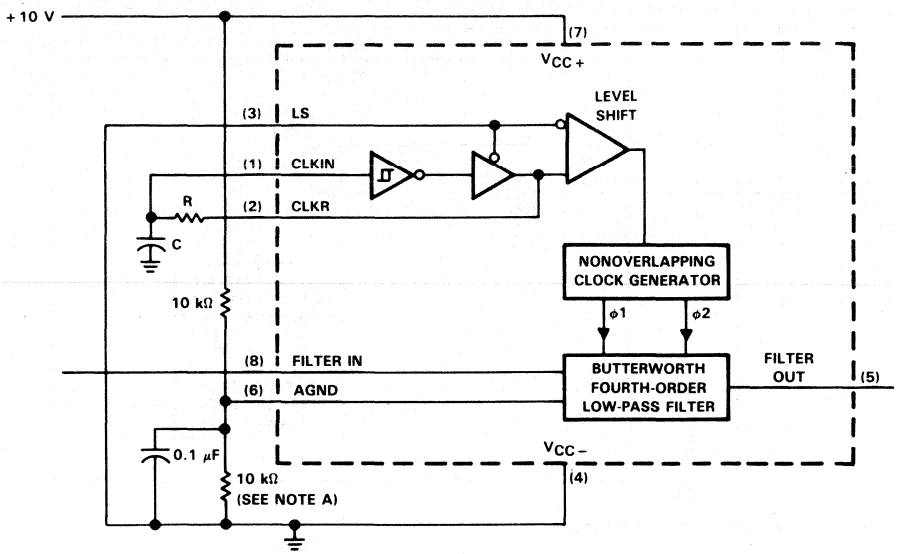
TYPICAL APPLICATION DATA



NOTES: A. The external clock used must be of CMOS level because the clock is input to a CMOS Schmitt trigger.
B. The Filter input signal should be dc-biased to mid-supply or ac-coupled to the terminal.
C. The AGND terminal must be biased to mid-supply.

FIGURE 4. EXTERNAL-CLOCK-DRIVEN SINGLE-SUPPLY OPERATION

TYPICAL APPLICATION DATA



$$f_{clock} = \frac{1}{RC \times \ln\left[\left(\frac{V_{CC} - V_{T-}}{V_{CC} - V_{T+}}\right)\left(\frac{V_{T+}}{V_{T-}}\right)\right]}$$

For $V_{CC} = 10$ V,

$$f_{clock} = \frac{1}{1.69\ RC}$$

NOTE A: The AGND terminal must be biased to mid-supply.

FIGURE 5. SELF-CLOCKING THROUGH SCHMITT TRIGGER OSCILLATOR, SINGLE-SUPPLY OPERATION

TYPICAL APPLICATION DATA

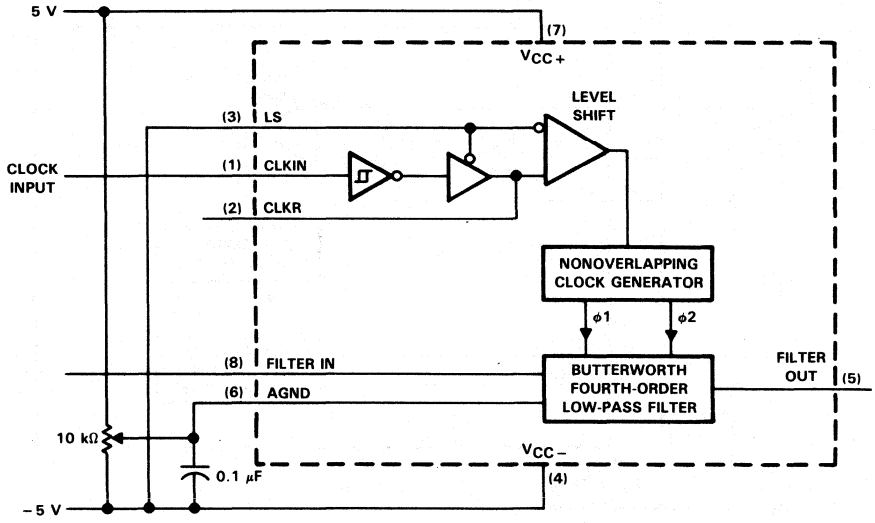


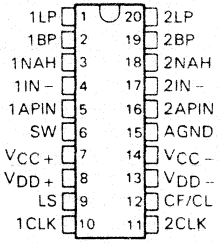
FIGURE 6. DC OFFSET ADJUSTMENT

TLC10, TLC20
UNIVERSAL DUAL SWITCHED-CAPACITOR FILTER

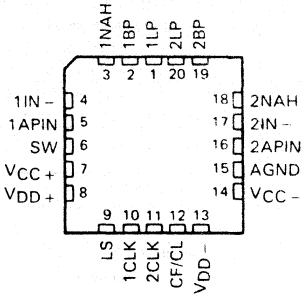
D2952 AUGUST 1986 – REVISED SEPTEMBER 1987

- **Maximum Clock to Center-Frequency Ratio Error**
  - **TLC10 . . . ±0.6%**
  - **TLC20 . . . ±1.5%**
- **Filter Cutoff Frequency Stability Dependent Only on External-Clock Frequency Stability**
- **Minimum Filter Response Deviation Due to External Component Variations over Time and Temperature**
- **Critical-Frequency Times Q Factor Range Up to 200 kHz**
- **Critical-Frequency Operation Up to 30 kHz**
- **Designed to be Interchangeable with:**
  - **National MF10**
  - **Maxim MF10**
  - **Linear Technology LTC1060**

N DUAL-IN-LINE PACKAGE
(TOP VIEW)



FN CHIP CARRIER PACKAGE
(TOP VIEW)



description

The TLC10 and TLC20 are monolithic general-purpose switched-capacitor CMOS filters each containing two independent active-filter sections. Each device facilitates configuration of Butterworth, Bessel, Cauer, or Chebyshev filter design.

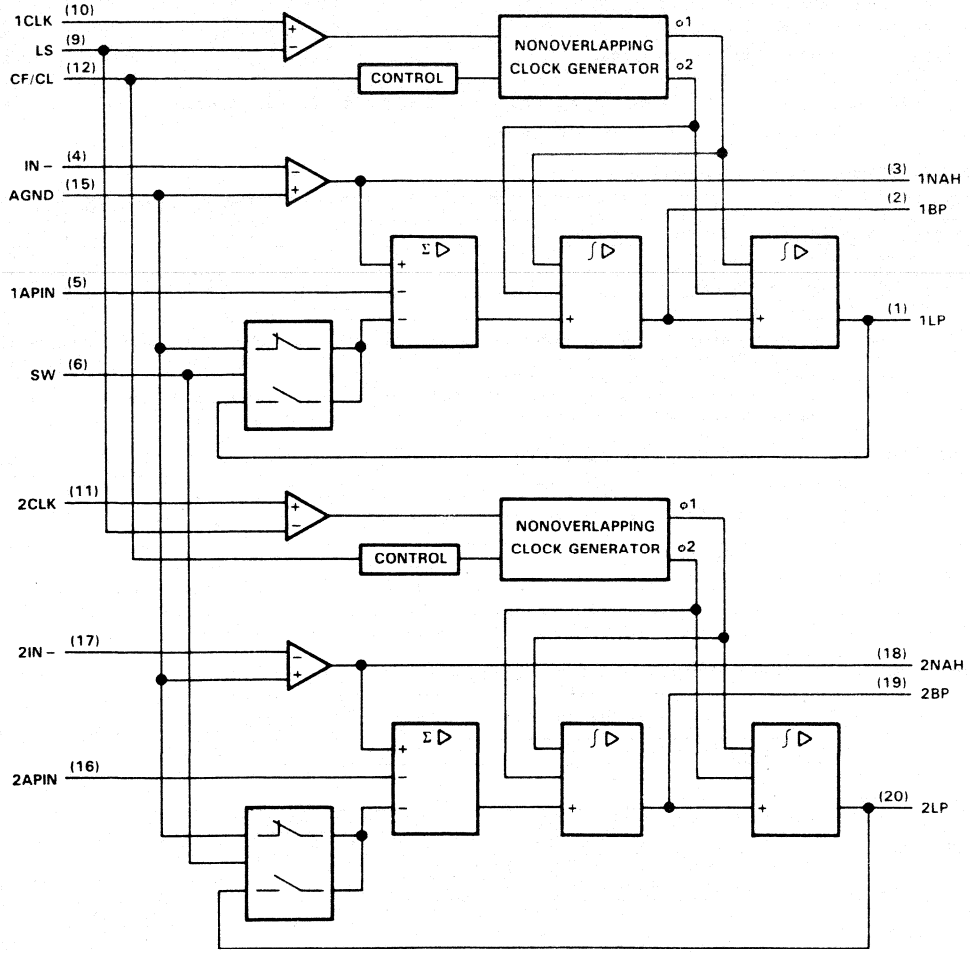
Filter features include cutoff frequency stability that is dependent only on the external clock frequency stability and minimal response deviation over time and temperature. Features also include a critical-frequency times filter quality (Q) factor range of up to 200 kiloHertz.

With external clock and resistors, each filter section can be used independently to produce various second-order functions or both sections can be cascaded to produce fourth-order functions. For functions greater than fourth-order, ICs can be cascaded.

The TLC10 and TLC20 are characterized for operation from 0°C to 70°C.

PIN NAME	PIN NO.	I/O	DESCRIPTION
AGND	15	I	Analog Ground — The noninverting inputs to the input operational amplifiers of both filter sections. This terminal should be at ground for dual supplies or at mid-supply level for single-supply operation.
1APIN 2APIN	5 16	I	All-Pass Inputs — The all-pass input to the summing amplifier of each respective filter section used for all-pass filter applications in configuration modes 1a, 4, 5, and 6. This terminal should be driven from a source having an impedance of less than 1 kilohm. In all other modes, this terminal is grounded. See Typical Application Data.
1BP 2BP	2 19	O	Band-Pass Outputs — The band-pass output of each respective filter section provides the second-order band-pass filter functions.
CF/CL	12	I	Center Frequency/Current Limit — This input terminal provides the option to select the input-clock-to-center-frequency ratio of 50:1 or 100:1 or to limit the current of the IC. For a 50:1 ratio, the CF/CL terminal is set to V_{DD+}. For a 100:1 ratio, the CF/CL terminal is set to ground for dual supplies or to mid-supply level for single-supply operation. For current limiting, the CF/CL terminal is set to V_{DD-}. This aborts filtering and limits the IC current to 0.5 milliamperes.
1CLK 2CLK	10 11	I	Clock Inputs — The clock input to the two-phase nonoverlapping generator of each respective filter section is used to generate the center frequency of the complex pole pair second-order function. Both clocks should be of the same level (TTL or CMOS) and have duty cycles close to 50%, especially when clock frequencies (f_{clock}) greater than 200 kiloHertz are used. At this duty cycle, the operational amplifiers have the maximum time to settle while processing analog samples.
1IN− 2IN−	4 17	I	Inverting Inputs — The inverting input side of the input operational amplifier whose output drives the summing amplifier of each respective filter section.
1LP 2LP	1 20	O	Low-Pass Outputs — The low-pass outputs of the second-order filters.
LS	9	I	Level Shift — This terminal accommodates various input clock levels of bipolar (CMOS) or unipolar (TTL or other clocks) to function with single or dual supplies. For CMOS (±5-volt) clocks, V_{DD-} or ground is applied to the LS terminal. For TTL and other clocks, ground is applied to the LS terminal.
1NAH 2NAH	3	O	Notch, All-Pass, or High-Pass Outputs — The output of each respective filter section can be used to provide either a second-order notch, all-pass, or high-pass output filter function, depending on circuit configuration.
SW	6	I	Switch Input — This input terminal is used to control internal switches to connect either the AGND input or the LP output to one of the inputs of the summing amplifier. The terminal controls both independent filter sections and places them in the same configuration simultaneously. If V_{CC-} is applied to the SW terminal, the AGND input terminal will be connected to one of the inputs of each summing amplifier. If V_{CC+} is applied to the SW terminal, the LP output will be connected to one of the inputs of the summing amplifier.
V_{CC+}	8		Analog positive supply voltage terminal
V_{CC-}	14		Analog negative supply voltage terminal
V_{DD+}	9		Digital positive supply voltage terminal
V_{DD-}	13		Digital negative supply voltage terminal

functional block diagram



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Analog supply voltage, $V_{CC\pm}$ (see Note 1) . . . . . ±7 V
Digital supply voltage, $V_{DD\pm}$ . . . . . ±7 V
Operating free-air temperature range . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: FN or N package . . . . . 260°C

NOTE 1: All voltage values are with respect to the AGND terminal.

recommended operating conditions

	MIN	NOM	MAX	UNIT
Analog supply voltage, $V_{CC\pm}$, (see Note 2)	±4	±5	±6	V
Digital supply voltage, $V_{DD\pm}$, (see Note 2)	±4	±5	±6	V
Clock frequency, f_{clock}, (see Note 3)	0.008		1.0	MHz
Operating free-air temperature, T_A	0		70	°C

NOTES: 2. A common supply voltage source should be used for the analog and digital supply voltages. Although each has separate terminals, they are connected together internally at the substrate. $V_{CC}+$ and $V_{DD}+$ can be connected together at the device terminals or at the supply voltage source. The same is true for $V_{CC}-$ and $V_{DD}-$.
3. Both input clocks should be of the same level type (TTL or CMOS), and their duty cycles should be at 50% above 200 kHz to allow the operational amplifiers the maximum time to settle while processing analog samples.

electrical characteristics at $V_{CC\pm}$ = ±5 V, $V_{DD\pm}$ + = ±5 V, T_A = 25°C (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	MIN	TYP	MAX	UNIT
V_{OPP}	Maximum peak-to-peak output voltage swing		R_L = 3.5 kΩ at all outputs	±4	±4.1		±3.8	±3.9		V
I_{OS}	Short-circuit output current, Pins 3 and 18	Source	See Note 4		2			2		mA
		Sink			50			50		
I_{CC}	Supply current				8	10		8	10	mA

NOTE 4: The short-circuit output current for pins 1, 2, 19, and 20 will be typically the same as pins 3 and 18.

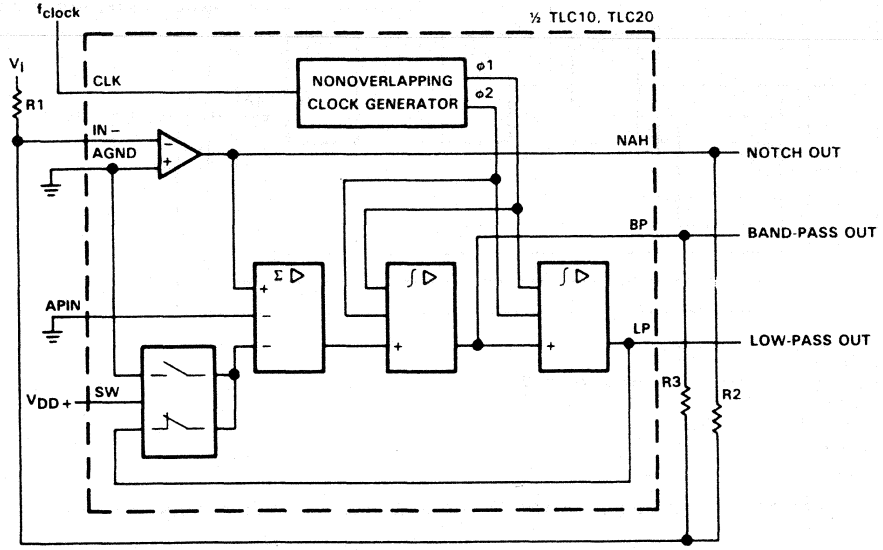
operating characteristics at $V_{CC\pm}$ = ±5 V, $V_{DD\pm}$ = ±5 V, T_A = 25°C (unless otherwise noted)

PARAMETER	TEST CONDITIONS		TLC10			TLC20			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
Critical-frequency range	$f_o \times Q \leq 200$ kHz		20	30		20	30		kHz
Maximum clock frequency, f_{clock}	See Note 3		1.0	1.5		1.0	1.5		MHz
Clock to center-frequency ratio	$f_o \leq 5$ kHz, R3/R2 = 10, Mode 1, See Figure 1	Pin 12 at 5 V	49.64	49.94	50.24	49.24	49.94	50.64	
		Pin 12 at 0 V	98.75	99.35	99.95	97.86	99.35	100.84	
Temperature coefficient of center frequency	$f_o \leq 5$ kHz, R3/R2 = 20, Mode 1, See Figure 1	Pin 12 at 5 V		±10			±10		ppm/°C
		Pin 12 at 0 V		±100			±100		
Filter Q (quality factor) deviation from 20	$f_o \leq 5$ kHz, R3/R2 = 20, Mode 1, See Figure 1	Pin 12 at 5 V		±2%	±4%		±2%	±6%	
		Pin 12 at 0 V		±2%	±3%		±2%	±6%	
Temperature coefficient of measured filter Q	$f_o \leq 5$ kHz, R3/R2 = 20, Mode 1			±500			±500		ppm/°C
Low-pass output deviation from unity gain	R1 = R2 = 10 kΩ, Mode 1, See Figure 1				±2%			±2%	
Crosstalk attenuation				60			60		dB
Clock feedthrough voltage				10			10		mV
Operational amplifier gain-bandwidth product				2.5			2.5		MHz
Operational amplifier slew rate				7			7		V/μs

TYPICAL APPLICATION DATA

modes of operation

The TLC10 and TLC20 are switched-capacitor (sampled-data) filters that closely approximate continuous filters. Each filter section is designed to approximate the response of a second-order variable filter. When the sampling frequency is much larger than the frequency band of interest, the sampled-data filter is a good approximation to its continuous time equivalent. In the case of the TLC10 and TLC20, the ratio is about 50:1 or 100:1. To fully describe their transfer function, a time domain approach would be appropriate. Since this may appear cumbersome, the following application examples are based on the well known frequency domain. It should be noted that in order to obtain the actual filter response, the filter's response must be examined in the z-domain.

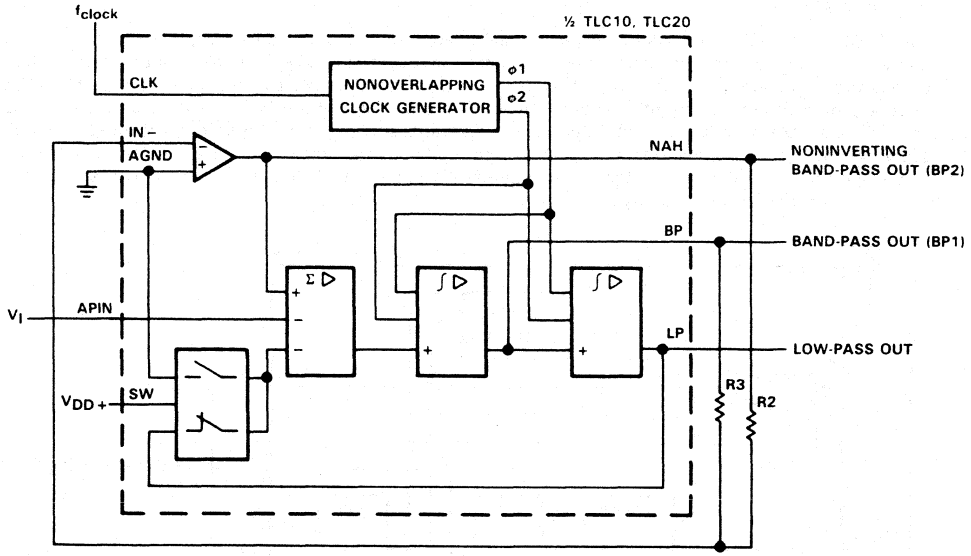


$f_o = f_{clock}/100$ or $f_{clock}/50$
$f_{notch} = f_o$
$H_{OLP} = -R2/R1$ (as $f \rightarrow 0$)
$H_{OBP} = -R3/R1$ (at $f = f_o$)
H_{ON} = notch gain { as f approaches 0 $-R2/R1$; as f approaches 0.5 f_{clock}
$Q = f_o/BW = R3/R2$

Circuit dynamics:
The following expressions determine the swing at each output as a function of the desired Q of the second-order function.
$H_{OLP} = H_{OBP}/Q$ or $H_{OLP} \times Q = H_{ON} \times Q$
H_{OLP} (peak) = $Q \times H_{OLP}$ (for high Qs)

FIGURE 1. MODE 1 FOR NOTCH, BAND-PASS, AND LOW-PASS OUTPUTS: $f_{notch} = f_o$

TYPICAL APPLICATION DATA

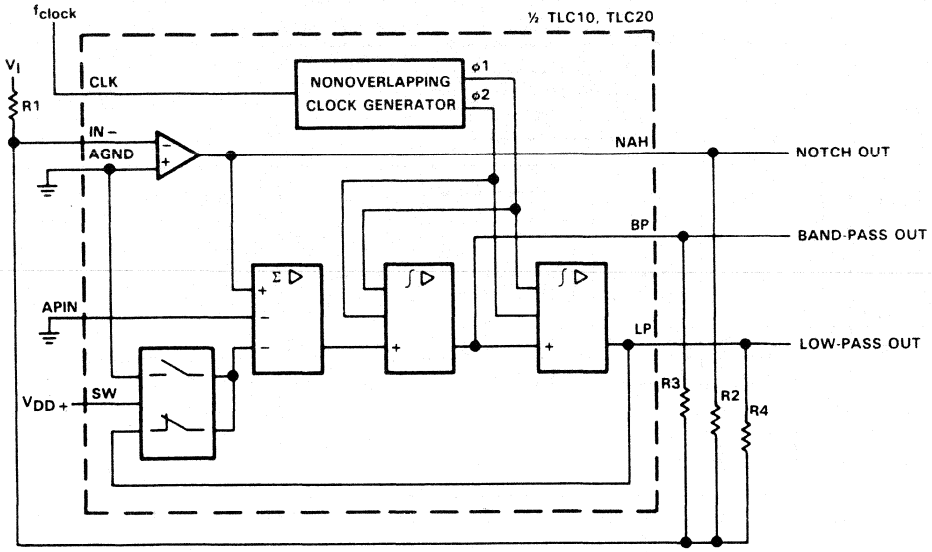


$f_o = f_{clock}/100$ or $f_{clock}/50$
$Q = R3/R2$
$H_{OLP} = -1\,H_{OLP}$ (peak) $= Q \times H_{OLP}$ (for high Qs)
$H_{OBP1} = -R3/R2$
$H_{OBP2} = 1$ (noninverting)

Circuit dynamics:
$H_{OBP1} = Q$

FIGURE 2. MODE 1a FOR NONINVERTING BAND-PASS AND LOW-PASS OUTPUTS

TYPICAL APPLICATION DATA



$f_o = f_{notch} \times \sqrt{R2/R4 + 1}$

$f_{notch} = f_{clock}/100$ or $f_{clock}/50$

$$Q = \frac{\sqrt{R2/R4 + 1}}{R2/R3}$$

$$H_{OLP} \text{ (as f approaches 0)} = \frac{-R2/R1}{R2/R4 + 1}$$

H_{OBP} (at $f = f_o$) $= -R3/R1$

$$H_{ON1} \text{ (as f approaches 0)} = \frac{-R2/R1}{R2/R4 + 1}$$

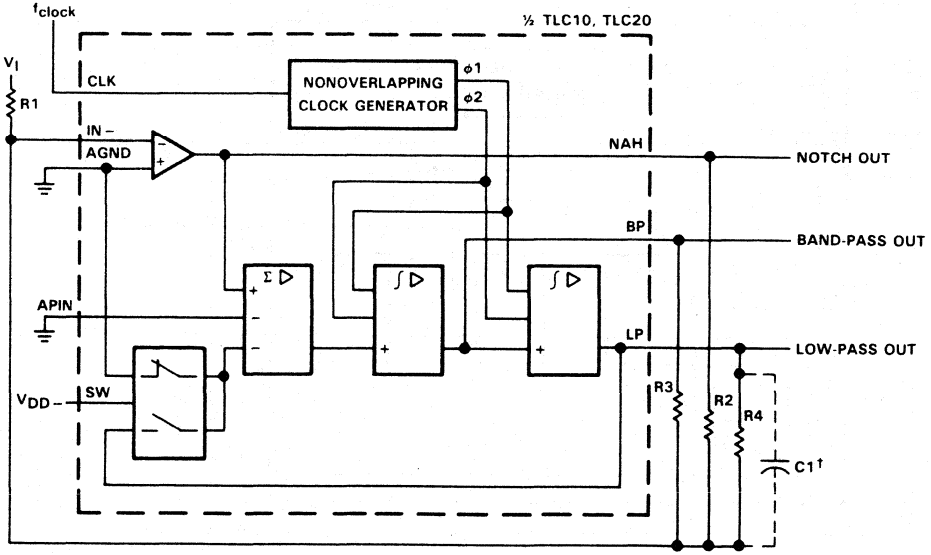
H_{ON2} (as f approaches 0.5 f_{clock}) $= -R2/R1$

Circuit dynamics:

$$H_{OBP} = Q\sqrt{H_{OLP} \cdot H_{ON2}} = Q\sqrt{H_{ON1} \cdot H_{ON2}}$$

FIGURE 3. MODE 2 FOR NOTCH 2, BAND-PASS, AND LOW-PASS OUTPUTS: $f_{notch} < f_o$

TYPICAL APPLICATION DATA



f_o = (f_{clock}/100 or f_{clock}/50) $\sqrt{R2/R4}$

Q = $\sqrt{R2/R4}$ × R3/R2

H_{OHP} (as f approaches 0.5 f_{clock}) = – R2/R1

H_{OLP} (as f approaches 0) = – R4/R1

H_{OBP} (at f = f_o) = – R3/R1

Circuit dynamics:

R2/R4 = H_{OHP}/H_{OLP}: H_{OBP} = $\sqrt{H_{OHP} \times H_{OLP}}$ × Q

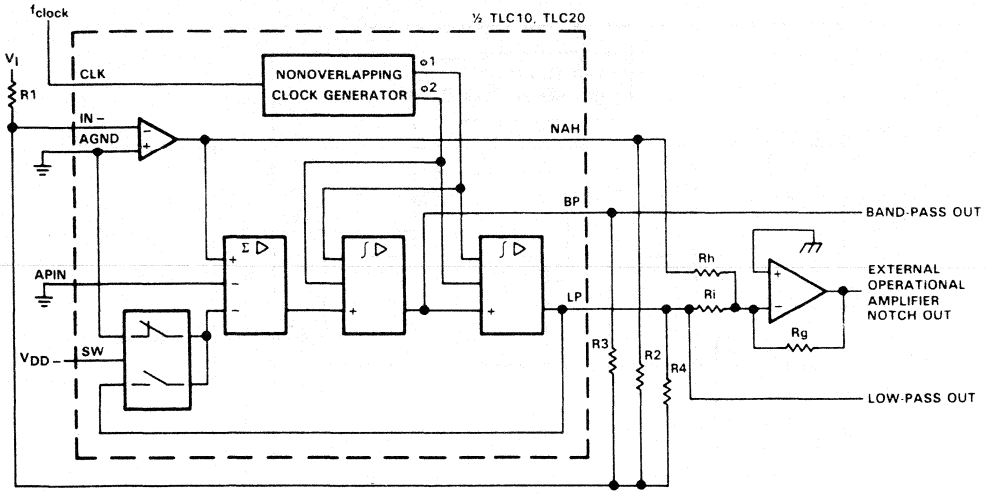
H_{OLP} (peak) = Q • H_{OLP} (for high Qs)

H_{OHP} (peak) = Q • H_{OHP} (for high Qs)

†In this mode, the feedback loop is closed around the input summing amplifier; the finite GBW product of this operational amplifier will cause a slight Q enhancement. If this is a problem, connect a low-value capacitor (10 pF to 100 pF) across R4 to provide some phase lead.

FIGURE 4. MODE 3 FOR HIGH-PASS, BAND-PASS, AND LOW-PASS OUTPUTS

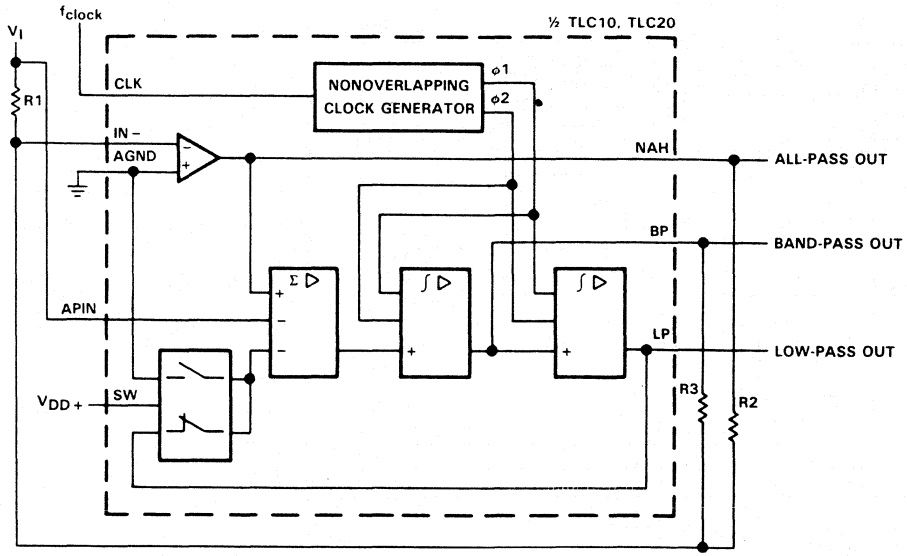
TYPICAL APPLICATION DATA



f_o = (f_{clock}/100 or f_{clock}/50) $\sqrt{R2/R4}$
Q = $\sqrt{R2/R4}$ × R3/R2
H_{OHP} = –R2/R1
H_{OBP} = –R3/R1
H_{OLP} = –R4/R1
f_{notch} = (f_{clock}/100 or f_{clock}/50) $\sqrt{Rh/Ri}$
H_{ON} (at f = f_o) = Q (Rg/Ri × H_{OLP} – Rg/Rh × HOHP)
H_{ON1} (as f approaches 0) = Rg/Ri × H_{OLP}
H_{ON2} (as f approaches 0.5 f_{clock}) = –Rg/Rh × H_{OHP}

FIGURE 5. MODE 3a FOR HIGH-PASS, BAND-PASS, LOW-PASS, AND NOTCH OUTPUTS WITH EXTERNAL OPERATIONAL AMPLIFIER

TYPICAL APPLICATION DATA



$f_o = f_{clock}/100$ or $f_{clock}/50$

$f_z = f_o$†

$Q = f_o/BW = R3/R2$

$Q_z = R3/R1$

H_{OAP} (at $0 \le f \le 0.5\ f_{clock}$) $= -R2/R1 = -1$
(for AP output R1 = R2)

H_{OLP} (as f approaches 0) $= -(R2/R1 + 1) = -2$

H_{OBP} (at $f = f_o$) $= -R3/R2\ (R2/R1 + 1) = -2\ (R3/R2)$

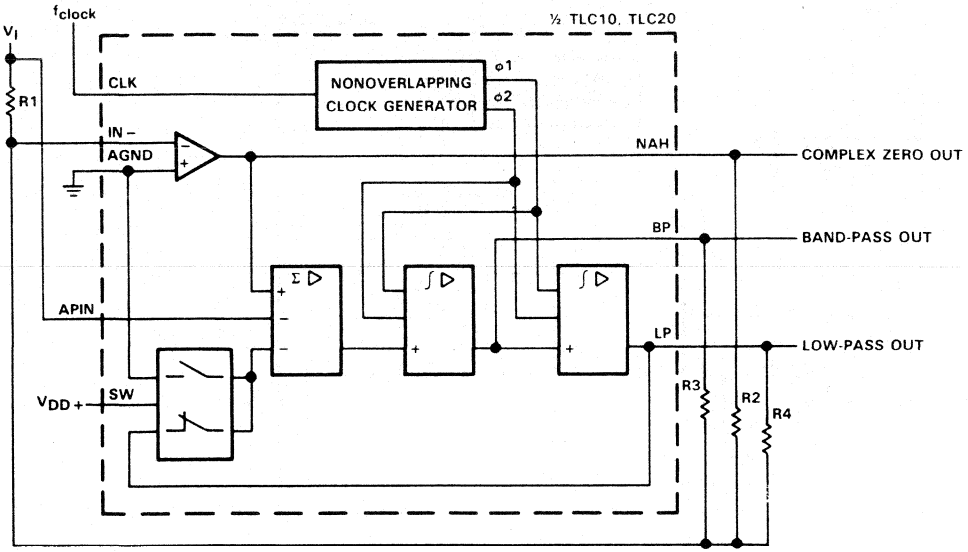
Circuit dynamics:

$H_{OBP} = H_{OLP} \cdot Q = (H_{OAP} + 1)\ Q$

†Due to the sampled-data nature of the filter, a slight mismatch of f_z and f_o occurs causing a 0.4-dB peaking around f_o of the all-pass filter amplitude response (which theoretically should be a straight line). If this is unacceptable, Mode 5 is recommended.

FIGURE 6. MODE 4 FOR ALL-PASS, BAND-PASS, AND LOW-PASS OUTPUTS

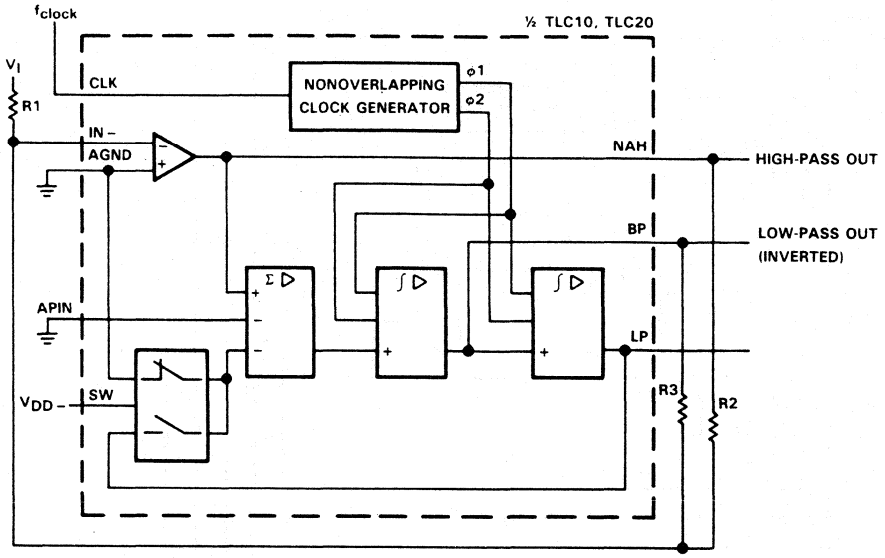
TYPICAL APPLICATION DATA



$f_o = \sqrt{R2/R4 + 1} \times (f_{clock}/100 \text{ or } f_{clock}/50)$
$f_z = \sqrt{1 - R1/R4} \times (f_{clock}/100 \text{ or } f_{clock}/50)$
$Q = \sqrt{R2/R4 + 1} \times R3/R2$
$Q_z = \sqrt{1 - R1/R4} \times R3/R1$
H_{OZ1} (as f approaches 0) = R2 (R4 – R1)/R1 (R2 + R4)
H_{OZ2} (as f approaches 0.5 f_{clock}) = R2/R1
$H_{OBP} = (R2/R1 + 1) \times R3/R2$
$H_{OLP} = (R2 + R1)/(R2 + R4) \times R4/R1$

FIGURE 7. MODE 5 FOR NUMERATOR COMPLEX ZEROS, BAND-PASS, AND LOW-PASS OUTPUTS

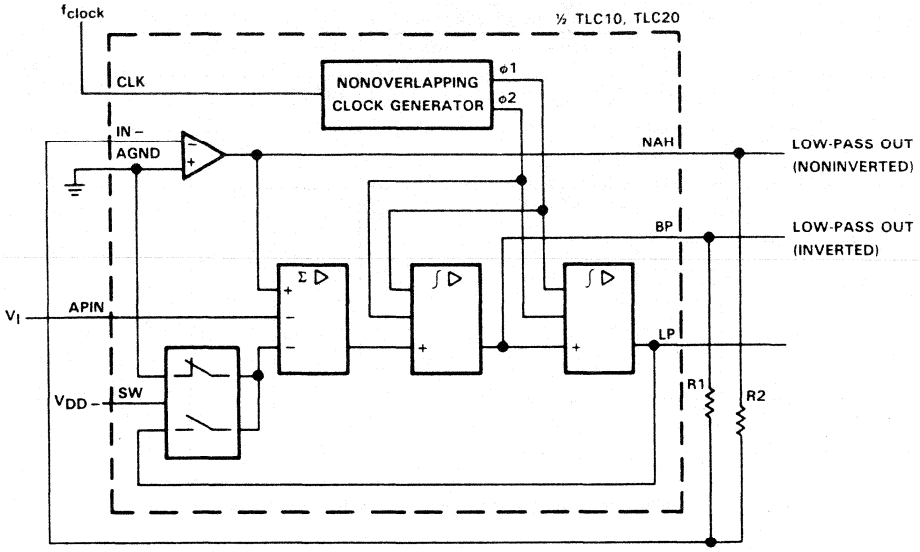
TYPICAL APPLICATION DATA



f_c = R2/R3 (f_{clock}/100 or f_{clock}/50)
H_{OLP} = – R3/R1
H_{OHP} = – R2/R1

FIGURE 8. MODE 6 FOR SINGLE-POLE HIGH-PASS AND LOW-PASS OUTPUT

TYPICAL APPLICATION DATA



f_c = R2/R3 • (f_{clock}/100 or f_{clock}/50)
H_{OLP1} = 1 (noninverting)
H_{OLP2} = – R3/R2

FIGURE 9. MODE 6a FOR SINGLE-POLE LOW-PASS OUTPUT (INVERTED AND NONINVERTED)

TYPICAL APPLICATION DATA

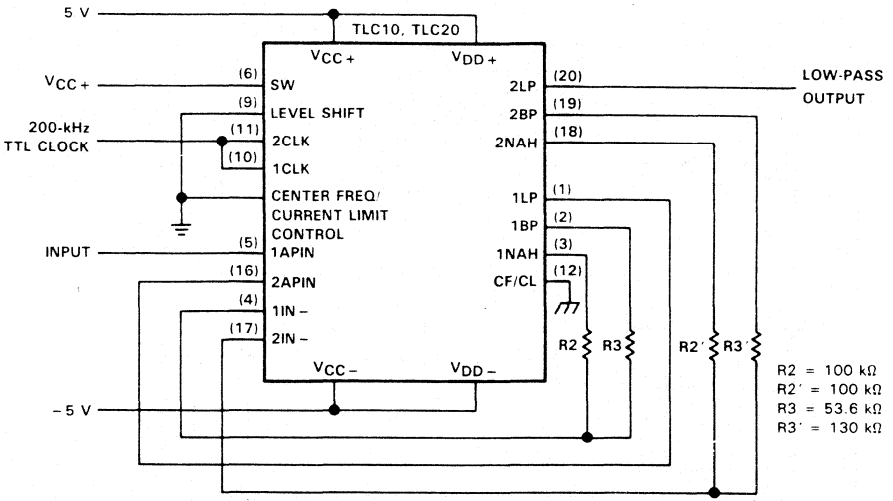
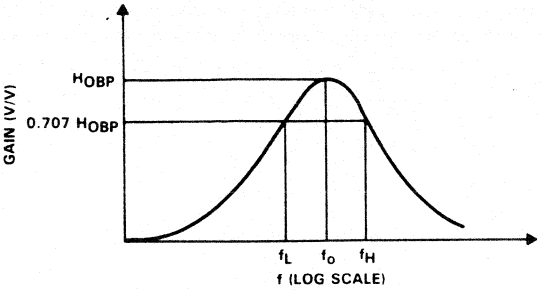


FIGURE 10. FOURTH-ORDER 2-kHz LOW-PASS BUTTERWORTH FILTER

filter terminology

f_c	The cutoff frequency of the low-pass or high-pass filter output
f_{clock}	The input clock frequency to the device
f_{notch}	The notch frequency of the notch output
f_o	The center frequency of the complex pole pair second-order function
f_z	The center frequency of the complex zero pair
H_{OBP}	The band-pass output voltage gain (V/V) at the band-pass center frequency
H_{OHP}	The high-pass output voltage gain (V/V) as the frequency approaches 0.5 f_{clock}
H_{OLP}	The low-pass output voltage gain (V/V) as the frequency approaches 0
HON	The notch output voltage gain (V/V) at the notch frequency
H_{ON1}	The low-side notch output voltage gain as the frequency approaches 0
H_{ON2}	The high-side notch output voltage gain as the frequency approaches 0.5 f_{clock}
H_{OZ1}	Gain at complex zero output (as $f \rightarrow 0$ Hz)
H_{OZ2}	Gain at complex zero output (as f approaches 0.5 f_{clock})
Q	The quality factor of the complex pole pair second-order function. Q is the ratio of f_o to the 3-dB bandwidth of the band-pass output. The value of Q also affects the possible peaking of the low-pass and high-pass outputs.
Q_z	The quality factor of the complex zero pair, if such a complex pair exists. This parameter is used when an all-pass filter output is desired.

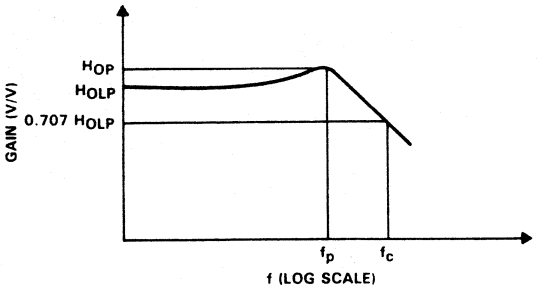


$$Q = \frac{f_o}{f_H - f_L} \; ; \; f_o = \sqrt{f_L f_H}$$

$$f_L = f_o \left(\frac{-1}{2Q} + \sqrt{\left(\frac{1}{2Q}\right)^2 + 1} \right)$$

$$f_H = f_o \left(\frac{1}{2Q} + \sqrt{\left(\frac{1}{2Q}\right)^2 + 1} \right)$$

FIGURE 11. BAND-PASS OUTPUT

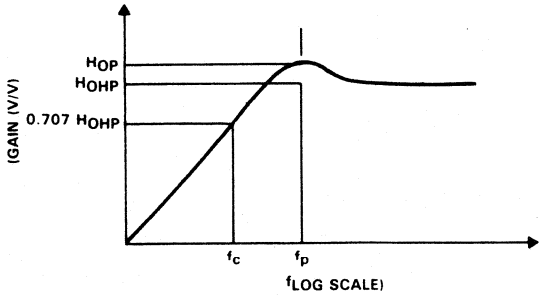


$$f_c = f_o \times \sqrt{\left(1 - \frac{1}{2Q^2}\right) + \sqrt{\left(1 - \frac{1}{2Q^2}\right)^2 + 1}}$$

$$f_p = f_o \sqrt{1 - \frac{1}{2Q^2}}$$

$$H_{OP} = H_{OLP} \times \frac{1}{\frac{1}{Q}\sqrt{1 - \frac{1}{4Q^2}}}$$

FIGURE 12. LOW-PASS OUTPUT



$$f_c = f_o \times \left[\sqrt{\left(1 - \frac{1}{2Q^2}\right) + \sqrt{\left(1 - \frac{1}{2Q^2}\right)^2 - 1}} \right]^{-1}$$

$$f_p = f_o \times \left[\sqrt{1 - \frac{1}{2Q^2}} \right]^{-1}$$

$$H_{OP} = H_{OHP} \times \frac{1}{\frac{1}{Q}\sqrt{1 - \frac{1}{4Q^2}}}$$

FIGURE 13. HIGH-PASS OUTPUT

General Information 1

Operational Amplifiers 2

Voltage Comparators 3

Timers 4

Analog to Digital Converters 5

Digital to Analog Converters 6

Analog Switches 7

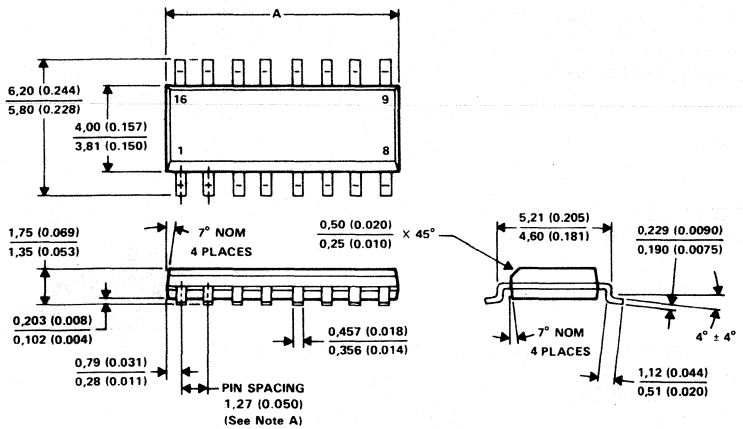
Switched Capacitor Filters 8

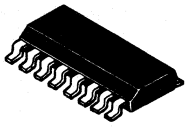
Packaging Information 9

D plastic "small outline" packages

Each of these "small outline" packages consists of a circuit mounted on a lead frame and encapsulated within a plastic compound. The compound will withstand soldering temperature with no deformation, and circuit performance characteristics will remain stable when operated in high-humidity conditions. Leads require no additional cleaning or processing when used in soldered assembly.

D PLASTIC PACKAGE
(16-pin package used for illustration)





DIM \ PINS	8	14	16
A MIN	4,80 (0.189)	8,55 (0.337)	9,80 (0.386)
A MAX	5,00 (0.197)	8,74 (0.344)	10,00 (0.394)

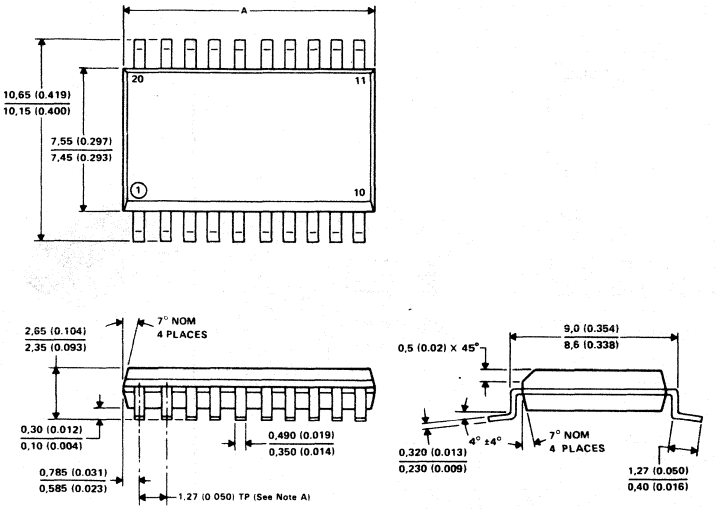
ALL LINEAR DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES

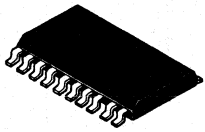
NOTES: A. Leads are within 0,25 (0.010) radius of true position at maximum material dimension.
B. Body dimensions do not include mold flash or protrusion.
C. Mold flash or protrusion shall not exceed 0,15 (0.006).
D. Lead tips to be planar within ±0,051 (0.002) exclusive of solder.

DW plastic "small outline" packages

Each of these "small outline" packages consists of a circuit mounted on a lead frame and encapsulated within a plastic compound. The compound will withstand soldering temperature with no deformation, and circuit performance characteristics will remain stable when operated in high-humidity conditions. Leads require no additional cleaning or processing when used in soldered assembly.

DW PLASTIC PACKAGE
(20-pin package used for illustration)





DIM \ PINS	16	20	24	28†
A MIN	10,16 (0.400)	12,70 (0.500)	15,29 (0.602)	17,68 (0.696)
A MAX	10,36 (0.408)	12,90 (0.508)	15,49 (0.610)	17,88 (0.704)

ALL LINEAR DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES

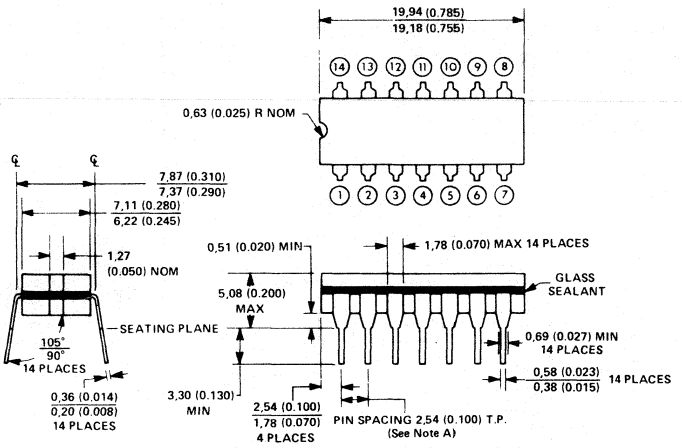
†The 28-pin package drawing is presently classified as Advance Information.

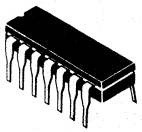
NOTES: A. Leads are within 0,25 (0.010) radius of true position at maximum material dimension.
B. Body dimensions do not include mold flash or protrusion.
C. Mold flash or protrusion shall not exceed 0,15 (0.006).
D. Lead tips to be planar within ±0,051 (0.002) exclusive of solder.

J ceramic dual-in-line package

This hermetically sealed dual-in-line package consists of a ceramic base, ceramic cap, and a lead frame. Hermetic sealing is accomplished with glass. The package is intended for insertion in mounting-hole rows on 7,62 (0.300) centers. Once the leads are compressed and inserted, sufficient tension is provided to secure the package in the board during soldering. Tin-plated (''bright-dipped'') leads require no additional cleaning or processing when used in soldered assembly.

14-PIN J CERAMIC





Falls Within JEDEC TO-116 and EIA MO-001AA Dimensions

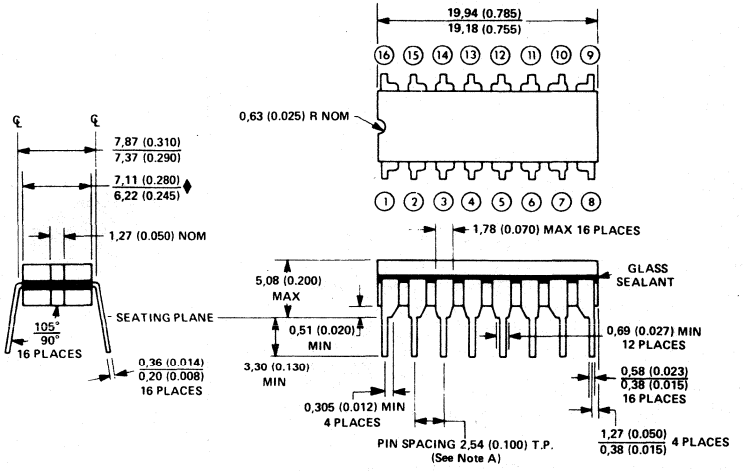
ALL LINEAR DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES

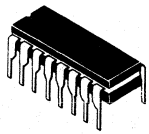
NOTE A: Each pin centerline is located within 0,25 (0.010) of its true longitudinal position.

J ceramic dual-in-line package

This hermetically sealed dual-in-line package consists of a ceramic base, ceramic cap, and a lead frame. Hermetic sealing is accomplished with glass. The package is intended for insertion in mounting-hole rows on 7,62 (0.300) centers. Once the leads are compressed and inserted, sufficient tension is provided to secure the package in the board during soldering. Tin-plated ("bright-dipped") leads require no additional cleaning or processing when used in soldered assembly.

16-PIN J CERAMIC





♦ For memories of 64 bits and up, a few MSI/LSI products in Series 54/74 and Series 54S/74S that are derived from memory circuit bars, and complex HCMOS parts, this maximum is 7,62 (0.300). All other dimensions apply without modification.

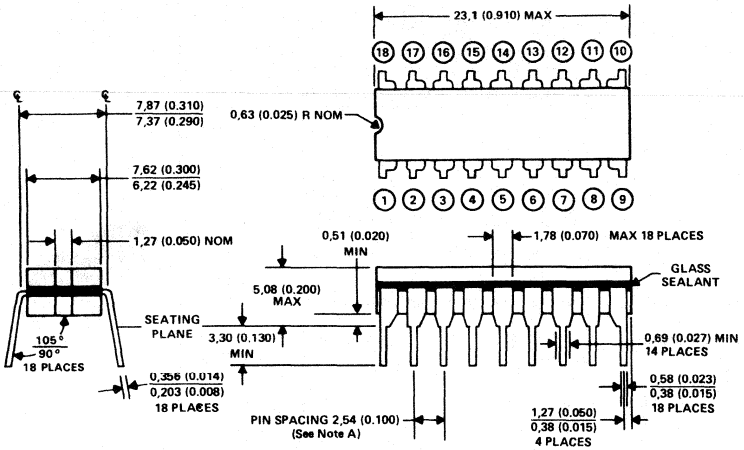
ALL LINEAR DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES

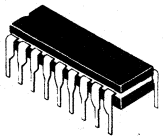
NOTE A: Each pin centerline is located within 0,25 (0.010) of its true longitudinal position.

J ceramic dual-in-line package

This hermetically sealed dual-in-line package consists of a ceramic base, ceramic cap, and a lead frame. Hermetic sealing is accomplished with glass. The package is intended for insertion in mounting-hole rows on 7,62 (0.300) centers. Once the leads are compressed and inserted, sufficient tension is provided to secure the package in the board during soldering. Tin-plated ("bright-dipped") leads require no additional cleaning or processing when used in soldered assembly.

18-PIN J CERAMIC





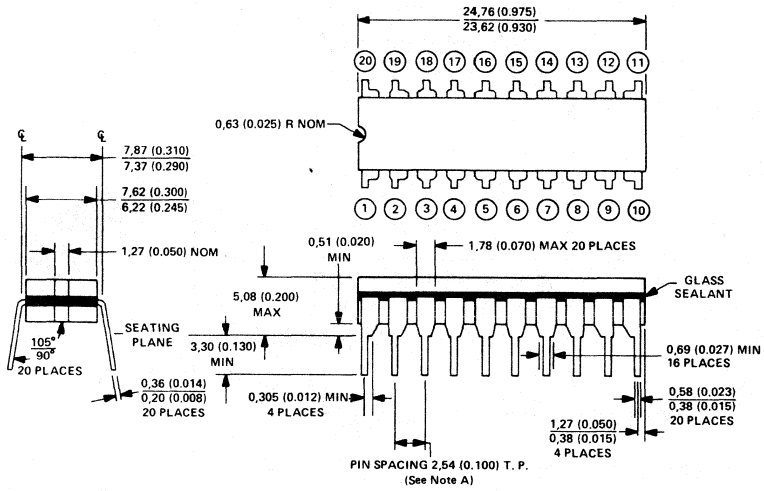
ALL LINEAR DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES

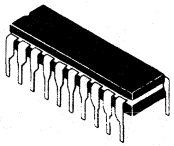
NOTE A: Each pin centerline is located within 0,25 (0.010) of its true longitudinal position.

J ceramic dual-in-line package

This hermetically sealed dual-in-line package consists of a ceramic base, ceramic cap, and a lead frame. Hermetic sealing is accomplished with glass. The package is intended for insertion in mounting-hole rows on 7,62 (0.300) centers. Once the leads are compressed and inserted, sufficient tension is provided to secure the package in the board during soldering. Tin-plated ("bright-dipped") leads require no additional cleaning or processing when used in soldered assembly.

20-PIN J CERAMIC





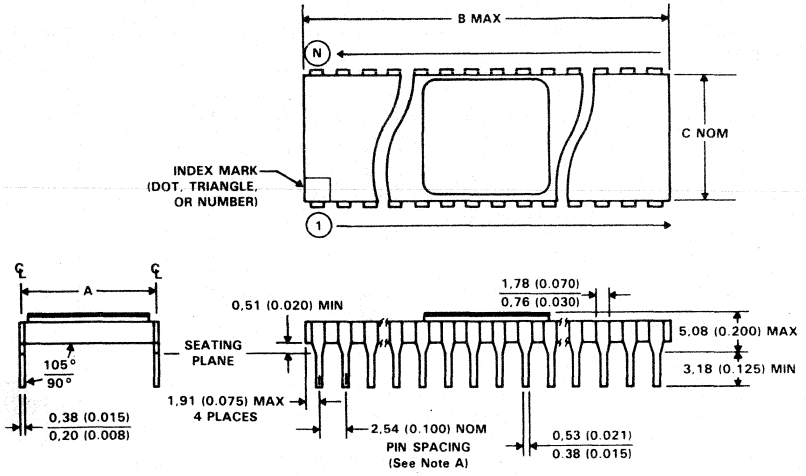
ALL LINEAR DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES

NOTE A: Each pin centerline is located within 0,25 (0.010) of its true longitudinal position.

JD ceramic side-braze dual-in-line packages

This is a hermetically sealed ceramic package with a metal cap and side-brazed tin-plated leads.

JD CERAMIC – SIDE-BRAZE



DIM \ PINS (N)	16	18	20	22	24
A +0,51 (+0.020) −0,25 (−0.010)	7,62 (0.300)	7,62 (0.300)	7,62 (0.300)	10,16 (0.400)	7,62 (0.300)
B (MAX)	20,57 (0.810)	23,11 (0.910)	25,65 (1.010)	27,94 (1.100)	30,86 (1.215)
C (NOM)	7,37 (0.290)	7,37 (0.290)	7,37 (0.290)	9,91 (0.390)	7,37 (0.290)

DIM \ PINS (N)	24	28	40	48	52	64
A +0,51 (+0.020) −0,25 (−0.010)	15,24 (0.600)	15,24 (0.600)	15,24 (0.600)	15,24 (0.600)	15,24 (0.600)	22,86 (0.900)
B (MAX)	31,8 (1.250)	36,8 (1.450)	52,1 (2.050)	62,2 (2.450)	67,3 (2.650)	82,6 (3.250)
C (NOM)	15,0 (0.590)	15,0 (0.590)	15,0 (0.590)	15,0 (0.590)	15,0 (0.590)	22,6 (0.890)

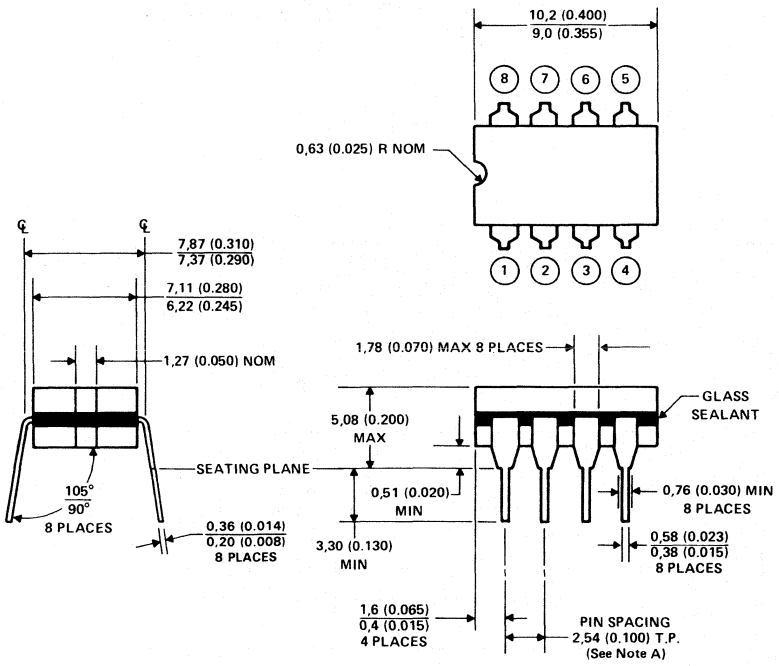
ALL LINEAR DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES

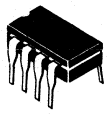
NOTE A: Each pin centerline is located within 0,25 (0.010) of its true longitudinal position.

JG ceramic dual-in-line package

This hermetically sealed dual-in-line package consists of a ceramic base, ceramic cap, and an 8-pin lead frame. The package is intended for insertion in mounting-hole rows 7,62 (0.300) centers (see Note A). Once the leads are compressed and inserted, sufficient tension is provided to secure the package in the board during soldering.

8-PIN JG CERAMIC





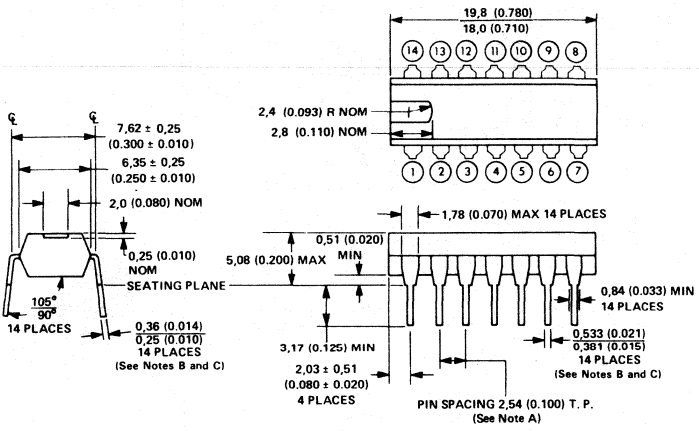
ALL LINEAR DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES

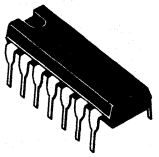
NOTE A: Each pin centerline is located within 0,25 (0.010) of its true longitudinal position.

N plastic dual-in-line package

This dual-in-line package consists of a circuit mounted on a lead frame and encapsulated within an electrically nonconductive plastic compound. The compound will withstand soldering temperature with no deformation, and circuit performance characteristics will remain stable when operated in high-humidity conditions. The package is intended for insertion in mounting-hole rows on 7,62 (0.300) centers. Once the leads are compressed and inserted, sufficient tension is provided to secure the package in the board during soldering. Leads require no additional cleaning or processing when used in soldered assembly.

14-PIN N PLASTIC





Falls Within JEDEC TO-116 and EIA MO-001AA Dimensions

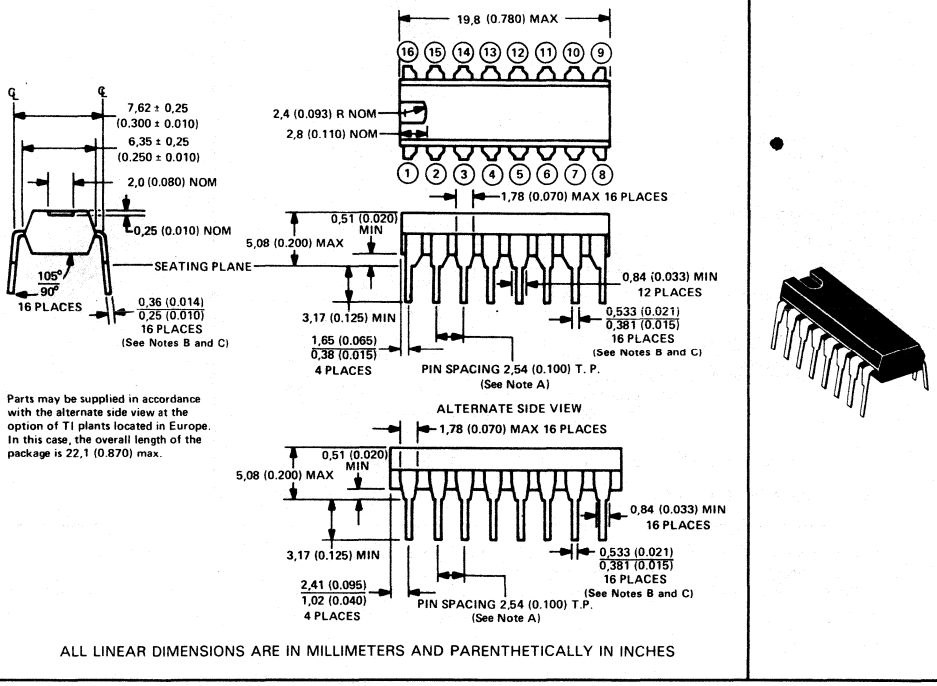
ALL LINEAR DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES

NOTES: A. Each pin centerline is located within 0,25 (0.010) of its true longitudinal position.
B. This dimension does not apply for solder-dipped leads.
C. When solder-dipped leads are specified, dipped area of the lead extends from the lead tip to at least 0,51 (0.020) above seating plane.

N plastic dual-in-line package

This dual-in-line package consists of a circuit mounted on a lead frame and encapsulated within an electrically nonconductive plastic compound. The compound will withstand soldering temperature with no deformation, and circuit performance characteristics will remain stable when operated in high-humidity conditions. The package is intended for insertion in mounting-hole rows on 7,62 (0.300) centers. Once the leads are compressed and inserted, sufficient tension is provided to secure the package in the board during soldering. Leads require no additional cleaning or processing when used in soldered assembly.

16-PIN N PLASTIC



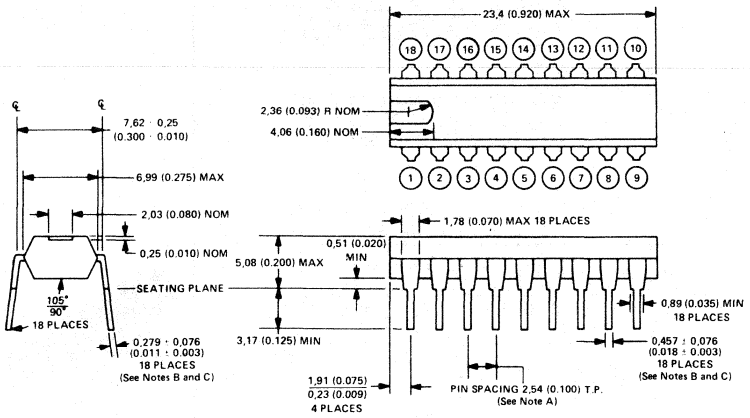
ALL LINEAR DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES

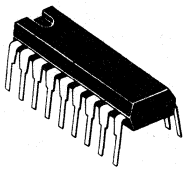
NOTES: A. Each pin centerline is located within 0,25 (0.010) of its true longitudinal position.
B. This dimension does not apply for solder-dipped leads.
C. When solder-dipped leads are specified, dipped area of the lead extends from the lead tip to at least 0,51 (0.020) above seating plane.

N plastic dual-in-line package

This dual-in-line package consists of a circuit mounted on a lead frame and encapsulated within an electrically nonconductive plastic compound. The compound will withstand soldering temperature with no deformation, and circuit performance characteristics will remain stable when operated in high-humidity conditions. The package is intended for insertion in mounting-hole rows on 7,62 (0.300) centers. Once the leads are compressed and inserted, sufficient tension is provided to secure the package in the board during soldering. Leads require no additional cleaning or processing when used in soldered assembly.

18-PIN N PLASTIC





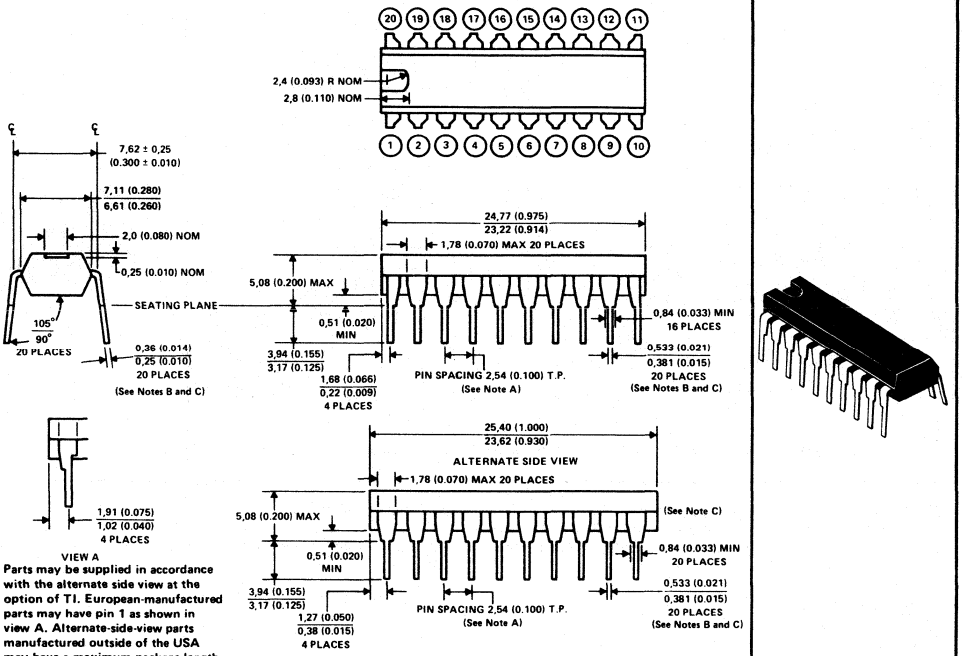
ALL LINEAR DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES

NOTES: A. Each pin centerline is located within 0,25 (0.010) of its true longitudinal position.
B. This dimension does not apply for solder-dipped leads.
C. When solder-dipped leads are specified, dipped area of the lead extends from the lead tip to at least 0,51 (0.020) above seating plane.

N plastic dual-in-line package

This dual-in-line package consists of a circuit mounted on a lead frame and encapsulated within an electrically nonconductive plastic compound. The compound will withstand soldering temperature with no deformation, and circuit performance characteristics will remain stable when operated in high-humidity conditions. The package is intended for insertion in mounting-hole rows on 7,62 (0.300) centers. Once the leads are compressed and inserted, sufficient tension is provided to secure the package in the board during soldering. Leads require no additional cleaning or processing when used in soldered assembly.

20-PIN N PLASTIC



Parts may be supplied in accordance with the alternate side view at the option of TI. European-manufactured parts may have pin 1 as shown in view A. Alternate-side-view parts manufactured outside of the USA may have a maximum package length of 26,7 (1.050).

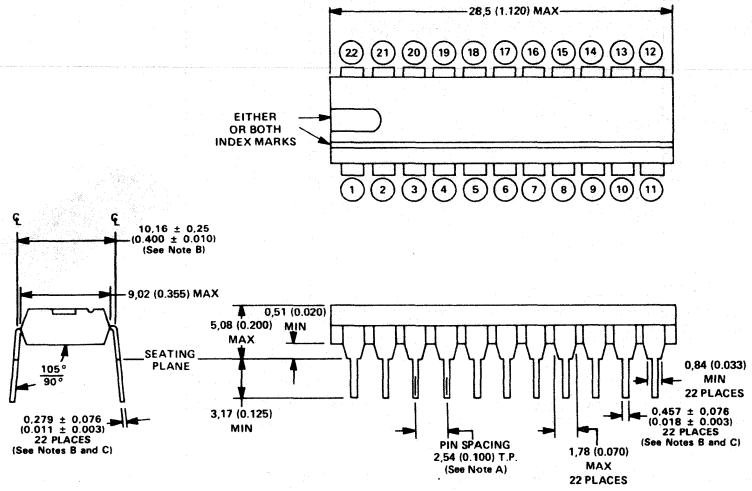
ALL LINEAR DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES

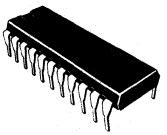
NOTES: A. Each pin centerline is located within 0,25 (0.010) of its true longitudinal position.
B. This dimension does not apply for solder-dipped leads.
C. When solder-dipped leads are specified, dipped area of the lead extends from the lead tip to at least 0,51 (0.020) above seating plane.

N plastic dual-in-line package

This dual-line package consists of a circuit mounted on a lead frame and encapsulated within an electrically nonconductive plastic compound. The compound will withstand soldering temperature with no deformation, and circuit performance characteristics will remain stable when operated in high-humidity conditions. The package is intended for insertion in mounting-hole rows on 10,16 (0.400) centers. Once the leads are compressed and inserted, sufficient tension is provided to secure the package in the board during soldering. Leads require no additional cleaning or processing when used in soldered assembly.

22-PIN N PLASTIC



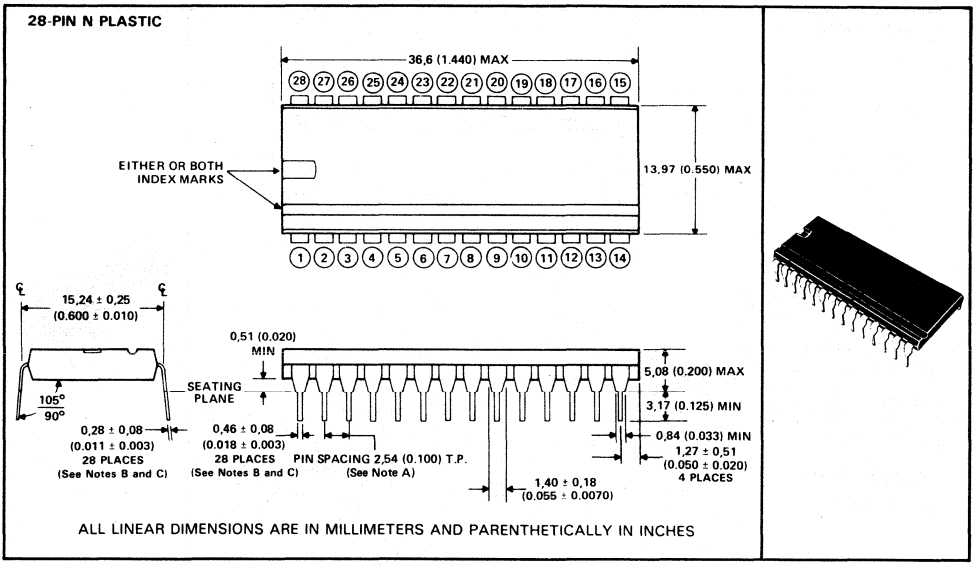


ALL LINEAR DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES

NOTES: A. Each pin centerline is located within 0,25 (0.010) of its true longitudinal position.
B. This dimension does not apply for solder-dipped leads.
C. When solder-dipped leads are specified, dipped area of the lead extends from the lead tip to at least 0,51 (0.020) above seating plane.

N plastic dual-in-line package

This dual-in-line package consists of a circuit mounted on a lead frame and encapsulated within an electrically nonconductive plastic compound. The compound will withstand soldering temperature with no deformation, and circuit performance characteristics will remain stable when operated in high-humidity conditions. The package is intended for insertion in mounting-hole rows on 15,24 (0.600) centers. Once the leads are compressed and inserted, sufficient tension is provided to secure the package in the board during soldering. Leads require no additional cleaning or processing when used in soldered assembly.

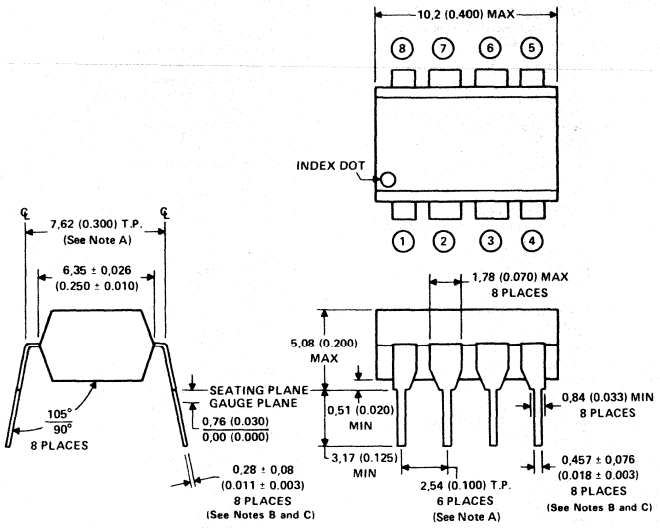


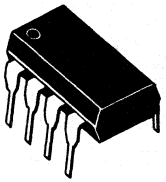
NOTES: A. Each pin centerline is located within 0,25 (0.010) of its true longitudinal position.
B. This dimension does not apply for solder-dipped leads.
C. When solder-dipped leads are specified, dipped area of the lead extends from the lead tip to at least 0,51 (0.020) above seating plane.

P dual-in-line plastic package

This package consists of a circuit mounted on an 8-pin lead frame and encapsulated within a plastic compound. The compound will withstand soldering temperature with no deformation, and circuit performance characteristics will remain stable when operated in high-humidity conditions. The package is intended for insertion in mounting-hole rows on 7,62 (0.300) centers (See Note A). Once the leads are compressed and inserted, sufficient tension is provided to secure the package in the board during soldering. Solder-plated leads require no additional cleaning or processing when used in soldered assembly.

8-PIN P PLASTIC





ALL LINEAR DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES

NOTES: A. Each pin centerline is located within 0,25 (0.010) of its true longitudinal position.
B. This dimension does not apply for solder-dipped leads.
C. When solder-dipped leads are specified, dipped area of the lead extends from the lead tip to at least 0,51 (0.020) above seating plane.

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